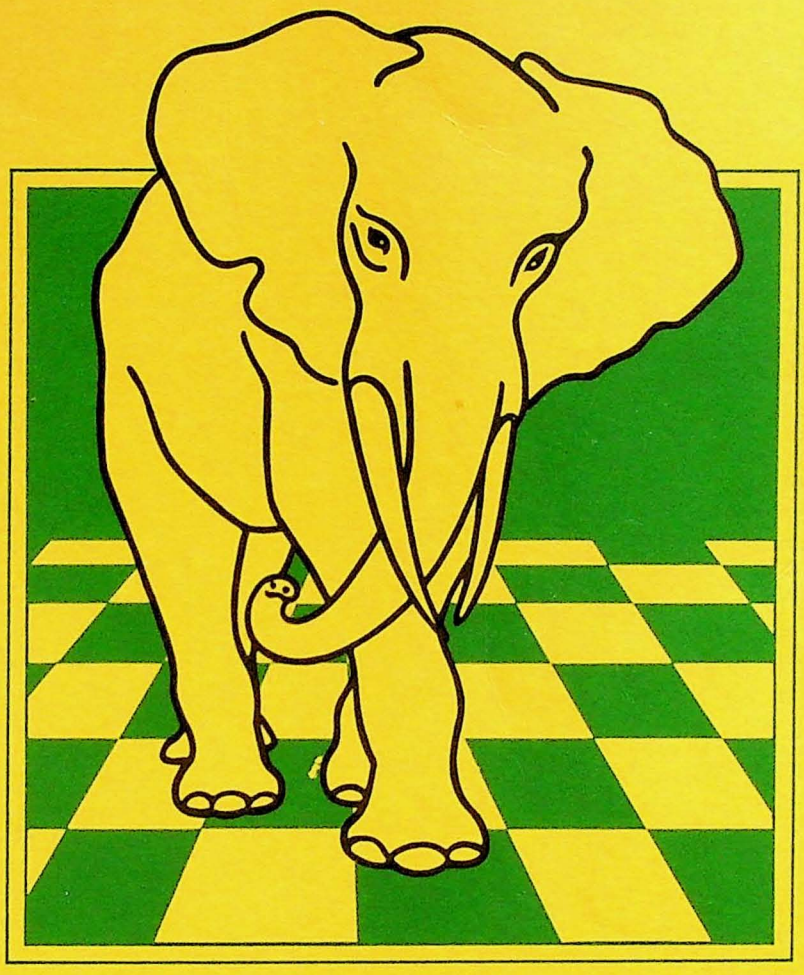
MEMORY



DATA MANUAL 1981·82

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MOTOROLA

SELECTOR GUIDES CROSS-REFERENCE 1

MOS Memories RAM, EPROM, EEPROM, ROM 2

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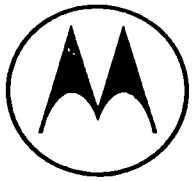

MOTOROLA

MEMORIES

Motorola has developed a very broad range of reliable MOS and bipolar memories for virtually any digital data processing system application. Complete specifications for the individual circuits are provided in the form of data sheets. In addition, selector guides are included to simplify the task of choosing the best combination of circuits for optimum system architecture.

New Motorola memories are being introduced continually. For the latest releases, and additional technical information or pricing, contact your nearest authorized Motorola distributor or Motorola sales office.

The information in this book has been carefully checked; no responsibility, however, is assumed for inaccuracies. Furthermore, this information does not convey to the purchaser of microelectronic devices any license under the patent rights of the manufacturer.

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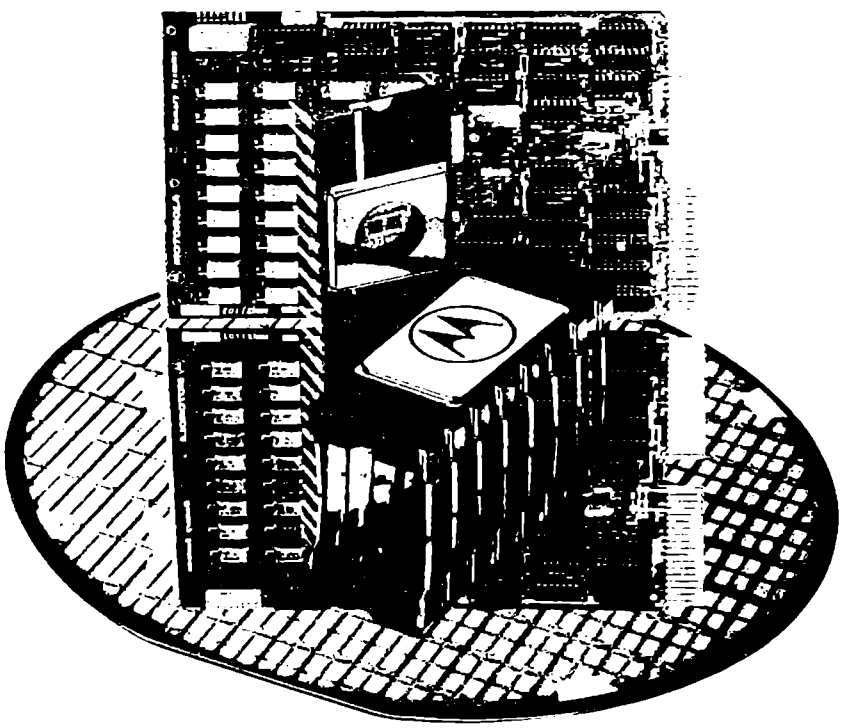
SELECTOR GUIDES CROSS-REFERENCE



NOTES

Not all package options are listed.

Operating temperature ranges:

MOS – 0°C to 70°C Selected MOS memories are offered in the following temperature ranges:
−40°C to +85°C ("G" series)
−55°C to +125°C ("E" series)

CMOS – 0°C to 70°C

ECL – Consult individual data sheets

TTL – Military −55°C to +125°C, Commercial 0°C to 70°C

FOOTNOTES

[1] Motorola's innovative pin #1 refresh.

[2] All MOS memory outputs are three-state except the open collector MCM2115A series.

[3] Character generators include shifted and unshifted characters, ASCII, alphanumeric control, math, Japanese, British, German, European and French symbols.

* To be introduced.

RAMs

MOS DYNAMIC RAMs

Organization	Part Number	Access Time (ns max)	Power Supplies	No. of Pins
4096 × 1	MCM4027AC-2	150	+12, ±5 V	16
4096 × 1	MCM4027AC-3	200	+12, ±5 V	16
4096 × 1	MCM4027AC-4	250	+12, ±5 V	16
16384 × 1	MCM4116BC15	150	+12, ±5 V	16
16384 × 1	MCM4116BC20	200	+12, ±5 V	16
16384 × 1	MCM4116BC25	250	+12, ±5 V	16
16384 × 1	MCM4116BC30	300	+12, ±5 V	16
16384 × 1	MCM4517C12	120	+5 V	16
16384 × 1	MCM4517C15	150	+5 V	16
16384 × 1	MCM4517C20	200	+5 V	16
32768 × 1	MCM6632L15[1]	150	+5 V	16
32768 × 1	MCM6632L20[1]	200	+5 V	16
32768 × 1	MCM6632L25[1]	250	+5 V	16
32768 × 1	MCM6633L15	150	+5 V	16
32768 × 1	MCM6633L20	200	+5 V	16
32768 × 1	MCM6633L25	250	+5 V	16
65536 × 1	MCM6664L15[1]	150	+5 V	16
65536 × 1	MCM6664L20[1]	200	+5 V	16
65536 × 1	MCM6664L25[1]	250	+5 V	16
65536 × 1	MCM6665L15	150	+5 V	16
65536 × 1	MCM6665L20	200	+5 V	16
65536 × 1	MCM6665L25	250	+5 V	16

TTL BIPOLAR RAMs

Organization	Part Number	Access Time (ns max)	Output	No. of Pins
256 × 4	MCM93L412*	55	Open Collector	22
256 × 4	MCM93L422*	55	3-State	22
256 × 4	MCM93412	45	Open Collector	22
256 × 4	MCM93422	45	3-State	22
256 × 9	MCM93478*	60	Open Collector	24
256 × 9	MCM93479*	60	3-State	24
1024 × 1	MCM93415	45	Open Collector	16
1024 × 1	MCM93425	45	3-State	16

See Notes on Page 1-2.

MOS STATIC RAMs (+5 Volts)

Organization	Part Number	Access Time (ns max)	No. of Pins
128 x 8	MCM6810	450	24
128 x 8	MCM68A10	360	24
128 x 8	MCM68B10	250	24
1024 x 4	MCM2114P20	200	18
1024 x 4	MCM2114P25	250	18
1024 x 4	MCM2114P30	300	18
1024 x 4	MCM2114P45	450	18
1024 x 4	MCM21L14P20	200	18
1024 x 4	MCM21L14P25	250	18
1024 x 4	MCM21L14P30	300	18
1024 x 4	MCM21L14P45	450	18
1024 x 1	MCM2115AC45[2]	45	16
1024 x 1	MCM2115AC55[2]	55	16
1024 x 1	MCM2115AC70[2]	70	16
1024 x 1	MCM21L15AC45[1]	45	16
1024 x 1	MCM21L15AC70[2]	70	16
1024 x 1	MCM2125AC45	45	16
1024 x 1	MCM2125AC55	55	16
1024 x 1	MCM2125AC70	70	16
1024 x 1	MCM21L25AC45	45	16
1024 x 1	MCM21L25AC70	70	16
4096 x 1	MCM2147C55	55	18
4096 x 1	MCM2147C70	70	18
4096 x 1	MCM2147C85	85	18
1024 x 4	MCM2148C55*	55	18
1024 x 4	MCM2148C70*	70	18
1024 x 4	MCM2148C85*	85	18
1024 x 4	MCM2149C55*	55	18
1024 x 4	MCM2149C70*	70	18
1024 x 4	MCM2149C85*	85	18

CMOS STATIC RAMs (+5 Volts)

Organization	Part Number	Access Time (ns max)	No. of Pins
256 x 4	MCM5101P65	650	22
256 x 4	MCM5101P80	800	22
256 x 4	MCM51L01P45	450	22
256 x 4	MCM51L01P65	650	22
1024 x 1	MCM6508C30	300	16
1024 x 1	MCM6508C46	460	16
1024 x 1	MCM6518C30	300	18
1024 x 1	MCM6518C46	460	18

See Notes on Page 1-2.

ECL BIPOLAR RAMs

Organization	Part Number	Access Time (ns max)	Output	No. of Pins
8 × 2	MCM10143	15	ECL output	24
256 × 1	MCM10144	26	ECL output	16
16 × 4	MCM10145	15	ECL output	16
1024 × 1	MCM10146	29	ECL output	16
1024 × 1	MCM10146A*	15	ECL output	16
128 × 1	MCM10147	15	ECL output	16
256 × 1	MCM10152	15	ECL output	16
256 × 4	MCM10422	15	ECL output	24
4096 × 1	MCM10470	35	ECL output	18
4096 × 1	MCM10470A*	20	ECL output	18
4096 × 1	MCM10470B* (Low power)	35	ECL output	18
1024 × 4	MCM10474	25	ECL output	24

EPROMs

MOS EPROMs

Organization	Part Number	Access Time (ns max)	Power Supplies	No. of Pins
1024 × 8	MCM2708C	450	+12, ±5 V	24
1024 × 8	MCM27A08C	300	+12, ±5 V	24
1024 × 8	MCM68708C	450	+12, ±5 V	24
1024 × 8	MCM68A708C	300	+12, ±5 V	24
2048 × 8	TMS2716C	450	+12, ±5 V	24
2048 × 8	TMS27A16C	300	+12, ±5 V	24
2048 × 8	MCM2716C	450	+5 V	24
2048 × 8	MCM2716C35	350	+5 V	24
2048 × 8	MCM27L16C	450	+5 V	24
2048 × 8	MCM27L16C35	350	+5 V	24
4096 × 8	MCM2532C	450	+5 V	24
4096 × 8	MCM2532C35	350	+5 V	24
4096 × 8	MCM25L32C	450	+5 V	24
4096 × 8	MCM25L32C35	350	+5 V	24
8192 × 8	MCM68764C	450	+5 V	24
8192 × 8	MCM68764C35	350	+5 V	24
8192 × 8	MCM68L764C	450	+5 V	24
8192 × 8	MCM68L764C35	350	+5 V	24
8192 × 8	MCM68766C35	350	+5 V	24

EEPROM

MOS EEPROM

Organization	Part Number	Access Time	Power Supplies	No. of Pins
16 × 16	MCM2801	10 μs	+5 V	14
32 × 32	MCM2802	10 μs	+5 V	14
2K × 8	MCM2816	0.45	+5 V	24

See Notes on Page 1-2.

ROMs

MOS STATIC ROMs (+ 5 Volts)

Character Generators[3]

Organization	Part Number	Access Time (ns max)	No. of Pins
128 x (7 x 5)	MCM6670P	350	18
128 x (7 x 5)	MCM6674P	350	18
128 x (9 x 7)	MCM66700P	350	24
128 x (9 x 7)	MCM66710P	350	24
128 x (9 x 7)	MCM66714P	350	24
128 x (9 x 7)	MCM66720P	350	24
128 x (9 x 7)	MCM66730P	350	24
128 x (9 x 7)	MCM66734P	350	24
128 x (9 x 7)	MCM66740P	350	24
128 x (9 x 7)	MCM66750P	350	24
128 x (9 x 7)	MCM66760P	350	24
128 x (9 x 7)	MCM66770P	350	24
128 x (9 x 7)	MCM66780P	350	24
128 x (9 x 7)	MCM66790P	350	24

Binary ROMs (+ 5 Volts)

Organization	Part Number	Access Time (ns max)	No. of Pins
1024 x 8	MCM68A308P	350	24
1024 x 8	MCM68A308P7	350	24
1024 x 8	MCM68B308P	250	24
2048 x 8	MCM68A316AP	350	24
2048 x 8	MCM68A316EP	350	24
2048 x 8	MCM68A316P91	350	24
4096 x 8	MCM68A332P	350	24
4096 x 8	MCM68A332P2	350	24
8192 x 8	MCM68A364P	350	24
8192 x 8	MCM68A364P3	350	24
8192 x 8	MCM68B364P	250	24
8192 x 8	MCM68365P25	250	24
8192 x 8	MCM68365P35	350	24
8192 x 8	MCM68366P25	250	24
8192 x 8	MCM68366P35	350	24
8192 x 8	MCM68766C45	450	24

CMOS ROMs (+ 5 Volts)

Organization	Part Number	Access Time (ns max)	No. of Pins
256 x 4	MCM14524	1200	16
2048 x 8	MCM65516C43	430	18
2048 x 8	MCM65516C55	550	18

See Notes on Page 1-2.

PROMs
ECL PROMs

Organization	Part Number	Access Time (ns max)	Output	No. of Pins
32 × 8	MCM10139	20	ECL output	16
256 × 4	MCM10149	25	ECL output	16

TTL PROMs

Organization	Part Number	Access Time (ns max)	Output	No. of Pins
512 × 8	MCM7640	70	Open Collector	24
512 × 8	MCM7641	70	3-State	24
1024 × 4	MCM7642	70	Open Collector	18
1024 × 4	MCM7643	70	3-State	18
1024 × 8	MCM7680	70	Open Collector	24
1024 × 8	MCM7681	70	3-State	24
2048 × 4	MCM7684*	70	Open Collector	18
2048 × 4	MCM7685*	70	3-State	18
2048 × 4	MCM7688*	–	Open Collector with Registers	20
2048 × 4	MCM7689*	–	3-State with Registers	20
2048 × 8	MCM76161*	70	3-State	24

See Notes on Page 1-2.

Memory Systems Board Selector Guide and Cross Reference

DEC COMPUTERS	MEMORY SIZE	MOTOROLA PART NUMBER	DEC PART NUMBER	INTEL PART NUMBER	MOSTEK PART NUMBER	NATIONAL PART NUMBER	MONOLITHIC SYSTEMS PART NUMBER	DATARAM PART NUMBER	PLESSEY PART NUMBER	CDC PART NUMBER	STANDARD MEMORIES PART NUMBER
• LSI 11 LSI 11/02 LSI 11/23 PDP 11/03 (Q Bus Plus slot)	8K × 16 16K × 16 32K × 16 64K × 16 128K × 16 8K × 18 16K × 18 32K × 18 64K × 18 128K × 18	MMS1102-31 MMS1122N3032 MMS1122N3064 MMS1132 MMS1132 MMS1102-31PC MMS1102-32PC MMS1102-34PC MMS1132 MMS1132	MSV11-BG MSV11-DC MSV11-DD MSV11-EC MSV11-EB MSV11-ED	CM 5004-616 CM 5004 632 CM 5004 816 CM 5004 832	MK 8005-03 MK 8005 02 MK 8005 00 MK 8005-14 MK 8005-12 MK 8005 10	NS23P NS23P	MSC4601 16K × 16 MSC4601 32K × 16 MSC4604 16K × 18 MSC4604 32K × 18	DR-115S DR-115S DR 115S DR-113S DR-113S DR 115S DR-115S DR 115S DR 113S DR-113S	PM SV32A/103 PM-SV32A/102 PM-SV32A/100 PM SV32AP/103 PM SV32AP/102 PM-SV32AP/100	94123-16 94123 32	
• PDP 11/04 05, 10, 34, 35, 40, 45 50, 55, 60 (MUDBUS SPC slot)	16K × 16 32K × 16 48K × 16 64K × 16 16K × 18 32K × 18 48K × 18 64K × 18	MMS1117-×2 MMS1117-×4 MMS1117-×6 MMS1117-×8 MMS1117-×2PC MMS1117-×4PC MMS1117-×6PC MMS1117-×8PC		CM 5034 832 CM 5034 848 CM 5034 864	MK 8001 02 MK 8001 01 MK 8001 00 MK 8011 02 MK 8011 01 MK 8011 00	NS11-34-16 NS11-34 32 NS11-34P 16 NS11-34P 32	MSC3503 16K × 16 MSC3503 32K × 16 MSC3503 48K × 16 MSC3503 64K × 16 MSC3605 16K × 18 MSC3605 32K × 18 MSC3605 48K × 18 MSC3605 64K × 18	DR-114S DR-114S DR 114S DR 114S DR 114S DR 114S DR 114S DR-114S	PM-S1164/102 PM S1164/101 PM-S1164/100 PM-S1164A/102 PM S1164A/101 PM-S1164A/100	94234-16 94234-32	• PINCOMM PS PINCOMM PS PINCOMM PS PINCOMM PS PINCOMM PS PINCOMM PS PINCOMM PS PINCOMM PS
• PDP-11/04 PDP-11/34 PDP-11/60 (Mudbus slot)	16K × 18 32K × 18 48K × 18 64K × 18 96K × 18	MMS1128P×016 MMS1128P×032 MMS1128P×048 •MMS1128P×064 †MMS1128P×096	MS11-LA MS11-LB MS11-LC	CM 5034 832 CM 5034 848	MK 8011 02 MK 8011 01 MK 8012 00	NS11-34P-16 NS11-34P 32	MSC3606 16K × 18 MSC3606 32K × 18 MSC3606 48K × 18 MSC3606 128K × 18	DR 114S DR 114S DR 114S DR-114S DR-114S	PM S11L/100 PM-S11L/100	94234 16 94234 32	• PINCOMM PS PINCOMM PS PINCOMM PS PINCOMM PS
• PDP-11/04 PDP-11/34 PDP 11/60 (Mudbus slot)	32K × 18 64K × 18 96K × 18 128K × 18 256K × 18 512K × 18	MMS1119P×032 MMS1119P×064 MMS1119P×096 MMS1119P×128 •MMS1119P×256 •MMS1119P×512	MS11-LA MS11-LB MS11-LC MS11-LD	CM 5034 832 CM 5034 864	MK 8012 03 MK 8012 02 MK 8012 01 MK 8012 00	NS11-34Q NS11-34Q NS11-34Q	MSC3606 32K × 18 MSC3606 64K × 18 MSC3606 96K × 18 MSC3606 128K × 18	DR-114S DR 114S DR 114S DR 114S	PM S11L/100 PM S11L/100 PM S11L/100 PM S11L/100	94134 32 94134 64 94134 128	• PINCOMM PS PINCOMM PS
• PDP-11/70 (Add-In)	32K × 39	MMS1170E1064									• PINCOMM 70S
• VAX 11/780 (Memory SUB-SYSTEM slot)	32K × 72	MMS780AE1032	MS780-DA (M8210)		MK 8016 01	NS 760	MSC 3610	DR-178S			• PINCOMM 780S

† Populated with 32K RAMS
• Populated with 64K RAMS
× = 3 for fast speed
× = 4 for standard speed
P PC- Parity • Controller eliminates the need for DEC's 7850 controller

- DEC, LSI-11, PDP-11, and VAX-11/780 are trademarks of Digital Equipment Corp
PINCOMM is a registered trademark of Trendata
Standard Memories

NOTE THIS DOCUMENT IS INTENDED AS AN AID TO OUR CUSTOMERS IN SELECTING THE PROPER ADD IN MEMORY BOARD WE RECOMMEND THAT THE DATA SHEET & TECHNICAL MANUALS FOR THE PARTICULAR BOARD IN QUESTION BE USED BEFORE INSTALLATION

INTEL MICROCOMPUTERS	MEMORY SIZE	MOTOROLA PART NUMBER	INTEL PART NUMBER	NATIONAL PART NUMBER	CHRISLIN PART NUMBER
• iSBC 80/10, 80/20, 86/12 • (MULTIBUS) MDS Development System SYSTEM 80	16K × 8 32K × 8 48K × 8 64K × 8 16K × 9 32K × 9 48K × 9 64K × 9	MMS8016 MMS8032 MMS8048 MMS8064 MMS8016P MMS8032P MMS8048P MMS8064P	SBC 016 SBC 032 SBC 048 SBC 064	• BLC 016 BLC 032 BLC 048 BLC 064	CI 8060 CI 8060 CI 8060
• iSBC 80/10, 80/20 † MDS Development System SYSTEM 80	16K × 8 32K × 8	MMS80810-1 MMS80810	SBC 016 SBC 032	BLC 016 BLC 032	CI 8080 CI 8080

- MULTIBUS and iSBC are trademarks of INTEL Corp
BLC is a trademark of NATIONAL Semiconductor Corp

† Compatible with limitations

THE OFFICIAL MOS MEMORY CROSS-REFERENCE
From Motorola

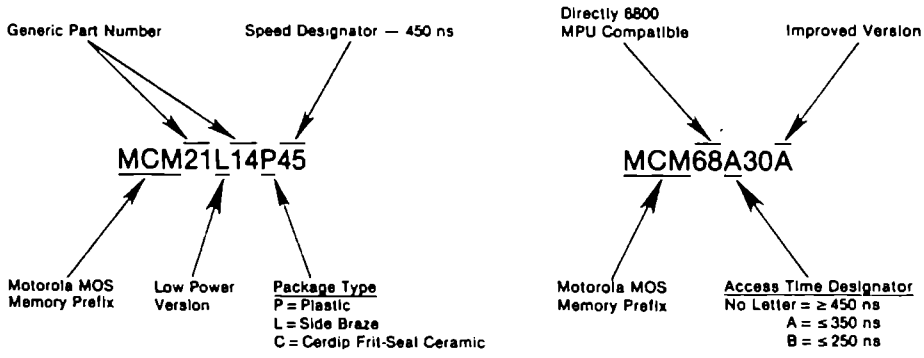
Part Number	Organization Description	Motorola's Access Time (ns Max)	Number of Pins	Power Supplies	Motorola Pin-to-Pin Replacement
AMD					
Am2708	1024 x 8 EPROM	300-450	24	+12, ±5 V	MCM2708
Am2716	2048 x 8 EPROM	450	24	+5 V	MCM2716
Am4044	4096 x 1 SRAM	200-450	18	+5 V	MCM66L41
Am9016	16,384 x 1 DRAM	150-300	16	+12, ±5 V	MCM4116
Am9114	1024 x 4 SRAM	200-450	18	+5 V	MCM2114
Am91L14	1024 x 4 SRAM	200-450	18	+5 V	MCM21L14
Am9147	4096 x 1 SRAM	55-85	18	+5 V	MCM2147
Am9208B	1024 x 8 SROM	350	24	+5 V	MCM68A308
Am9217	2048 x 8 SROM	350	24	+5 V	MCM68A316A
Am9218	2048 x 8 SROM	350	24	+5 V	MCM68A316E
Am9232	4096 x 8 SROM	350	24	+5 V	MCM68A332
AMI					
S2114	1024 x 4 SRAM	200-450	18	+5 V	MCM2114
S2114L	1024 x 4 SRAM	200-450	18	+5 V	MCM21L14
S2147	4096 x 1 SRAM	70-100	18	+5 V	MCM2147
S4264	8192 x 8 SROM	350	24	+5 V	MCM68A364
S5101	256 x 4 SRAM	450-800	22	+5 V	MCM5101
S6508	1024 x 1 SRAM	300-460	16	+5 V	MCM6508
S6518	1024 x 1 SRAM	300-460	18	+5 V	MCM6518
S6810	128 x 8 SRAM	250-450	24	+5 V	MCM6810
S6830	1024 x 8 SROM	350	24	+5 V	MCM68A30A
S6831A	2048 x 8 SROM	350	24	+5 V	MCM68A316A
S6831B	2048 x 8 SROM	350	24	+5 V	MCM68A316E
S68332	4096 x 8 ROM	350	24	+5 V	MCM68A332
FAIRCHILD					
F16K	16,384 x 1 DRAM	150-300	16	+12, ±5 V	MCM4116
2114	1024 x 4 SRAM	200-450	18	+5 V	MCM2114
F2708	1024 x 8 EPROM	450	24	+12, ±5 V	MCM2708
F2708I	1024 x 8 EPROM	300	24	+12, ±5 V	MCM27A08
2716	2048 x 8 EPROM	450	24	+5 V	MCM2716
3508	1024 x 8 SROM	350	24	+5 V	MCM68A308
F3516E	2048 x 8 SROM	350	24	+5 V	MCM68A316E
FM4027	4096 x 1 DRAM	120-250	16	+12, ±5 V	MCM4027A
F68B10	128 x 8 SRAM	250-450	24	+5 V	MCM68B10
F68B308	1024 x 8 SROM	250-350	24	+5 V	MCM68B308
F68708	1024 x 8 EPROM	450	24	+12, ±5 V	MCM68708
FUJITSU					
MB2147	4096 x 1 SRAM	70-100	18	+5 V	MCM2147
MBM2716	2048 x 8 EPROM	450	24	+5 V	MCM2716
MB4044	4096 x 1 SRAM	200-450	18	+5 V	MCM6641
MB8114	1024 x 4 SRAM	200-450	18	+5 V	MCM2114
MB8116	16,384 x 1 DRAM	150-300	16	+12, ±5 V	MCM4116
MB8227	4096 x 1 DRAM	120-250	16	+12, ±5 V	MCM4027A
MB8308	1024 x 8 SROM	350	24	+5 V	MCM68A308
MB8518H	1024 x 8 EPROM	450	24	+12, ±5 V	MCM2708
GENERAL INSTRUMENT					
RO3-8316B	2048 x 8 SROM	350	24	+5 V	MCM68A316A
RO3-9316B	2048 x 8 SROM	350	24	+5 V	MCM68A316E
RO3-9332C	4096 x 8 SROM	350	24	+5 V	MCM68A332
RO3-9364B	8092 x 8 SROM	350	24	+5 V	MCM68365-35

Part Number	Organization Description	Motorola's Access Time (ns Max)	Number of Pins	Power Supplies	Motorola Pin-to-Pin Replacement
HARRIS					
6501	256 x 4 SRAM	450-800	22	+5 V	MCM5101
6508	1024 x 1 SRAM	300-460	16	+5 V	MCM6508
6514	1024 x 1 SRAM	200-450	18	+5 V	MCM65114
6518	1024 x 1 SRAM	300-460	18	+5 V	MCM6518
HITACHI					
HM4334P	1024 x 4 SRAM	300-450	18	+5 V	MCM65114
HM435101	256 x 4 CMOS SRAM	450-800	22	+5 V	MCM5101
HM482316EP	2048 x 8 SROM	350	24	+5 V	MCM68A316E
HM462532	4096 x 8 EPROM	450	24	+5 V	MCM2532
HM462708	1024 x 8 EPROM	450	24	+5 V	MCM2708
HM462716	2048 x 8	450	24	+5 V	MCM2716
HM48332	4096 x 8 SROM	350	24	+5 V	MCM68A332
HM46364	8192 x 8 SROM	350	24	+5 V	MCM68A364
HM488A10	128 x 8 SRAM	350	24	+5 V	MCM68A10
HM46830	1024 x 8 SROM	350	24	+5 V	MCM68A30A
HM4716	16,384 x 1 DRAM	150-300	16	+12, ±5 V	MCM4116
HM472114A	1024 x 1 SRAM	200-450	18	+5 V	MCM2114
HM48016	2048 x 8 EEPROM	350	24	+5 V	MCM2816
HM4816	16,384 x 1 DRAM	100-200	16	+5 V	MCM4517
HM4847	4096 x 1 SRAM	55-85	18	+5 V	MCM2147
HM4864	65,536 x 1 DRAM	150-200	16	+5 V	MCM6665
HM6116P	2048 x 8 CMOS SRAM	120-200	18	+5 V	MCM65116
HM6147P	4096 x 1 CMOS SRAM	55-70	18	+5 V	MCM65147
HM6148P	1024 x 4 CMOS SRAM	55-85	18	+5 V	MCM65148
INTEL					
2114	1024 x 4 SRAM	200-450	18	+5 V	MCM2114
2114L	1024 x 4 SRAM	200-450	18	+5 V	MCM21L14
2115A	1024 x 1 SRAM	45-70	16	+5 V	MCM2115A
2115AL	1024 x 1 SRAM	45-70	16	+5 V	MCM21L15A
2115H	1024 x 1 SRAM	20-35	16	+5 V	MCM2115H
2117	16,384 x 1 DRAM	150-300	16	+12, ±5 V	MCM4116
2118	16,384 x 1 DRAM	100-200	16	+5 V	MCM4517
2125A	1024 x 1 SRAM	45-70	16	+5 V	MCM2125A
2125AL	1024 x 1 SRAM	45-70	16	+5 V	MCM21L25A
2125H	1024 x 1 SRAM	20-35	16	+5 V	MCM2125H
2147	4096 x 1 SRAM	55-100	18	+5 V	MCM2147
2147H	4096 x 1 SRAM	35-55	18	+5 V	MCM2147H
2148	1024 x 4 SRAM	70-85	18	+5 V	MCM2148
2148H	1024 x 4 SRAM	45-55	18	+5 V	MCM2148H
2149H	1024 x 4 SRAM	45-55	18	+5 V	MCM2149H
2308	1024 x 8 SROM	350	24	+5 V	MCM68A308
2316A	2048 x 8 SROM	350	24	+5 V	MCM68A316A
2316E	2048 x 8 SROM	350	24	+5 V	MCM68A316E
2332	4096 x 8 SROM	350	24	+5 V	MCM68A332
2708	1024 x 8 EPROM	450	24	+12, ±5 V	MCM2708
2708-1	1024 x 8 EPROM	350	24	+12, ±5 V	MCM27A08
2716	2048 x 8 EPROM	450	24	+5 V	MCM2716
2716-1	2048 x 8 EPROM	350	24	+5 V	MCM27A16
2816	2048 x 8 EEPROM	350	24	+5 V	MCM2816
INTERSIL					
2114 (IM2114)	1024 x 4 SRAM	200-450	18	+5 V	MCM2114
IM2147	4096 x 1 SRAM	55-85	18	+5 V	MCM2147
MK4027	4096 x 1 DRAM	150-250	16	+12, ±5 V	MCM4027A
IM6508	1024 x 1 SRAM	300-460	16	+5 V	MCM6508
IM6518	1024 x 1 SRAM	300-460	18	+5 V	MCM6518
IM7027	4096 x 1 DRAM	120-250	6	+12, ±5 V	MCM4027A
IM2114L	1024 x 4 SRAM	200-450	18	+5 V	MCM21L14
IM4116	16,384 x 1 DRAM	150-300	16	+12, ±5 V	MCM4116
IM7141	4096 x 1 SRAM	200-450	18	+5 V	MCM6641
IM7141L	4096 x 1 SRAM	200-450	18	+5 V	MCM66L41
ITT					
ITT4027	4096 x 1 DRAM	120-250	16	+12, ±5 V	MCM4027A
ITT4116	16,384 x 1 DRAM	150-300	16	+12, ±5 V	MCM4116

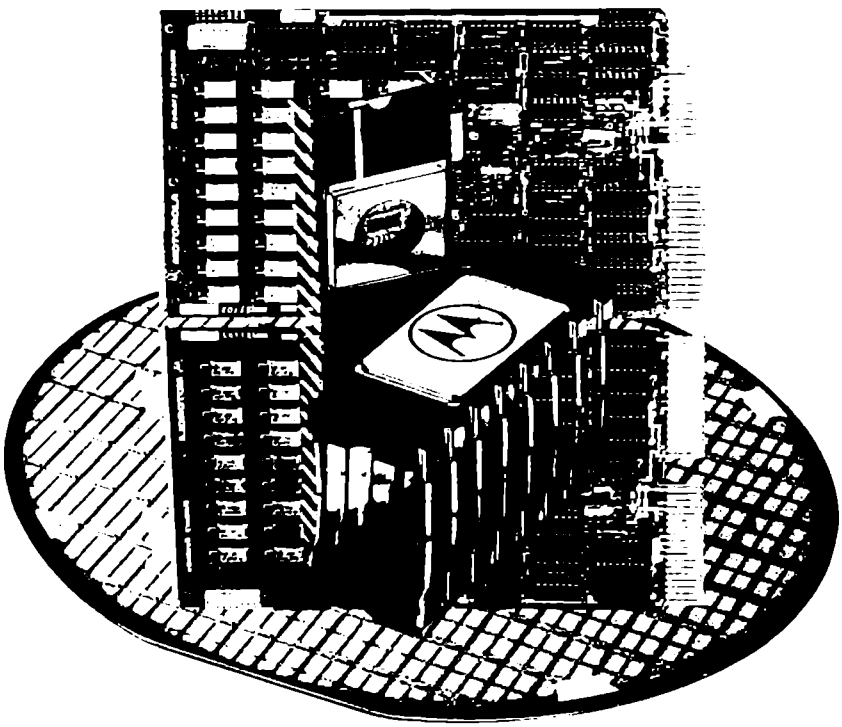
Part Number	Organization Description	Motorola's Access Time (ns Max)	Number of Pins	Power Supplies	Motorola Pin-to-Pin Replacement
MIC					
MIC2316E	2048 x 8 SROM	350	24	+5 V	MCM68A316E
MIC2332	4096 x 8 SROM	350	24	+5 V	MCM68A332
MOSTEK					
MK2147	4096 x 1 SRAM	70-100	18	+5 V	MCM2147
MK2716	2048 x 8 EPROM	450	24	+5 V	MCM2716
MK4027	4096 x 1 DRAM	150-250	16	+12, ±5 V	MCM4027A
MK4116	16,384 x 1 DRAM	150-300	16	+12, ±5 V	MCM4116
MK4516	16,384 x 1 DRAM	120-200	16	+5 V	MCM4516
MK4164	65,536 x 1 DRAM	150-250	16	+5 V	MCM6664
MK30000	1024 x 8 SROM	350	24	+5 V	MCM68A308
MK31000	2048 x 8 SROM	350	24	+5 V	MCM68A316A
MK32000	4096 x 8 SROM	350	24	+5 V	MCM68A332
MK34000	2048 x 8 SROM	350	24	+5 V	MCM68A316E
MK36000	8192 x 8 SROM	350	24	+5 V	MCM68A364
MK36000-4	8192 x 8 SROM	250	24	+5 V	MCM68B364
NATIONAL					
MM2114	1024 x 4 SRAM	200-450	18	+5 V	MCM2114
MM2147	4096 x 1 SRAM	55-85	18	+5 V	MCM2147
MM2708	1024 x 8 EPROM	450	24	+12, ±5 V	MCM2708
MM2716	2048 x 8 EPROM	450	24	+5 V	MCM2716
MM5235	8192 x 8 SROM	350	24	+5 V	MCM68A364
MM5257	4096 x 1 SRAM	200-450	18	+5 V	MCM6641
MM5257L	4096 x 1 SRAM	200-450	18	+5 V	MCM66L41
MM5290	16,384 x 1 DRAM	150-300	16	+12, ±5 V	MCM4116
NEC/EA					
μPD414A	4096 x 1 DRAM	150-250	16	+12, ±5 V	MCM4027A
μPD416	16,384 x 1 DRAM	150-300	16	+12, ±5 V	MCM4116A
μPD2114L	1024 x 4 SRAM	200-450	18	+5 V	MCM21L14
μPD2147	4096 x 1 SRAM	55-85	18	+5 V	MCM2147
μPD2332	4096 x 8 ROM	350	24	+5 V	MCM68A332
μPD2716	2048 x 8 EPROM	450	24	+5 V	MCM2716
μPD4104	4096 x 1 SRAM	200-450	18	+5 V	MCM66L41
μPD5101	256 x 4 SRAM	450-800	22	+5 V	MCM5101
μPD6508	1024 x 1 SRAM	300-460	16	+5 V	MCM6508
EA2114	1024 x 4 SRAM	200-450	18	+5 V	MCM2114
EA2308/8308 μPD or	1024 x 8 SROM	350	24	+5 V	MCM68A308
EA2316A/8316A μPD or	2048 x 8 SROM	350	24	+5 V	MCM68A316A
EA2316E/8316E	2048 x 8 SROM	350	24	+5 V	MCM68A316E
EA2708	1024 x 8 EPROM	450	24	+12, ±5 V	MCM2708
μPD or EA2716	2048 x 8 EPROM	450	24	+5 V	MCM2716
EA8332	4096 x 8 SROM	350	24	+5 V	MCM68A332
NITRON					
NC6570	128 x (7 x 9) SROM	350	24	+5 V	MCM66700
NC6571	128 x (7 x 9) SROM	350	24	+5 V	MCM66710
NC6572	128 x (7 x 9) SROM	350	24	+5 V	MCM66720
NC6573	128 x (7 x 9) SROM	350	24	+5 V	MCM66730
NC6574	128 x (7 x 9) SROM	350	24	+5 V	MCM66740
NC6575	128 x (7 x 9) SROM	350	24	+5 V	MCM66750
SIGNETICS					
2607	1024 x 8 SROM	350	24	+5 V	MCM68A308
2608	1024 x 8 SROM	350	24	+5 V	MCM68A30A
2609	128 x (7 x 9) SROM	350	24	+5 V	MCM66700
2660	4096 x 1 DRAM	120-250	16	+12, ±5 V	MCM4027A
2814	1024 x 4 SRAM	200-450	18	+5 V	MCM21L14
2616	2048 x 8 SROM	350	24	+5 V	MCM68A316E
2633	4096 x 8 SROM	350	24	+5 V	MCM68A332
2664	8192 x 8 SROM	350	24	+5 V	MCM68A364
2690	16,384 x 1 DRAM	250-350	16	+12, ±5 V	MCM4116
2708	1024 x 8 EPROM	450	24	+12, ±5 V	MCM2708
2716	2048 x 8 EPROM	450	24	+5 V	MCM2716
4027	4096 x 1 DRAM	150-250	16	+12, ±5 V	MCM4027A
5101	256 x 4 SRAM	450-800	22	+5 V	MCM5101

Part Number	Organization Description	Motorola's Access Time (ns Max)	Number of Pins	Power Supplies	Motorola Pin-to-Pin Replacement
SYNERTEK					
SY2114	1024 x 4 SRAM	200-450	18	+5 V	MCM21L14
SY2147	4096 x 1 SRAM	55-85	18	+5 V	MCM2147
SY2316A	2048 x 8 SROM	350	24	+5 V	MCM68A316A
SY2316B	2048 x 8 SROM	350	24	+5 V	MCM68A316E
SY2332	4096 x 8 ROM	350	24	+5 V	MCM68A332
SY2716	2048 x 8 EPROM	450	24	+5 V	MCM2716
SY5101	256 x 4 SRAM	450-800	22	+5 V	MCM5101
TEXAS INSTRUMENTS					
TMS2114	1024 x 4 SRAM	200-450	18	+5 V	MCM2114
TMS2147	4096 x 1 SRAM	55-85	18	+5 V	MCM2147
TMS2516	2048 x 8 EPROM	450	24	+5 V	MCM2716
TMS2532	4096 x 8 EPROM	350-450	24	+5 V	MCM2532
TMS2708	1024 x 8 EPROM	450	24	+12, ±5 V	MCM2708
TMS2716	2048 x 8 EPROM	450	24	+12, ±5 V	TMS2716
TMS4016	2048 x 8 SRAM	200	24	+5 V	MCM4016
TMS4044	4096 x 1 SRAM	200-450	18	+5 V	MCM6641
TMS4116	16,384 x 1 DRAM	150-300	16	+12, ±5 V	MCM4116
TMS4164	65,536 x 1 DRAM	150-250	16	+5 V	MCM6665
TMS4732	4096 x 8 SROM	350	24	+5 V	MCM68A332
TMS4764	8192 x 8 SROM	350	24	+5 V	MCM68365
TOSHIBA					
TMM314	1024 x 4 SRAM	200-450	18	+5 V	MCM2114
TMM2147	4096 x 1 SRAM	55-85	18	+5 V	MCM2147
TC5516P	2048 x 8 SRAM	200	24	+5 V	MCM4016

Part Number Guide



MOS Memories
RAM, EPROM, EEPROM, ROM



MOTOROLA

MCM4027A

4096-BIT DYNAMIC RANDOM ACCESS MEMORY

The MCM4027A is a 4096 x 1 bit high-speed dynamic Random Access Memory. It has smaller die size than the MCM4027 providing improved speed selections. The MCM4027A is fabricated using Motorola's highly reliable N-channel silicon-gate technology.

By multiplexing row and column address inputs, the MCM4027A requires only six address lines and permits packaging in Motorola's standard 16-pin dual-in-line packages. Complete address decoding is done on chip with address latches incorporated.

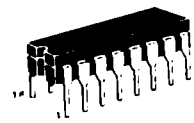
All inputs are TTL compatible, and the output is 3-state TTL compatible. The MCM4027A incorporates a one-transistor cell design and dynamic storage techniques, with each of the 64 row addresses requiring a refresh cycle every 2.0 milliseconds.

- Maximum Access Time = 120 ns – MCM4027AC1
  150 ns – MCM4027AC2
  200 ns – MCM4027AC3
  250 ns – MCM4027AC4
- Maximum Read and Write Cycle Time =
  320 ns – MCM4027AC1, C2
  375 ns – MCM4027AC3, C4
- Low Power Dissipation – 470 mW Max (Active)
  27 mW Max (Standby)
- 3-State Output for OR-Ties
- On-Chip Latches for Address, Chip Select, and Data In
- Power Supply Pins on Package Corners for Optimum Layout
- Industry Standard 16-Pin Package
- Page-Mode Capability
- Compatible with the Popular 2104/MK4096/MCM6604
- Second Source for MK4027

MOS

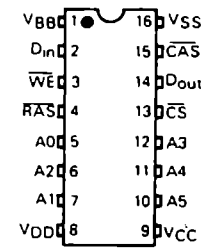
(N-CHANNEL, SILICON-GATE)

4096-BIT DYNAMIC RANDOM ACCESS MEMORY



C SUFFIX
FRIT-SEAL CERAMIC PACKAGE
CASE 620-06

PIN ASSIGNMENT

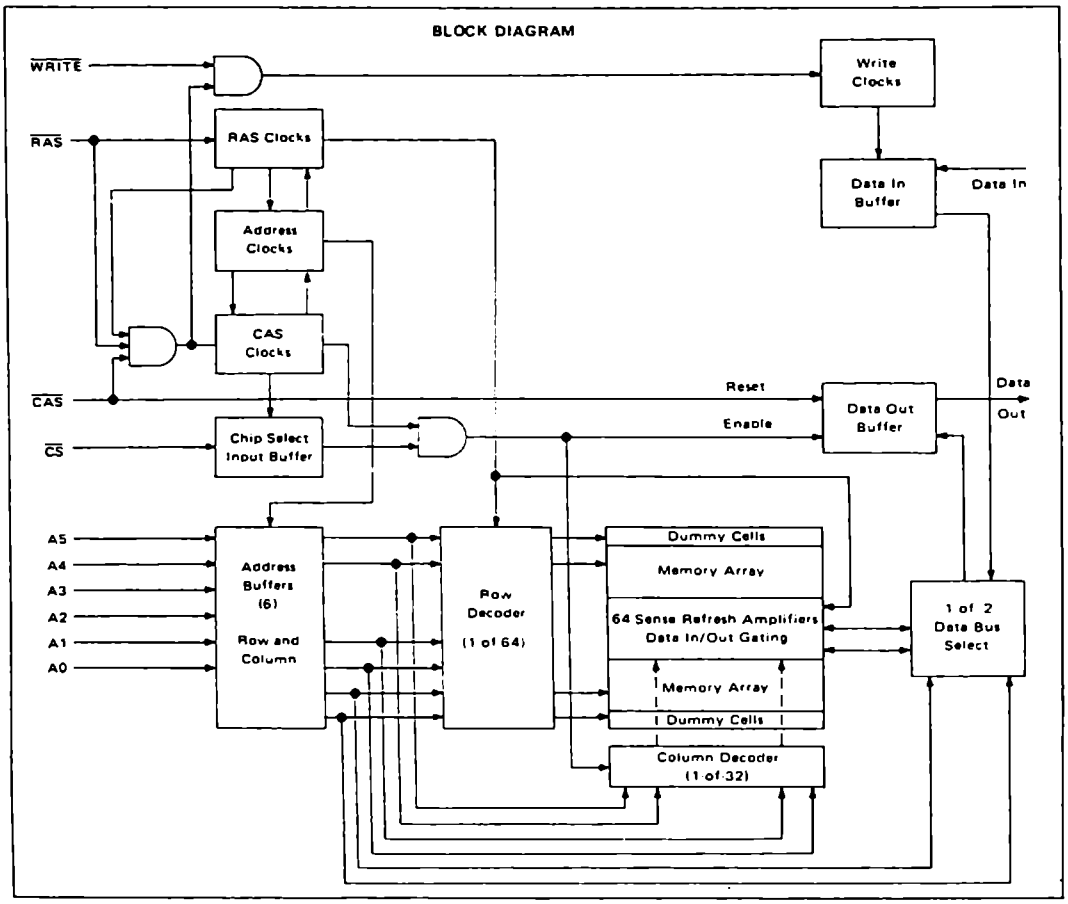


TRUTH TABLE

Inputs				Data Out			Cycle Power	Ref	Function
RAS	CAS	CS	WE	Previous	Interim	Present			
L	L	L	L	Valid data	High Imp.	Input data	Full-operating	Yes	Write cycle
L	L	L	H	Valid data	High Imp.	Valid data (cell)	Full-operating	Yes	Read cycle
L	L	H	X	Valid data	High Imp.	High Imp.	Full-operating	Yes	Deselected-refresh
L	H	X	X	Valid data	Valid data	Valid data	Reduced operating	Yes	RAS only-refresh
H	L	X	X	Valid data	High Imp.	High Imp.	Standby	No	Standby-output disabled
H	H	X	X	Valid data	Valid data	Valid data	Standby	No	Standby-output valid

H = High, L = Low, X = Don't Care

DS9464R1/11-78



OPERATING CHARACTERISTICS

ADDRESSING

The MCM4027A has six address inputs (A0–A5) and two clock signals designated Row Address Strobe ($\overline{RAS}$) and Column Address Strobe ($\overline{CAS}$). At the beginning of a memory cycle, the six low order address bits A0 through A5 are strobed into the chip with $\overline{RAS}$ to select one of the 64 rows. The row address strobe also initiates the timing that will enable the 64 column sense amplifiers. After a specified hold time, the row address is removed and the six high order address bits (A6–A11) are placed on the address pins. This address is then strobed into the chip with $\overline{CAS}$. Two of the 64 column sense amplifiers are selected by A1 through A5. A one of two data bus select is accomplished by A0 to complete the data selection. The Chip Select ($\overline{CS}$) is latched into the port along with the column addresses.

DATA OUTPUT

In order to simplify the memory system designed and reduce the total package count, the MCM4027A contains an input data latch and a buffered output data latch. The state of the output latch and buffer at the end of a memory cycle will depend on the type of memory cycle performed and whether the chip is selected or unselected for that memory cycle.

A chip will be unselected during a memory cycle if:

(1) The chip receives both $\overline{RAS}$ and $\overline{CAS}$ signals, but no $\overline{Chip\ Select}$ signal.

(2) The chip receives a $\overline{CAS}$ signal but no $\overline{RAS}$ signal. With this condition, the chip will be unselected regardless of the state of $\overline{Chip\ Select}$ input.

If, during a read, write, or read-modify-write cycle,

the chip is unselected, the output buffer will be in the high impedance state at the end of the memory cycle. The output buffer will remain in the high impedance state until the chip is selected for a memory cycle.

For a chip to be selected during a memory cycle, it must receive the following signals: $\overline{RAS}$, $\overline{CAS}$, and $\overline{Chip\ Select}$. The state of the output latch and buffer of a selected chip during the following type of memory cycles would be:

(1) Read Cycle – On the negative edge of $\overline{CAS}$, the output buffer will unconditionally go to a high impedance state. It will remain in this state until access time. At this time, the output latch and buffer will assume the logic state of the data read from the selected cell. This output state will be maintained until the chip receives the next $\overline{CAS}$ signal.

(2) Write Cycle – If the $\overline{WE}$ input is switched to a logic 0 before the $\overline{CAS}$ transition, the output latch and buffer will be switched to the state of the data input at the end of the access time. This logic state will be maintained until the chip receives the next $\overline{CAS}$ signal.

(3) Read-Modify-Write – Same as read cycle.

DATA INPUT

Data to be written into a selected storage cell of the memory chip is first stored in the on-chip data latch. The gating of this latch is performed with a combination of the $\overline{WE}$ and $\overline{CAS}$ signals. The last of these signals to make a negative transition will strobe the data into the latch. If the $\overline{WE}$ input is switching to a logic 0 in the beginning of a write cycle, the falling edge of $\overline{CAS}$ strobes the data into the latch. The data setup and hold times are then referenced to the negative edge of $\overline{CAS}$.

If a read-modify-write cycle is being performed, the $\overline{WE}$ input would not make its negative transistion until after the $\overline{CAS}$ signal was enabled. Thus, the data would not be strobed into the latch until the negative transistion of $\overline{WE}$. The data setup and hold times would now be referenced to the negative edge of the $\overline{WE}$ signal. The only other timing constraints for a write-type-cycle is that both the $\overline{CAS}$ and $\overline{WE}$ signals remain in the logic 0 state for a sufficient time to accomplish the permanent storage of the data into the selected cell.

INPUT/OUTPUT LEVELS

All of the inputs to the MCM4027A are TTL-compatible, featuring high impedance and low capacitance (5 to 7 pF). The three state data output buffer is TTL-compatible and has sufficient current sink capability (3.2 mA) to drive two TTL loads. The output buffer also has a separate V_{CC} pin so that it can be powered from the same supply as the logic being employed.

REFRESH

In order to maintain valid data, each of the 64 internal rows of the MCM4027A must be refreshed once every 2 ms. Any cycle in which a $\overline{RAS}$ signal occurs accomplishes a refresh operation. Any read, write, or read-modify-write cycle will refresh an entire internally selected row. However, if a write or read-modify-write cycle is used to perform a refresh cycle the chip must be deselected to prevent writing data into the selected cell. The memory can also be refreshed by employing only the $\overline{RAS}$ cycle. This refresh mode will not shorten the refresh cycle time, however, the system standby power can be reduced by approximately 30%.

If the $\overline{RAS}$ only refresh cycles are employed for an extended length of time, the output buffer may eventually lose data and assume the high impedance state. Applying $\overline{CAS}$ to the chip will restore activity of the output buffer.

POWER DISSIPATION

Since the MCM4027A is a dynamic RAM, its power drain will be extremely small during the time the chip is unselected.

The power increases when the chip is selected and most of this increase is encountered on the address strobe edge. The circuitry of the MCM4027A is largely dynamic so power is not drawn during the whole time the strobe is active. Thus the dynamic power is a function of the operating frequency rather than the active duty cycle.

In a memory system, the $\overline{CAS}$ signal must be supplied to all the memory chips to ensure that the outputs of the unselected chips are switched to the high impedance state. Those chips that do not receive a $\overline{RAS}$ signal will not dissipate any power on the $\overline{CAS}$ edge except for that required to turn off the chip outputs. Thus, in order to ensure minimum system power, the $\overline{RAS}$ signal should be decoded so that only the chips to be selected receive a $\overline{RAS}$ signal. If the $\overline{RAS}$ signal is decoded, then the chip select input of all the chips can be set to a logic 0 state.

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DC OPERATING CONDITIONS AND CHARACTERISTICS
(Full operating voltage and temperature range unless otherwise noted.)

RECOMMENDED OPERATING CONDITIONS (Referenced to V_{SS} = Ground.)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply Voltage	V_{DD}	10.8	12.0	13.2	Vdc	2
	V_{CC}	V_{SS}	5.0	V_{DD}	Vdc	3
	V_{SS}	0	0	0	Vdc	2
	V_{BB}	-4.5	-5.0	-5.5	Vdc	2
Logic 1 Voltage, $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	V_{IHC}	2.4	5.0	7.0	Vdc	2, 4
Logic 1 Voltage, all inputs except $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	V_{IH}	2.2	5.0	7.0	Vdc	2, 4
Logic 0 Voltage, all inputs	V_{IL}	-1.0	0	0.8	Vdc	2, 4

DC CHARACTERISTICS (V_{DD} = 12 V ± 10%, V_{CC} = 5.0 V ± 10%, V_{BB} = -5.0 V ± 10%, V_{SS} = 0 V, T_A = 0 to 70°C.) Notes 1, 5

Characteristic	Symbol	Min	Typ	Max	Units	Notes
Average V_{DD} Power Supply Current	I_{DD1}			35	mA	6
V_{CC} Power Supply Current	I_{CC}				mA	7
Average V_{BB} Power Supply Current	I_{BB}			250	µA	
Standby V_{DD} Power Supply Current	I_{DD2}			2	mA	9
Average V_{DD} Power Supply Current during "$\overline{RAS}$ only" cycles	I_{DD3}			25	mA	6
Input Leakage Current (any input)	$I_{I(L)}$			10	µA	8
Output Leakage Current	$I_{O(L)}$			10	µA	9, 10
Output Logic 1 Voltage @ I_{out} = -5 mA	V_{OH}	2.4			Vdc	
Output Logic 0 Voltage @ I_{out} = 3.2 mA	V_{OL}			0.4	Vdc	

NOTES 1 through 11:

1. T_A is specified for operation at frequencies to $t_{RC} \geq t_{RC}(min)$. Operation at higher cycle rates with reduced ambient temperatures and higher power dissipation is permissible provided that all ac parameters are met.
2. All voltages referenced to V_{SS}.
3. Output voltage will swing from V_{SS} to V_{CC} when enabled, with no output load. For purposes of maintaining data in standby mode, V_{CC} may be reduced to V_{SS} without affecting refresh operations or data retention. However, the $V_{OH}(min)$ specification is not guaranteed in this mode.
4. Device speed is not guaranteed at input voltages greater than TTL levels (0 to 5 v).
5. Several cycles are required after power-up before proper device operation is achieved. Any 8 cycles which perform refresh are adequate for this purpose.
6. Current is proportional to cycle rate. $I_{DD1}(max)$ is measured at the cycle rate specified by $t_{RC}(min)$.
7. I_{CC} depends on output loading. During readout of high level data V_{CC} is connected through a low impedance (135 Ω typ) to Data Out. At all other times I_{CC} consists of leakage currents only.
8. All device pins at 0 volts except V_{BB} which is at -5 volts and the pin under test which is at +10 volts.
9. Output is disabled (high-impedance) and $\overline{RAS}$ and $\overline{CAS}$ are both at a logic 1. Transient stabilization is required prior to measurement of this parameter.
10. $0 V \leq V_{Out} \leq +10 V$.
11. Effective capacitance is calculated from the equation:

$$C = \frac{\Delta Q}{\Delta V} \text{ with } \Delta V = 3 \text{ volts.}$$

EFFECTIVE CAPACITANCE (Full operating voltage and temperature range, periodically sampled rather than 100% tested) Note 11

Characteristic		Symbol	Max	Unit
Input Capacitance	(A0-A5), D_{in}, $\overline{CS}$	$C_{in(EFF)}$	5.0	pF
	$\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$		10.0	
Output Capacitance		$C_{out(EFF)}$	7.0	pF

ABSOLUTE MAXIMUM RATINGS (See Notes 1 and 2)

Rating	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{BB}*	V_{in}, V_{out}	-0.5 to +20	Vdc
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C
Output Current (Short Circuit)	I_{out}	50	mAdc

* ($V_{SS} - V_{BB} > 4.5$ V)

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS ARE EXCEEDED. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability. V_{BB} must be applied prior to V_{CC} and V_{DD}. V_{BB} must also be the last power supply switched off.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

AC OPERATING CONDITIONS AND CHARACTERISTICS
(Read, Write, and Read-Modify-Write Cycles)

RECOMMENDED AC OPERATING CONDITIONS (V_{DD} 12 V ± 10%, V_{CC} = 5.0 V ± 10%, V_{BB} = -5.0 V ± 10%, V_{SS} 0 V, T_A 0 to 70°C) Notes 1, 5, 12, 18

Parameter	Symbol	MCM4027AC1		MCM4027AC2		MCM4027AC3		MCM4027AC4		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RC}	320		320		375		375		ns	13
Read Write Cycle Time	t_{RWC}	320		320		375		375		ns	13
Page Mode Cycle Time	t_{PC}	160		170		225		285		ns	13
Access Time From Row Address Strobe	t_{RAC}		120		150		200		250	ns	14, 16
Access Time From Column Address Strobe	t_{CAC}		80		100		135		165	ns	15, 16
Output Buffer and Turn-Off Delay	t_{OFF}		35		40		50		60	ns	
Row Address Strobe Precharge Time	t_{RP}	100		100		120		120		ns	
Row Address Strobe Pulse Width	t_{RAS}	120	10,000	150	10,000	200	10,000	250	10,000	ns	
Row Address Strobe Hold Time	t_{RSH}	80		100		135		165		ns	
Column Address Strobe Pulse Width	t_{CAS}	80		100		135		165		ns	
Column Address Strobe Hold Time	t_{CSH}	120		150		200		250		ns	
Row to Column Strobe Lead Time	t_{RCD}	15	40	20	50	25	65	35	85	ns	17
Row Address Setup Time	t_{ASR}	0		0		0		0		ns	
Row Address Hold Time	t_{RAH}	15		20		25		35		ns	
Column Address Setup Time	t_{ASC}	-5		10		10		10		ns	
Column Address Hold Time	t_{CAH}	40		45		55		75		ns	
Column Address Hold Time Referenced to $\overline{RAS}$	t_{AR}	80		95		120		160		ns	
Chip Select Setup Time	t_{CSC}	0		10		10		10		ns	
Chip Select Hold Time	t_{CH}	40		45		55		75		ns	
Chip Select Hold Time Referenced to $\overline{RAS}$	t_{CHR}	80		95		120		160		ns	
Transition Time Rise and Fall	t_T	3	35	3	35	3	50	3	50	ns	18
Read Command Setup Time	t_{RCS}	0		0		0		0		ns	
Read Command Hold Time	t_{RCH}	0		0		0		0		ns	
Write Command Hold Time	t_{WCH}	40		45		55		75		ns	
Write Command Hold Time Referenced to $\overline{RAS}$	t_{WCR}	80		95		120		160		ns	
Write Command Pulse Width	t_{WP}	40		45		55		75		ns	
Write Command to Row Strobe Lead Time	t_{RWL}	50		50		70		85		ns	
Write Command to Column Strobe Lead Time	t_{CWL}	50		50		70		85		ns	
Data in Setup Time	t_{DS}	0		0		0		0		ns	19
Data in Hold Time	t_{DH}	40		45		55		75		ns	19
Data in Hold Time Referenced to $\overline{RAS}$	t_{DHR}	80		95		120		160		ns	
Column to Row Strobe Precharge Time	t_{CRP}	0		0		0		0		ns	
Column Precharge Time	t_{CP}	60		60		80		110		ns	
Refresh Period	t_{RFSH}		2		2		2		2	ms	
Write Command Setup Time	t_{WCS}	0		0		0		0		ns	
$\overline{CAS}$ to $\overline{WRITE}$ Delay	t_{CWD}	60		60		80		90		ns	20
$\overline{RAS}$ to $\overline{WRITE}$ Delay	t_{RWD}	100		110		145		175		ns	20
Data Out Hold Time	t_{DOH}	10		10		10		10		µs	

NOTES 12 through 20:

12. AC measurements assume t_T = 5 ns.

13. The specifications for t_{RC}(min) and t_{RWC}(min) are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.

14. Assumes that $t_{RCD} \leq t_{RCD}$(max)

15. Assumes that $t_{RCD} \geq t_{RCD}$ (max).

16. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.

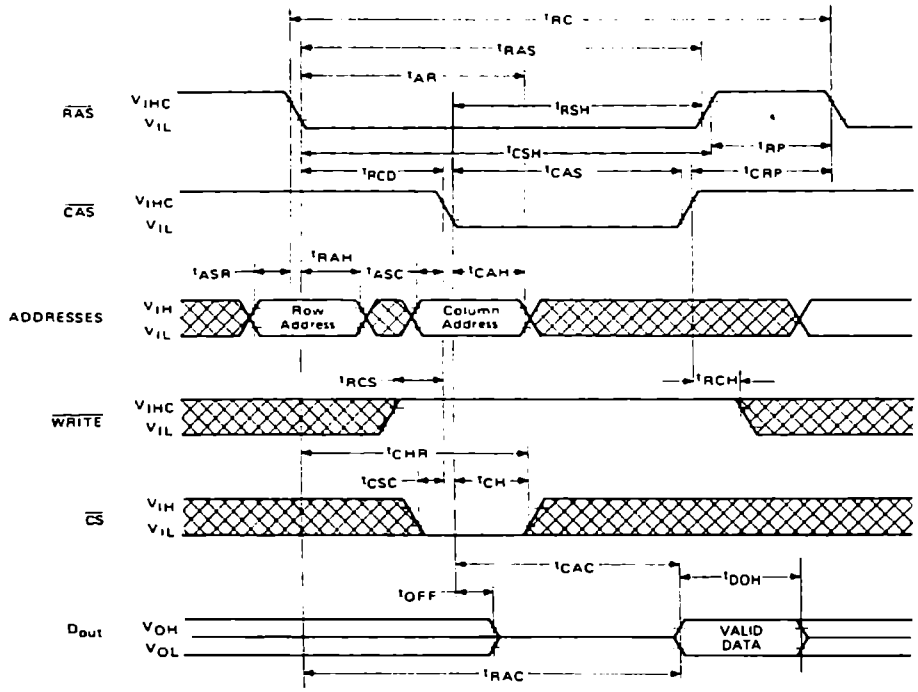
17. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.

18. V_{IHC}(min) or V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IHC} or V_{IH} and V_{IL}.

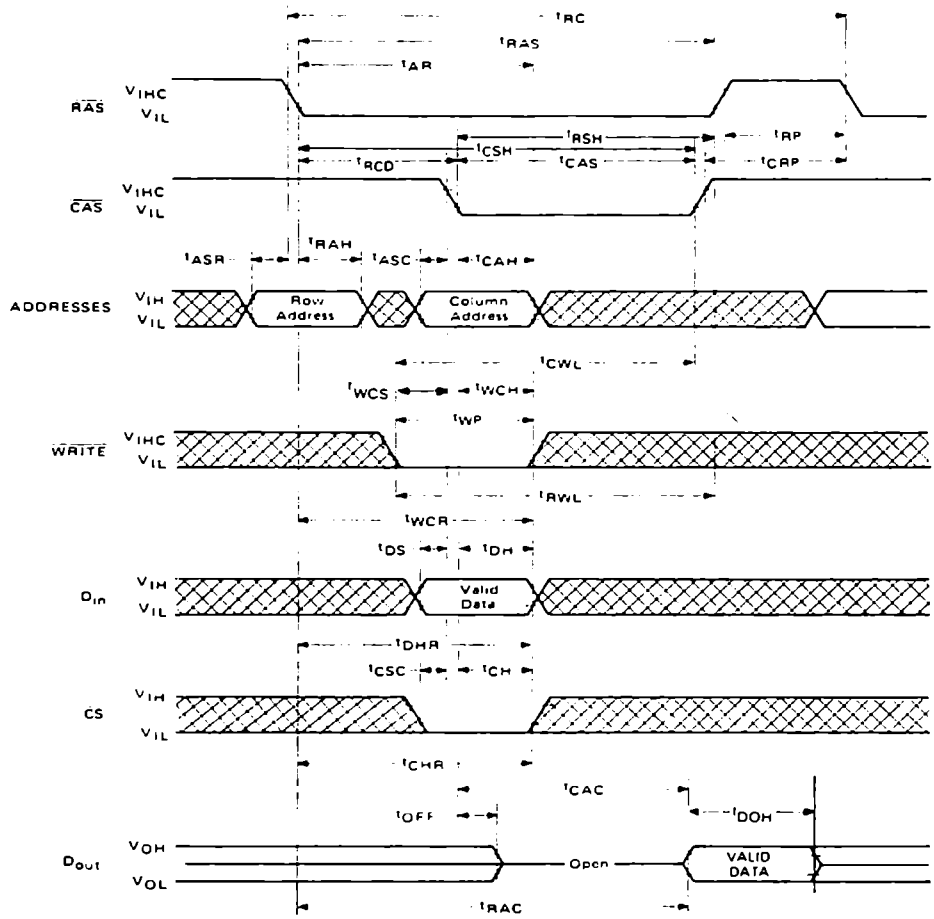
19. These parameters are referenced to $\overline{CAS}$ leading edge in random write cycles and to $\overline{WRITE}$ leading edge in delayed write or read-modify write cycles.

20. t_{WCS}, t_{CWD}, and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: If $t_{WCS} \geq t_{WCS}$(min), the cycle is an early write cycle and Data Out will contain the data written into the selected cell. If $t_{CWD} \geq t_{CWD}$(min) and $t_{RWD} \geq t_{RWD}$(min), the cycle is a read-write cycle and Data Out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of Data Out (at access time) is indeterminate.

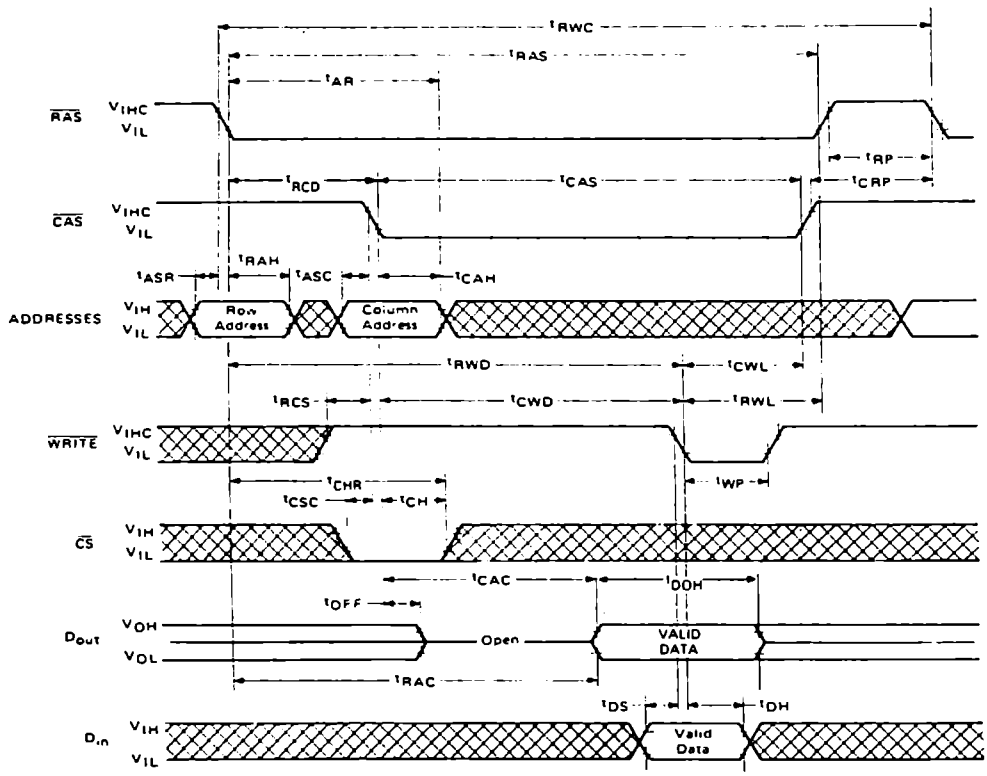
READ CYCLE TIMING



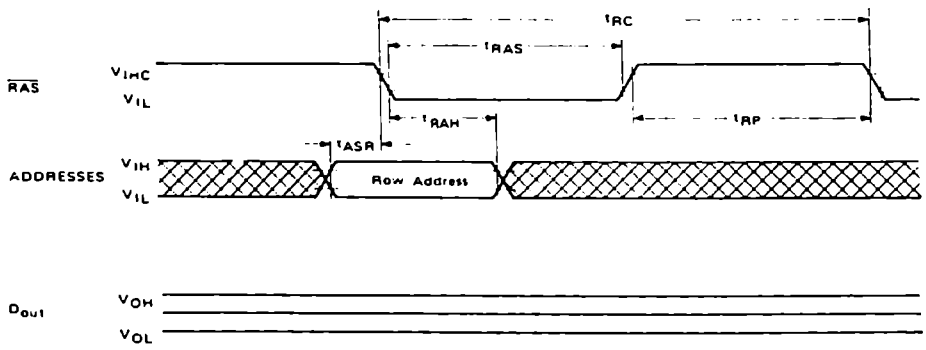
WRITE CYCLE TIMING



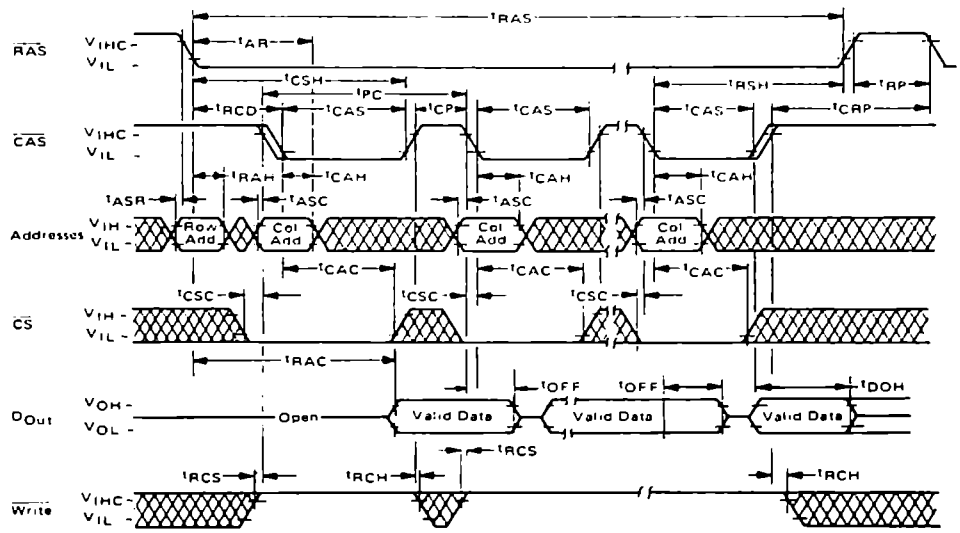
READ-MODIFY-WRITE TIMING



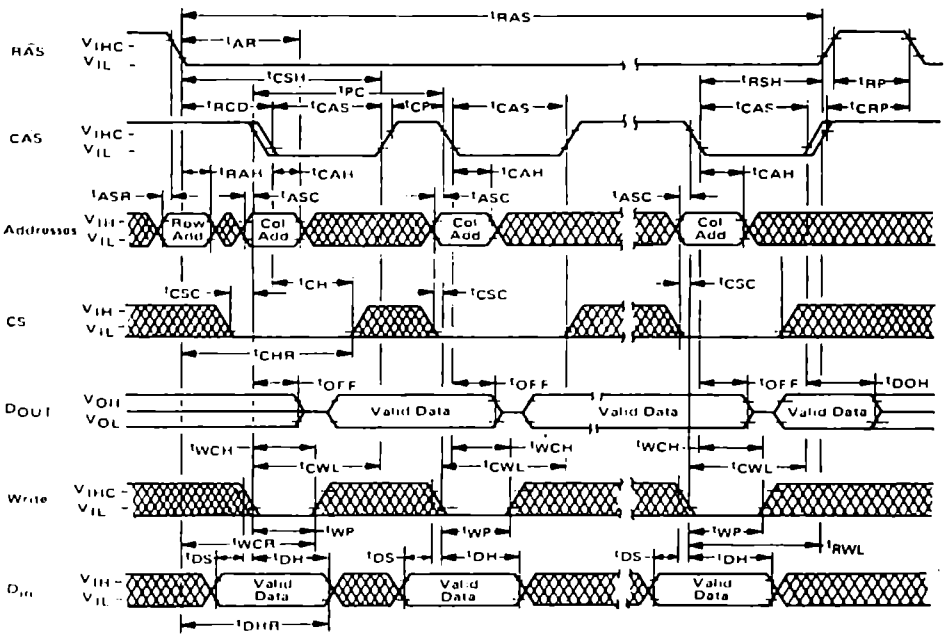
RAS ONLY REFRESH TIMING

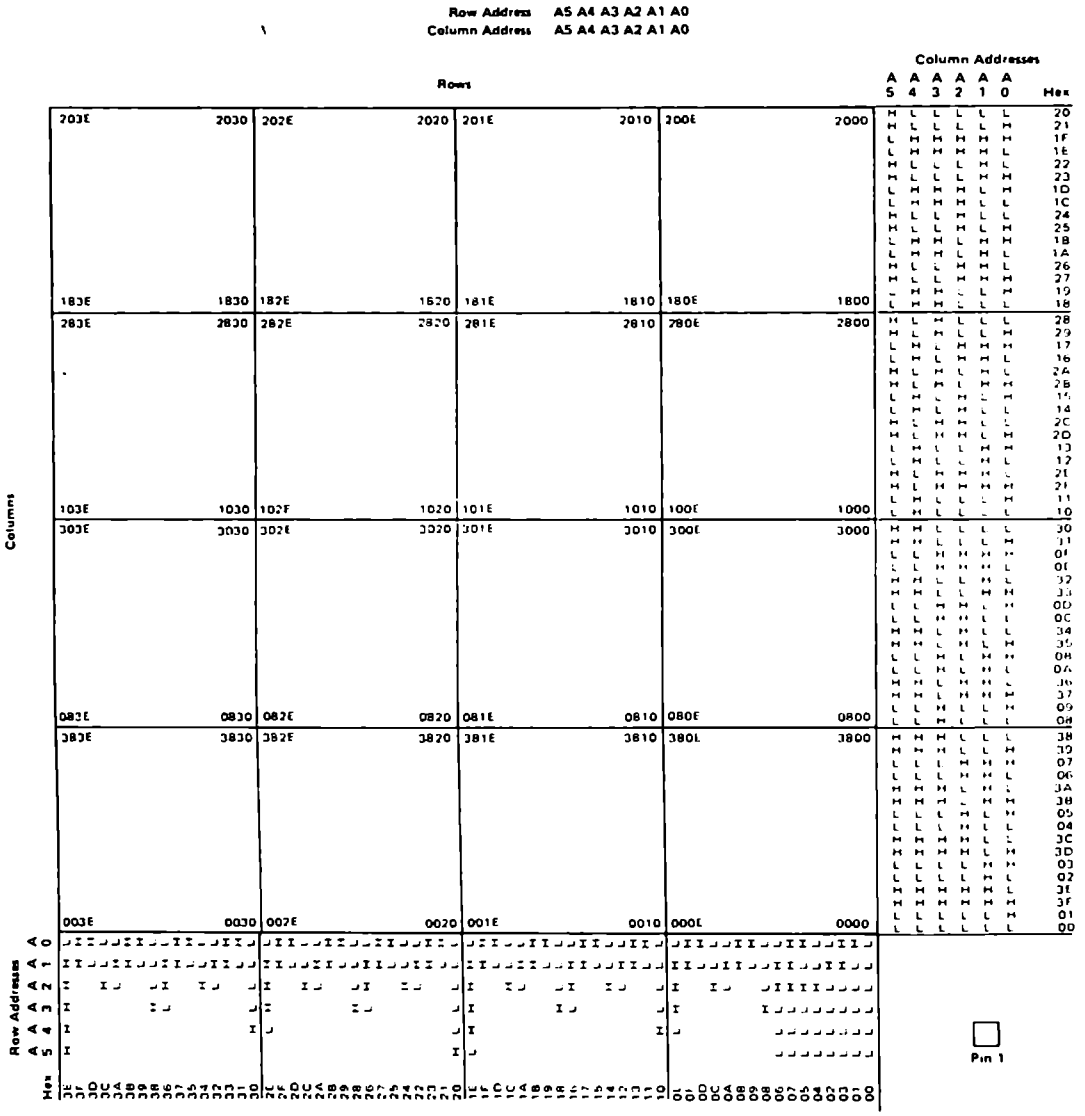


PAGE MODE READ CYCLE



PAGE MODE WRITE CYCLE





MCM4027A BIT ADDRESS MAP

MOTOROLA

MCM4116B

16,384-BIT DYNAMIC RANDOM ACCESS MEMORY

The MCM4116B is a 16,384-bit, high-speed dynamic Random Access Memory designed for high-performance, low-cost applications in mainframe and buffer memories and peripheral storage. Organized as 16,384 one-bit words and fabricated using Motorola's highly reliable N-channel double-polysilicon technology, this device optimizes speed, power, and density tradeoffs.

By multiplexing row and column address inputs, the MCM4116B requires only seven address lines and permits packaging in Motorola's standard 16-pin dual in-line packages. This packaging technique allows high system density and is compatible with widely available automated test and insertion equipment. Complete address decoding is done on chip with address latches incorporated.

All inputs are TTL compatible, and the output is 3-state TTL compatible. The data output of the MCM4116B is controlled by the column address strobe and remains valid from access time until the column address strobe returns to the high state. This output scheme allows higher degrees of system design flexibility such as common input/output operation and two dimensional memory selection by decoding both row address and column address strobes.

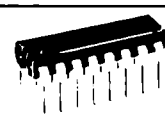
The MCM4116B incorporates a one-transistor cell design and dynamic storage techniques, with each of the 128 row addresses requiring a refresh cycle every 2 milliseconds.

- Flexible Timing with Read-Modify-Write, RAS-Only Refresh, and Page-Mode Capability
- Industry Standard 16-Pin Package
- 16,384 X 1 Organization
- ±10% Tolerance on All Power Supplies
- All Inputs are Fully TTL Compatible
- Three-State Fully TTL-Compatible Output
- Common I/O Capability When Using "Early Write" Mode
- On-Chip Latches for Addresses and Data In
- Low Power Dissipation — 463 mW Active, 20 mW Standby (Max)
- Fast Access Time Options 150 ns — MCM4116BP-15, BC-15
  200 ns — MCM4116BP-20, BC-20
  250 ns — MCM4116BP-25, BC-25
  300 ns — MCM4116BP-30, BC-30
- Easy Upgrade from 16-Pin 4K RAMs

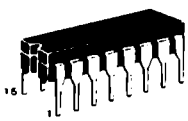
MOS

(N-CHANNEL)

16,384-BIT DYNAMIC RANDOM ACCESS MEMORY

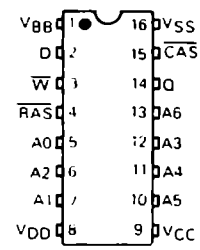


P SUFFIX
PLASTIC PACKAGE
CASE 648



C SUFFIX
FRIT-SEAL CERAMIC PACKAGE
CASE 620

PIN ASSIGNMENT



PIN NAMES	
A0-A6	Address Inputs
CAS	Column Address Strobe
D	Data In
Q	Data Out
RAS	Row Address Strobe
W	Read/Write Input
VBB	Power (−5 V)
VCC	Power (+5 V)
VDD	Power (+12 V)
VSS	Ground

ABSOLUTE MAXIMUM RATINGS (See Note)

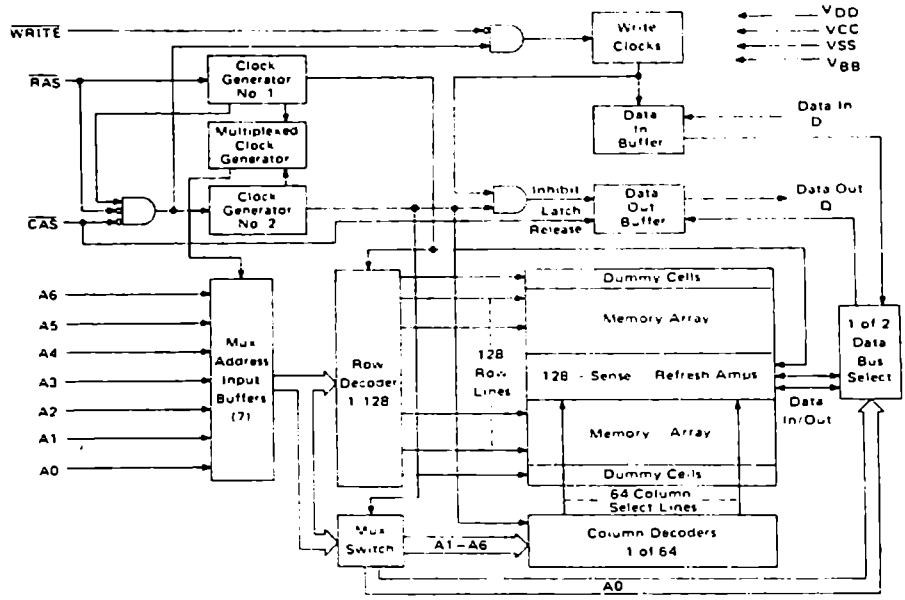
Rating	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{BB}	V_{in}, V_{out}	−0.5 to +20	V
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Power Dissipation	P_D	1.0	W
Data Out Current	I_{out}	50	mA

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

DS9806/10-79

BLOCK DIAGRAM



DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted.)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply Voltage	V_{DD}	10.8	12.0	13.2	V	1
	V_{CC}	4.5	5.0	5.5	V	1, 2
	V_{SS}	0	0	0	V	1
	V_{BB}	-4.5	-5.0	-5.5	V	1
Logic 1 Voltage, $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	V_{IHC}	2.4	–	7.0	V	1
Logic 1 Voltage, all inputs except $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	V_{IH}	2.4	–	7.0	V	1
Logic 0 Voltage, all inputs	V_{IL}	-1.0		0.8	V	1

DC CHARACTERISTICS (V_{DD} 12 V ±10%, V_{CC} 5.0 V ±10%, V_{BB} -5.0 V ±10%, V_{SS} 0 V, T_A 0 to 70°C)

Characteristic	Symbol	Min	Max	Units	Notes
Average V_{DD} Power Supply Current	I_{DD1}	–	35	mA	4
V_{CC} Power Supply Current	I_{CC}	–	–	mA	5
Average V_{BB} Power Supply Current	$I_{BB1,3}$	–	200	µA	
Standby V_{BB} Power Supply Current	I_{BB2}	–	100	µA	
Standby V_{DD} Power Supply Current	I_{DD2}	–	1.5	mA	6
Average V_{DD} Power Supply Current during "RAS only" cycles	I_{DD3}	–	27	mA	4
Input Leakage Current (any input)	$I_{I(L)}$	–	10	µA	
Output Leakage Current	$I_{O(L)}$	–	10	µA	6, 7
Output Logic 1 Voltage @ I_{out} = -5 mA	V_{OH}	2.4	–	V	2
Output Logic 0 Voltage @ I_{out} = 4.2 mA	V_{OL}	–	0.4	V	

NOTES:

1. All voltages referenced to V_{SS}. V_{BB} must be applied before and removed after other supply voltages.
2. Output voltage will swing from V_{SS} to V_{CC} under open circuit conditions. For purposes of maintaining data in power down mode, V_{CC} may be reduced to V_{SS} without affecting refresh operations. V_{OH} (min) specification is not guaranteed in this mode.
3. Several cycles are required after power up before proper device operation is achieved. Any 8 cycles which perform refresh are sufficient.
4. Current is proportional to cycle rate; maximum current is measured at the fastest cycle rate.
5. I_{CC} depends upon output loading. The V_{CC} supply is connected to the output buffer only.
6. Output is disabled (open-circuit) when $\overline{CAS}$ is at a logic 1.
7. $0 V \leq V_{out} \leq +5.5 V$

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, V_{CC} = 5 V, periodically sampled rather than 100% tested) (See Note 8)

Parameter	Symbol	Typ	Max	Unit	Notes
Input Capacitance (A0-A6), D_{in}	C_{I1}	4.0	5.0	pF	9
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	C_{I2}	8.0	10	pF	9
Output Capacitance (D_{out})	C_O	5.0	7.0	pF	7, 9

AC OPERATING CONDITIONS AND CHARACTERISTICS (See Notes 3, 9, 14)

READ, WRITE, AND READ-MODIFY-WRITE CYCLES

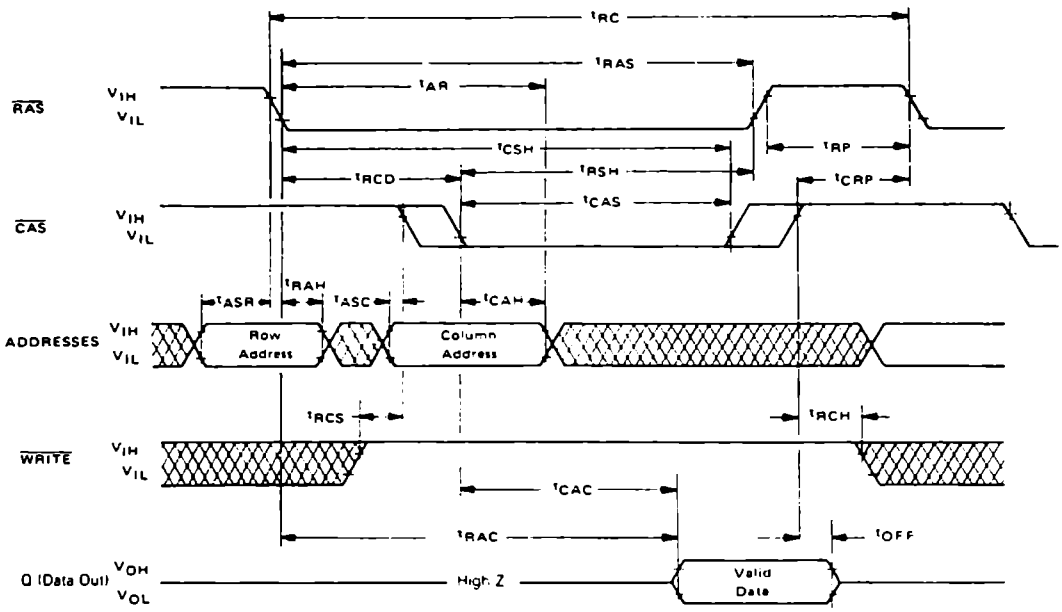
(V_{DD} = 12 V ± 10%, V_{CC} = 5.0 V ± 10%, V_{BB} = -5.0 V ± 10%, V_{SS} = 0 V, T_A = 0 to 70°C)

Parameter	Symbol	MCM4116B-15		MCM4116B-20		MCM4116B-25		MCM4116B-30		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RC}	375	–	375	–	410		480	–	ns	
Read Write Cycle Time	t_{RWC}	375	–	375	–	515	–	660	–	ns	
Access Time from Row Address Strobe	t_{RAC}	–	150	–	200		250	–	300	ns	10, 12
Access Time from Column Address Strobe	t_{CAC}	–	100	–	135	–	165	–	200	ns	11, 12
Output Buffer and Turn-off Delay	t_{OFF}	0	50	0	50	0	60	0	60	ns	17
Row Address Strobe Precharge Time	t_{RP}	100	–	120	–	150	–	180	–	ns	
Row Address Strobe Pulse Width	t_{RAS}	150	10,000	200	10,000	250	10,000	300	10,000	ns	
Column Address Strobe Pulse Width	t_{CAS}	100	10,000	135	10,000	165	10,000	200	10,000	ns	
Row to Column Strobe Lead Time	t_{RCD}	20	50	25	65	35	85	60	100	ns	13
Row Address Setup Time	t_{ASR}	0	–	0	–	0	–	0	–	ns	
Row Address Hold Time	t_{RAH}	20	–	25	–	35	–	60	–	ns	
Column Address Setup Time	t_{ASC}	-10	–	-10	–	-10	–	-10	–	ns	
Column Address Hold Time	t_{CAH}	45	–	55	–	75	–	100	–	ns	
Column Address Hold Time Referenced to $\overline{RAS}$	t_{AR}	95	–	120	–	160	–	200	–	ns	
Transition Time (Rise and Fall)	t_T	3.0	35	3.0	50	3.0	50	3.0	50	ns	14
Read Command Setup Time	t_{RCS}	0	–	0	–	0		0	–	ns	
Read Command Hold Time	t_{RCH}	0	–	0	–	0	–	0	–	ns	
Write Command Hold Time	t_{WCH}	45	–	55	–	75	–	100	–	ns	
Write Command Hold Time Referenced to $\overline{RAS}$	t_{WCR}	95	–	120	–	160	–	200	–	ns	
Write Command Pulse Width	t_{WP}	45	–	55	–	75	–	100	–	ns	
Write Command to Row Strobe Lead Time	t_{RWL}	60	–	80	–	100	–	180	–	ns	
Write Command to Column Strobe Lead Time	t_{CWL}	60		80		100	–	180	–	ns	
Data in Setup Time	t_{DS}	0		0	–	0	–	0	–	ns	15
Data in Hold Time	t_{DH}	45	–	55	–	75	–	100	–	ns	15
Data in Hold Time Referenced to $\overline{RAS}$	t_{DHR}	95	–	120	–	160	–	200	–	ns	
Column to Row Strobe Precharge Time	t_{CRP}	-20		-20	–	-20	–	-20	–	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	100		135	–	165	–	200	–	ns	
Refresh Period	t_{RFSH}	–	2.0	–	2.0	–	2.0	–	2.0	ms	
$\overline{WRITE}$ Command Setup Time	t_{WCS}	-20	–	-20	–	-20	–	-20	–	ns	
$\overline{CAS}$ to $\overline{WRITE}$ Delay	t_{CWD}	70	–	95	–	125	–	180	–	ns	16
$\overline{RAS}$ to $\overline{WRITE}$ Delay	t_{RWD}	120	–	160	–	210	–	280	–	ns	16
$\overline{CAS}$ Precharge Time (Page mode cycle only)	t_{CP}	60	–	80	–	100	–	100	–	ns	
Page Mode Cycle Time	t_{PC}	170	–	225	–	275	–	325	–	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	150	–	200	–	250	–	300	–	ns	

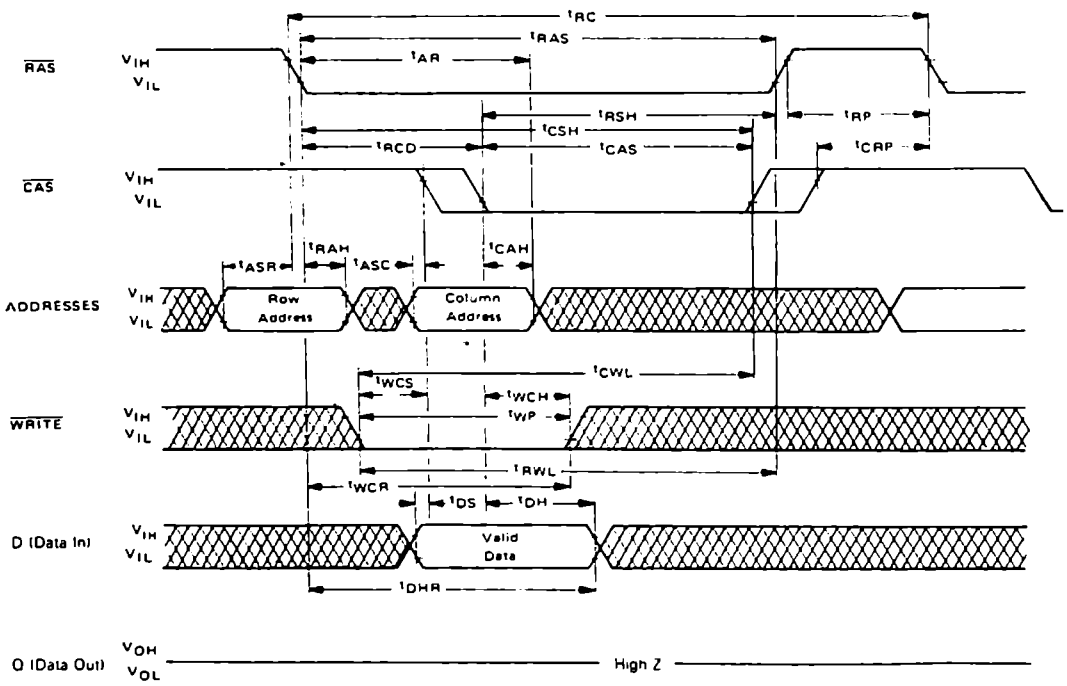
NOTES (continued)

8. Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation $C = \frac{\Delta t}{\Delta V}$
9. AC measurements assume t_T = 5.0 ns.
10. Assumes that $t_{RCD} \leq t_{RCD}$ (max)
11. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
12. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
13. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit then access time is controlled exclusively by t_{CAC}
14. V_{IHC} (min) or V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transistion times are measured between V_{IHC} or V_{IH} and V_{IL}.
15. These parameters are referenced to $\overline{CAS}$ leading edge in random write cycles and to $\overline{WRITE}$ leading edge in delayed write or read-modify-write cycles.
16. t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min), the cycle is a read-write cycle and the data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate
17. Assumes that t_{CRP} = 50 ns

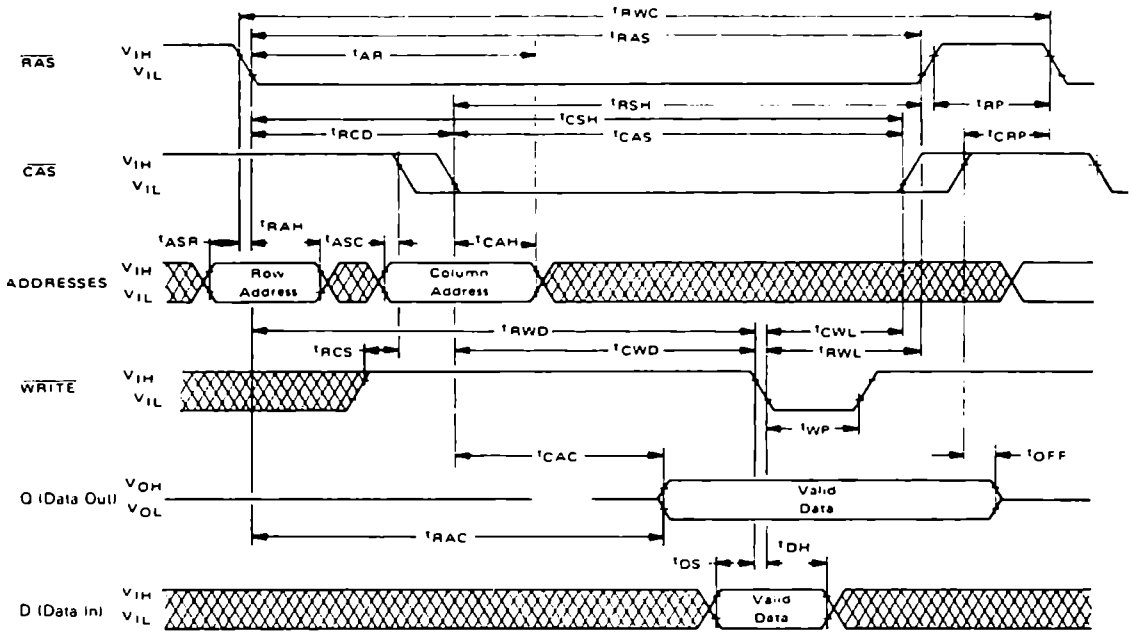
READ CYCLE TIMING



WRITE CYCLE TIMING

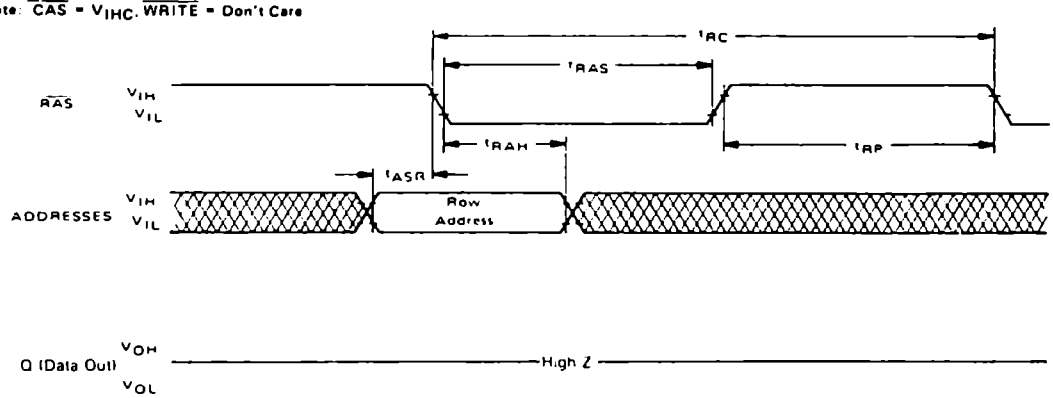


READ-WRITE/READ-MODIFY-WRITE CYCLE

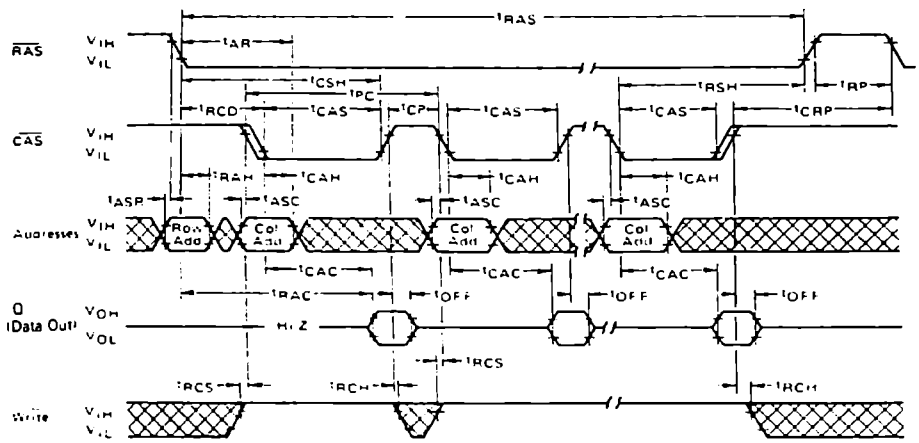


$\overline{RAS}$ ONLY REFRESH TIMING

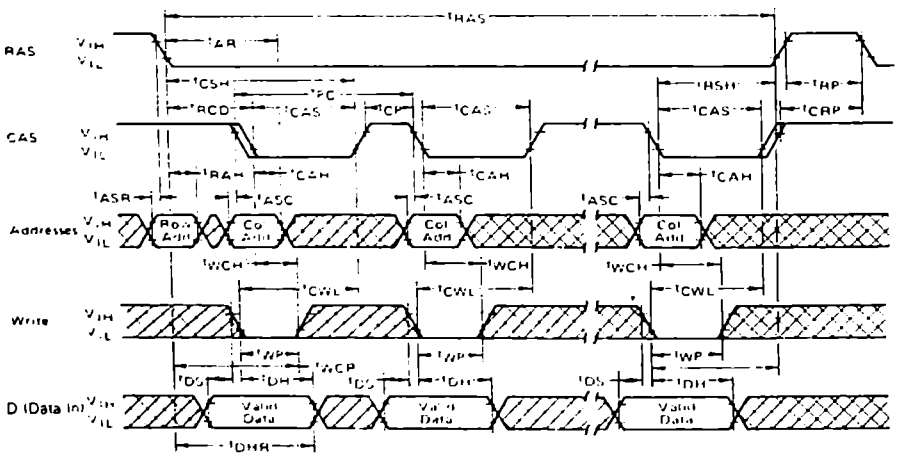
Note: $\overline{CAS}$ = V_{IHC}, $\overline{WRITE}$ = Don't Care



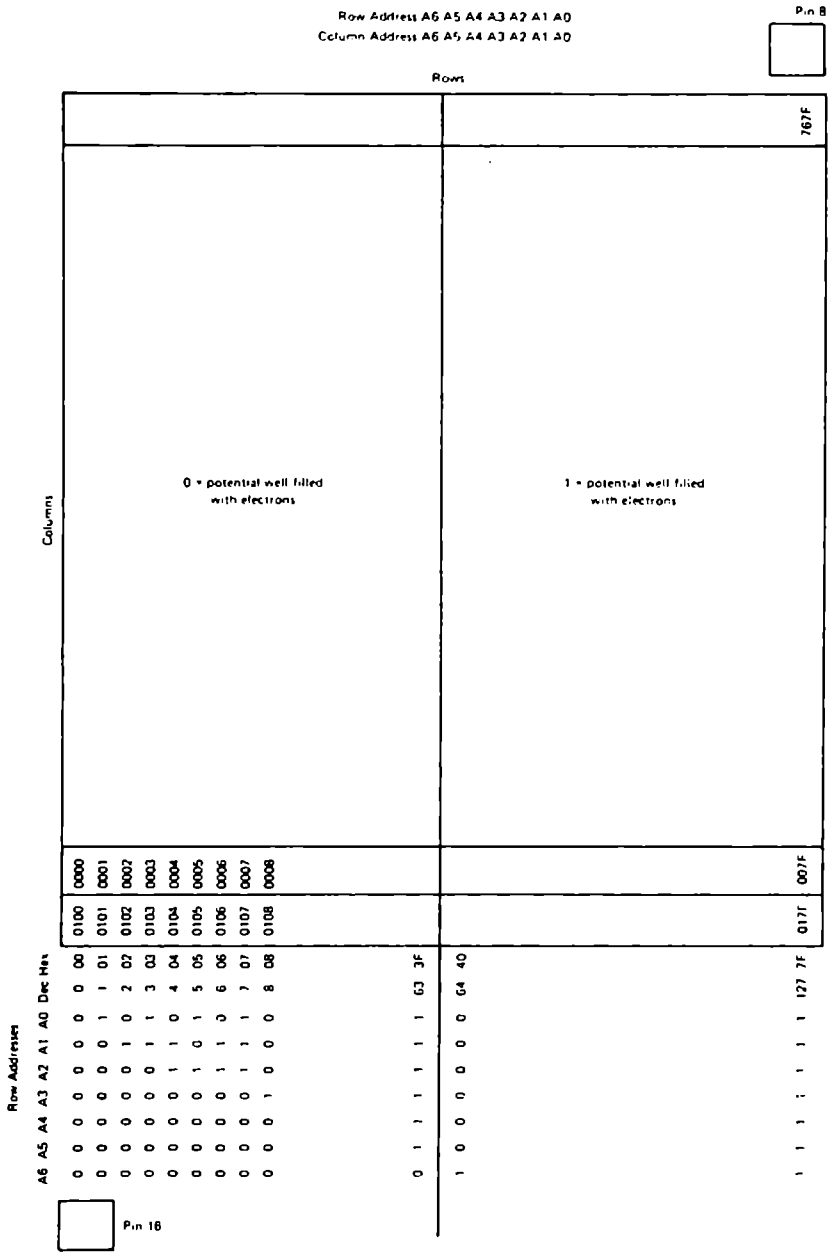
PAGE MODE READ CYCLE



PAGE MODE WRITE CYCLE



MCM4116B BIT ADDRESS MAP



MOTOROLA

MCM4517

Advance Information

16,384-BIT DYNAMIC RAM

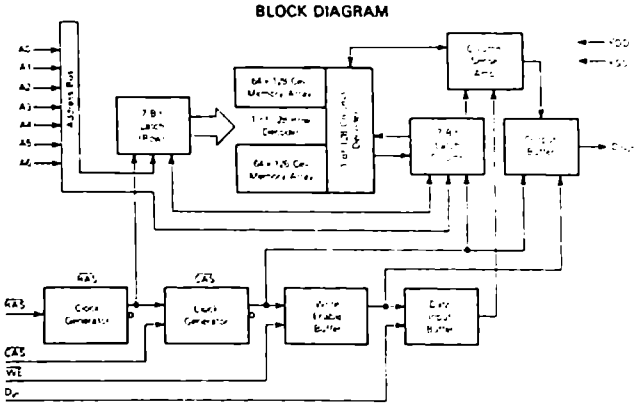
The MCM4517 is a 16,384-bit, high-speed, dynamic Random-Access Memory. Organized as 16,384 one-bit words and fabricated using HMOS high-performance, N-channel, silicon-gate technology. This new breed of 5-volt only dynamic RAM combines high performance with low cost and improved reliability.

By multiplexing row- and column-address inputs, the MCM4517 requires only seven address lines and permits packaging in standard 16-pin dual-in-line packages. Complete address decoding is done on chip with address latches incorporated. Data out is controlled by $\overline{CAS}$ allowing for greater system flexibility.

All inputs and outputs, including clocks, are fully TTL compatible. The MCM4517 incorporates a one-transistor cell design and dynamic storage techniques.

- Organized as 16,384 Words of 1 Bit
- Single +5 Volt Operation
- Fast 100 ns Operation
- Low Power Dissipation:
  - 150 mW Maximum (Active)
  - 14 mW Maximum (Standby)
- Maximum Access Time
  - MCM4517-10 – 100 ns
  - MCM4517-12 – 120 ns
  - MCM4517-15 – 150 ns
  - MCM4517-20 – 200 ns
- Three-State Data Output
- Internal Latches for Address and Data Input
- Early-Write Common I/O Output Capability
- 64K Compatible 128-cycle, 2 ms Refresh
- $\overline{RAS}$-only Refresh Mode
- $\overline{CAS}$ Controlled Output
- Upward Pin Compatibility from the 16K RAM (MCM4116) to the 64K RAM (MCM6664)
- Allows Negative Overshoot V_{IL} Min = −2 V
- Hidden $\overline{RAS}$ Only Refresh Capability

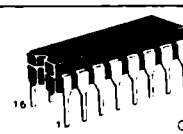
BLOCK DIAGRAM



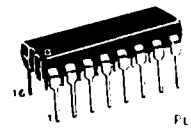
MOS

(N-CHANNEL, SILICON-GATE)

16,384-BIT
DYNAMIC RAM

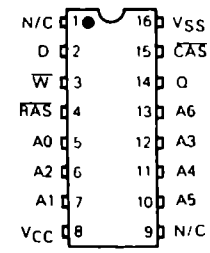


C SUFFIX
CERAMIC PACKAGE
CASE 620-06



P SUFFIX
PLASTIC PACKAGE
CASE 648-05

PIN ASSIGNMENT



PIN NAMES	
A0-A6	Address Input
D	Data In
Q	Data Out
$\overline{W}$	Read/Write Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
V_{CC}	Power (+5 V)
V_{SS}	Ground

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields, however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

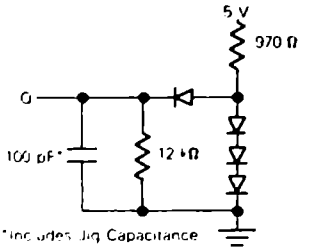
ADI836R1/11-80

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}	V_{in}, V_{out}	−2.0 to +7	Vdc
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Power Dissipation	P_D	1.0	W
Data Out Current	I_{out}	50	mA

NOTE Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

FIGURE 1 – OUTPUT LOAD



*Includes Jig Capacitance

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full Operating Voltage and Temperature Range Unless Otherwise Noted.)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply Voltage	V_{CC} V_{SS}	4.5 0	5.0 0	5.5 0	V	1
Logic 1 Voltage, All Inputs	V_{IH}	2.4	–	V_{CC} + 1	V	1
Logic 0 Voltage, All Inputs	V_{IL}	−2.0	–	0.8	V	1

DC CHARACTERISTICS

Characteristics	Symbol	Min	Typ	Max	Units	Notes
V_{CC} Supply Current (Standby)	I_{CC1}	–	1.2	2.5	mA	5
V_{CC} Supply Current (Operating) 4517-10, t_{RC} = 225 4517-12, t_{RC} = 250 4517-15, t_{RC} = 300 4517-20, t_{RC} = 350	I_{CC2}	 – – – –	 22 20 18 16	 27 25 23 21	mA	4
V_{CC} Supply Current (RAS Only Cycle) 4517-10, t_{RC} = 225 4517-12, t_{RC} = 250 4517-15, t_{RC} = 300 4517-20, t_{RC} = 350	I_{CC3}	 – – – –	 14 12 11 10	 18 16 14 12	mA	4
V_{CC} Standby Current (Standby, Output Enable) ($\overline{CAS}$ at V_{IL}, $\overline{RAS}$ at V_{IH})	I_{CC4}	–	2.5	5	mA	
Input Leakage Current (Any Input)	$I_{I(L)}$	–	–	10	µA	
Output Leakage Current ($0 \le V_{out} \le 5.5$) ($\overline{CAS}$ at Logic 1)	$I_{O(L)}$	–	–	10	µA	
Output Logic 1 Voltage@I_{out} = −4 mA	V_{OH}	2.4	–	–	V	
Output Logic 0 Voltage@I_{out} = 4 mA	V_{OL}	–	–	0.4	V	

AC OPERATING CONDITIONS AND CHARACTERISTICS

(See Notes 2, 3, 9, 14 and Figure 1) (Read, Write, and Read-Modify-Write Cycles)

(Full Operating Voltage and Temperature Range Unless Otherwise Noted)

RECOMMENDED AC OPERATING CONDITIONS

Parameter	Symbol	MCM4517-10		MCM4517-12		MCM4516-15		MCM4517-20		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RC}	225	–	250	–	300	–	350	–	ns	8, 9
Read-Modify-Write Cycle Time	t_{RWC}	235	–	270	–	320	–	365	–	ns	8, 9
Access Time from Row Address Strobe	t_{RAC}	–	100	–	120	–	150	–	200	ns	10, 12
Access Time from Column Address Strobe	t_{CAC}	–	60	–	75	–	95	–	120	ns	11, 12
Output Buffer and Turn-Off Delay	t_{OFF}	0	30	0	35	0	40	0	60	ns	18
Row Address Strobe Precharge Time	t_{RP}	100	–	110	–	125	–	150	–	ns	
Row Address Strobe Pulse Width	t_{RAS}	100	10000	120	10000	150	10000	200	10000	ns	
Column Address Strobe Pulse Width	t_{CAS}	60	10000	75	10000	95	10000	120	10000	ns	
Row to Column Strobe Lead Time	t_{RCD}	25	40	25	45	25	55	30	80	ns	13
Row Address Setup Time	t_{ASR}	0	–	0	–	0	–	0	–	ns	
Row Address Hold Time	t_{RAH}	15	–	15	–	20	–	25	–	ns	
Column Address Setup Time	t_{ASC}	0	–	0	–	0	–	0	–	ns	
Column Address Hold Time	t_{CAH}	40	–	45	–	55	–	60	–	ns	
Column Address Hold Time Referenced to $\overline{RAS}$	t_{AR}	80	–	90	–	110	–	140	–	ns	
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	3	50	ns	6

AC OPERATING CONDITIONS AND CHARACTERISTICS

(See Notes 2, 3, 9, 14 and Figure 1)

(Read, Write, and Read-Modify-Write Cycles)

(Full Operating Voltage and Temperature Range Unless Otherwise Noted)

Parameter	Symbol	MCM4517-10		MCM4517-12		MCM4517-15		MCM4517-20		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Read Command Setup Time	t_{RCS}	0	–	0	–	0	–	0	–	ns	
Read Command Hold Time	t_{RCH}	0	–	0	–	0	–	0	–	ns	14
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	20	–	25	–	35	–	40	–		14
Write Command Hold Time	t_{WCH}	40	–	45	–	55	–	60	–	ns	
Write Command Hold Time Referenced to $\overline{RAS}$	t_{WCR}	90	–	100	–	120	–	140	–	ns	
Write Command Pulse Width	t_{WP}	30	–	35	–	40	–	45	–	ns	
Write Command to Row Strobe Lead Time	t_{RWL}	40	–	45	–	50	–	55	–	ns	
Write Command to Column Strobe Lead Time	t_{CWL}	40	–	45	–	50	–	55	–	ns	
Data in Setup Time	t_{DS}	0	–	0	–	0	–	0	–	ns	15
Data in Hold Time	t_{DH}	40	–	45	–	55	–	60	–	ns	15
Data in Hold Time Referenced to $\overline{RAS}$	t_{DHR}	80	–	90	–	110	–	140	–	ns	
Column to Row Strobe Precharge Time	t_{CRP}	0	–	0	–	0	–	0	–	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	60	–	75	–	95	–	120	–	ns	
Refresh Period	t_{RFSH}	–	2.0	–	2.0	–	2.0	–	2.0	ms	
Write Command Setup Time	t_{WCS}	0	–	0	–	0	–	0	–	ns	16
$\overline{CAS}$ to $\overline{WRITE}$ Delay	t_{CWD}	50	–	60	–	75	–	80	–	ns	16
$\overline{RAS}$ to $\overline{WRITE}$ Delay	t_{RWD}	90	–	110	–	140	–	160	–	ns	16
$\overline{CAS}$ Hold Time	t_{CSH}	100	–	120	–	150	–	200	–	ns	
$\overline{CAS}$ Precharge, Non Page Mode	t_{CPN}	30	–	35	–	40	–	50	–	ns	

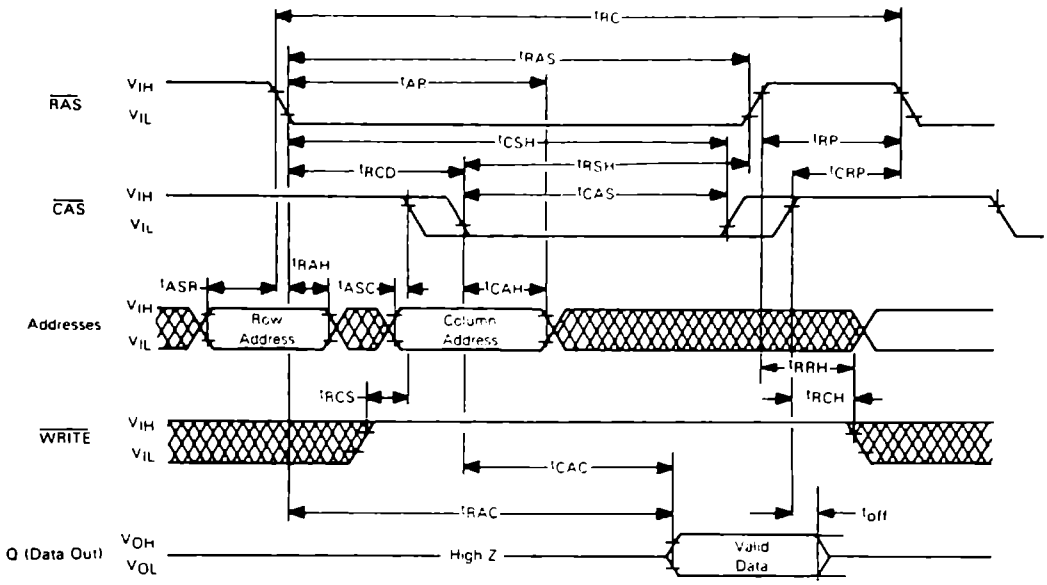
CAPACITANCE (f = 1.0 MHz, T_A = 25°C, V_{CC} = +5 V, Periodically sampled rather than 100% tested.)

Parameter	Symbol	Typ	Max	Units	Notes
Input Capacitance (A0-A6), D_{in}	C_{I1}	4.0	5.0	pF	7
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	C_{I2}	5.0	7.0	pF	7

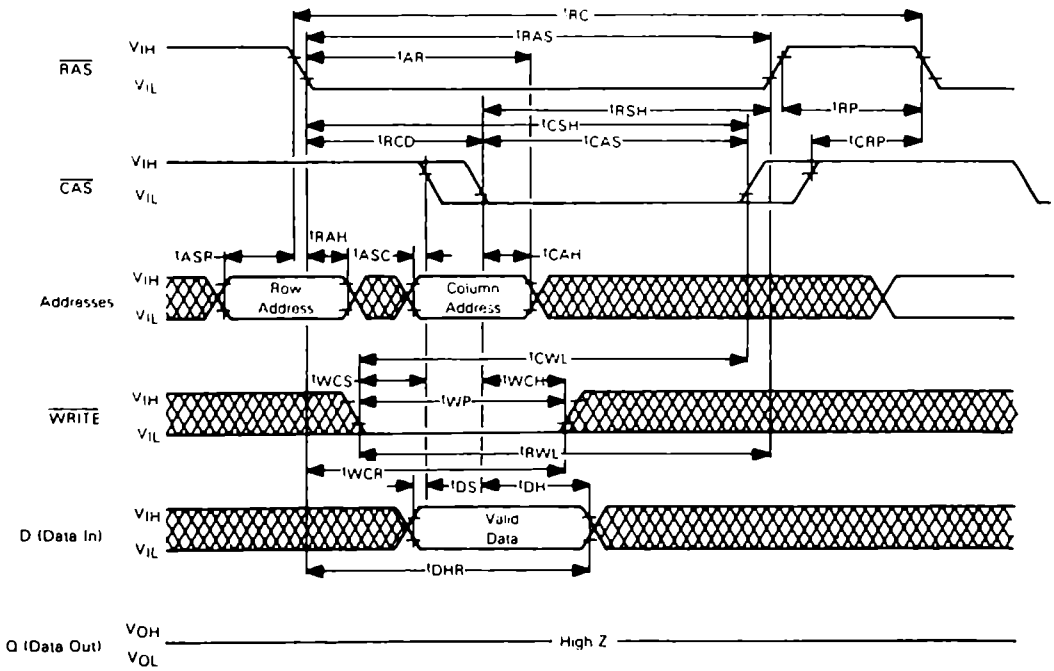
NOTES

1. All voltages referenced to V_{SS}.
2. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
3. An initial pause of 100 µs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is guaranteed.
4. Current is a function of cycle rate and output loading; maximum current is measured at the fastest cycle rate with the output open.
5. Output is disabled (open-circuit) and $\overline{RAS}$ and $\overline{CAS}$ are both at a logic 1.
6. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transmit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
7. Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation $C = \frac{I\Delta t}{\Delta V}$.
8. The specifications for t_{RC} (min), and t_{RWC} (min) are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
9. AC measurements assume t_T = 5.0 ns.
10. Assumes that $t_{RCD} \leq t_{RCD}$ (Max).
11. Assumes that $t_{RCD} \geq t_{RCD}$ (Max).
12. Measured with a current load equivalent to 2 TTL loads (+200 µA, −4 mA) and 100 pF (V_{OH} = 2.0 V, V_{OL} = 0.8 V).
13. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
14. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
15. These parameters are referenced to $\overline{CAS}$ leading edge in random write cycles and to $\overline{WRITE}$ leading edge in delayed write or read-modify-write cycles.
16. t_{WCS}, t_{CWD}, and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min), the cycle is a read-write cycle and the data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
17. Addresses, data-in and $\overline{WRITE}$ are don't care. Data-out depends on the state of $\overline{CAS}$. If $\overline{CAS}$ remains low, the previous output will remain valid. $\overline{CAS}$ is allowed to make an active to inactive transition during the $\overline{RAS}$-only refresh cycle. When $\overline{CAS}$ is brought high, the output will assume a high-impedance state.
18. t_{off} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

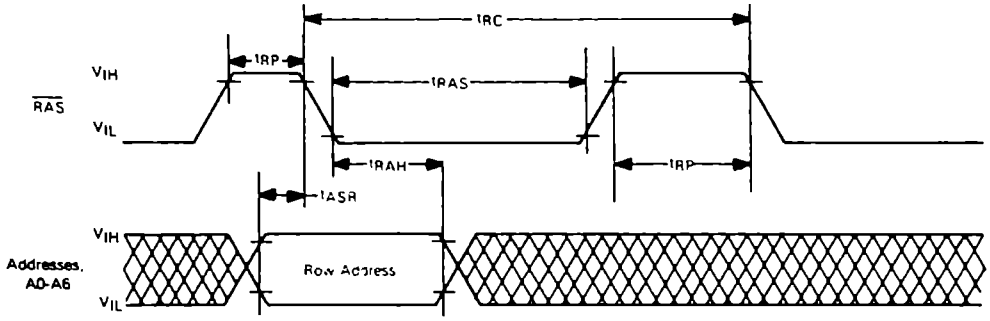
READ CYCLE TIMING



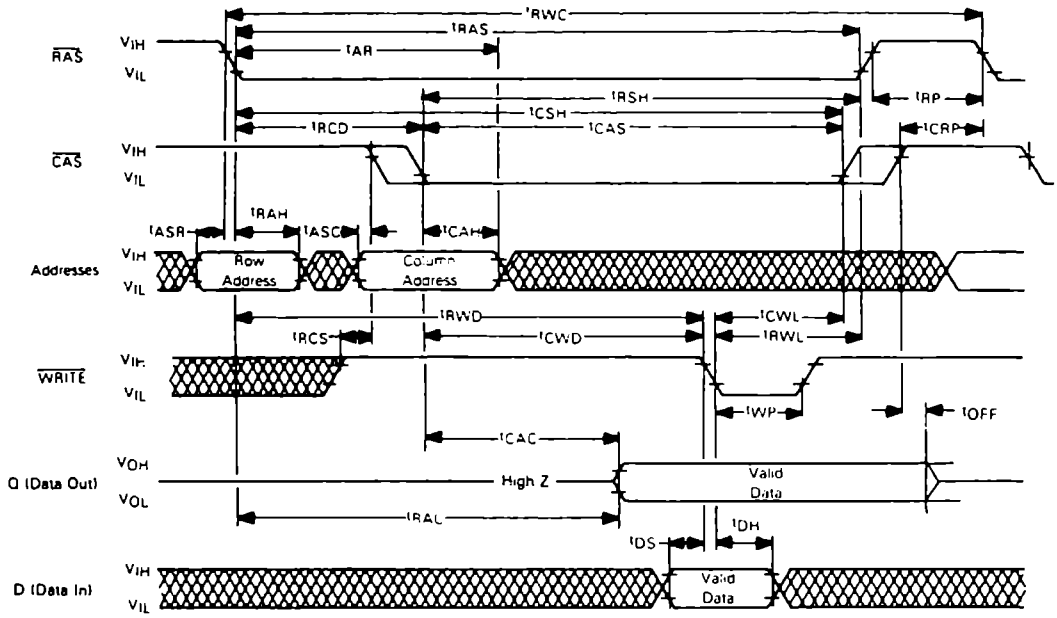
WRITE CYCLE TIMING



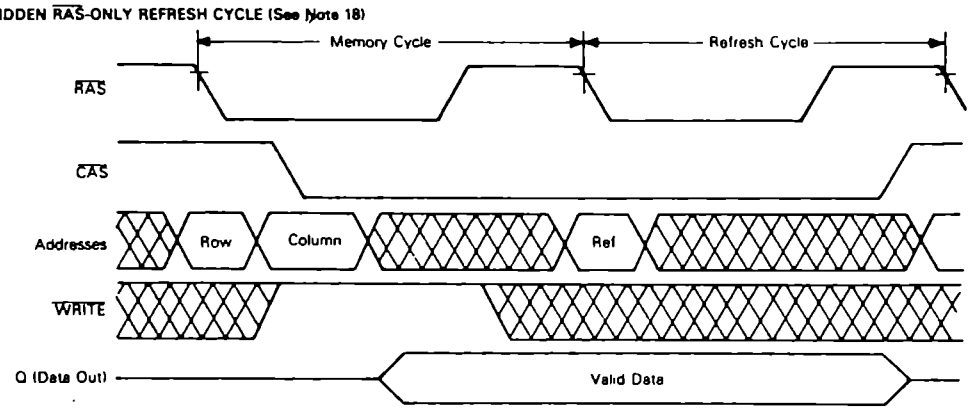
RAS-ONLY REFRESH CYCLE
(Data-in and Write are Don't Care, $\overline{CAS}$ is HIGH)



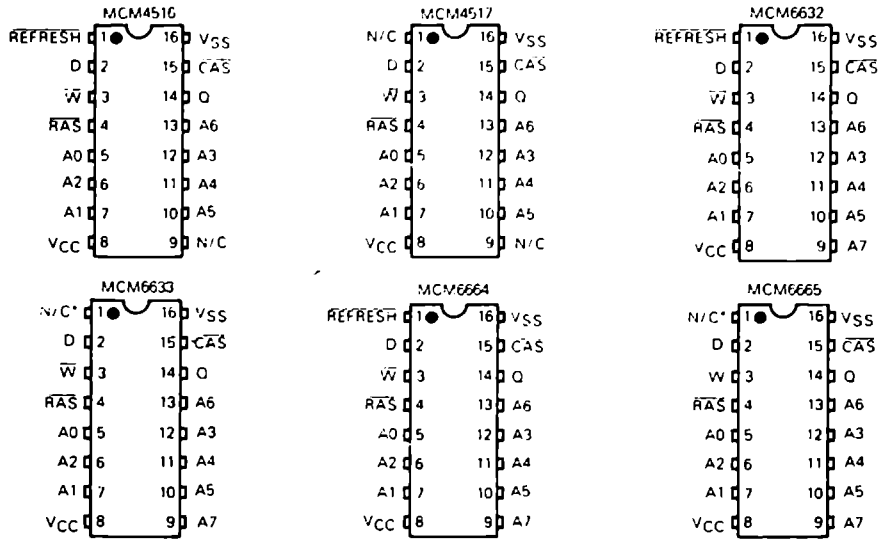
READ-WRITE/READ-MODIFY-WRITE CYCLE



HIDDEN $\overline{RAS}$-ONLY REFRESH CYCLE (See Note 18)



PIN ASSIGNMENT COMPARISON



PIN VARIATIONS

Pin Number	MCM4116	MCM4516	MCM4517	MCM6632	MCM6663	MCM6664	MCM6665
1	V_{BB} (−5 V)	$\overline{\text{REFRESH}}$	N/C	$\overline{\text{REFRESH}}$	N/C*	$\overline{\text{REFRESH}}$	N/C*
8	V_{DD} (+12 V)	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}
9	V_{CC} (+5 V)	N/C	N/C	A7	A7	A7	A7

*Internal pullup resistor should be left open or tied to V_{CC}

MOTOROLA

MCM6632

32,768-BIT DYNAMIC RAM

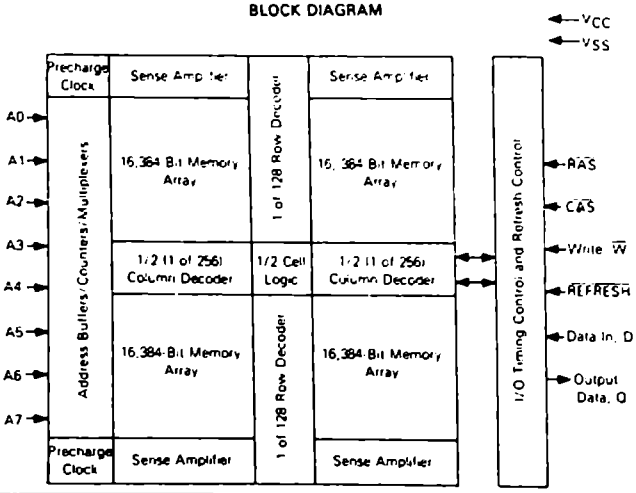
The MCM6632 is a 32,768 bit, high-speed, dynamic Random-Access Memory. Organized as 32,768 one-bit words and fabricated using HMOS high performance N channel silicon-gate technology. This new breed of 5-volt only dynamic RAM combines high performance with low cost and improved reliability.

By multiplexing row- and column address inputs, the MCM6632 requires only eight address lines and permits packaging in standard 16-pin dual-in-line packages. Complete address decoding is done on chip with address latches incorporated. Data out is controlled by $\overline{CAS}$ allowing for greater system flexibility.

All inputs and outputs, including clocks, are fully TTL compatible. The MCM6632 incorporates a one-transistor cell design and dynamic storage techniques. In addition to the $\overline{RAS}$-only refresh mode, refresh control function available on pin 1 provides automatic and self-refresh modes.

- Organized as 32,768 Words of 1 Bit
- Single +5 V Operation
- Fast 150 ns Operation
- Low Power Dissipation
  - 275 mW Maximum (Active)
  - 30 mW Maximum (Standby)
- Three-State Data Output
- Internal Latches for Address and Data Input
- Early-Write Common I/O Capability
- 16K Compatible 128-Cycle, 2 ms Refresh
- Control on Pin 1 for Automatic and Self Refresh
- $\overline{RAS}$-only Refresh Mode
- $\overline{CAS}$ Controlled Output
- Upward Pin Compatible from the 16K RAM (MCM4116)
- One Half of the 64K RAM MCM6664
- The Operating Half of the MCM6632 is Indicated by Device Marking:
  - MCM66320 Tie A7 CAS (A15) Low "0"
  - MCM66321 Tie A7 CAS (A15) High "1"

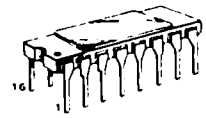
BLOCK DIAGRAM



MOS

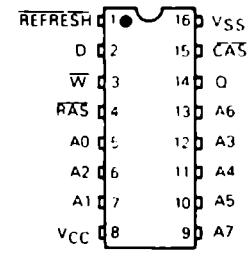
(N-CHANNEL, SILICON-GATE)

32,768-BIT DYNAMIC RANDOM ACCESS MEMORY



L SUFFIX
CERAMIC PACKAGE
CASE 690

PIN ASSIGNMENT



PIN NAMES	
$\overline{REFRESH}$	Refresh
A0-A7	Address Input
D	Data In
Q	Data Out
$\overline{W}$	Read/Write Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
V_{CC}	Power (+5 V)
V_{SS}	Ground

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields, however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

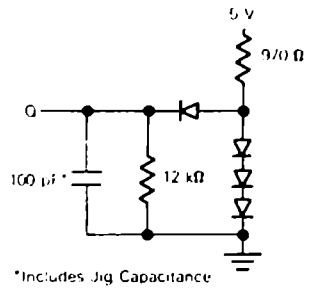
DS9826/9-80

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS} (except V_{CC})	V_{in}, V_{out}	−2 to +7	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{in}, V_{out}	1 to +7	V
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Power Dissipation	P_D	1.0	W
Data Out Current	I_{out}	50	mA

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

• FIGURE 1 – OUTPUT LOAD



*Includes Jig Capacitance

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted.)

RECOMMENDED OPERATING CONDITIONS

Parameter		Symbol	Min	Typ	Max	Unit	Notes
Supply Voltage	MCM6664-15, -20	V_{CC}	4.5	5.0	5.5	V	1
		V_{SS}	0	0	0	V	1
Logic 1 Voltage, All Inputs		V_{IH}	2.4	–	V_{CC} + 1	V	1
Logic 0 Voltage, All Inputs		V_{IL}	−2.0	–	0.8	V	1

DC CHARACTERISTICS

Characteristic	Symbol	Min	Max	Units	Notes
V_{CC} Power Supply Current (t_{RC} min)	I_{CC1}	–	50	mA	4
Standby V_{CC} Power Supply Current	I_{CC2}	–	5	mA	5
V_{CC} Power Supply Current During $\overline{RAS}$ Only Refresh Cycles	I_{CC3}	–	40	mA	–
Input Leakage Current (any input) (except $\overline{REFRESH}$) ($V_{SS} \le V_{in} \le V_{CC}$)	$I_{I(L)}$	–	10	µA	–
$\overline{REFRESH}$ Input Current ($V_F = V_{SS}$)	I_F	–	125	µA	–
Output Leakage Current ($\overline{CAS}$ at logic 1, $0 \le V_{out} \le 5.5$)	$I_{O(L)}$	–	10	µA	–
Output Logic 1 Voltage @ I_{out} = −4 mA	V_{OH}	2.4	–	V	–
Output Logic 0 Voltage @ I_{out} = 4 mA	V_{OL}	–	0.4	V	–

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, V_{CC} = 5 V. Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Typ	Max	Units	Notes
Input Capacitance (A0-A7), D_{in}	C_{I1}	4	5	pF	7
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	C_{I2}	8	10	pF	7
Output Capacitance (D_{out}) ($\overline{CAS}$ = V_{IH} to disable output)	C_o	5	7	pF	7

AC OPERATING CONDITIONS AND CHARACTERISTICS

(See Notes 2, 3, 6, and Figure 1)

(Read, Write, and Read-Modify-Write Cycles)

(Full Operating Voltage and Temperature Range Unless Otherwise Noted)

Parameter	Symbol	MCM6632-15		MCM6632-20		Units	Notes
		Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RC}	300	–	350	–	ns	8, 9
Read Write Cycle Time	t_{RWC}	300	–	350	–	ns	8, 9
Access Time from Row Address Strobe	t_{RAC}	–	150	–	200	ns	10, 12
Access Time from Column Address Strobe	t_{CAC}	–	75	–	110	ns	11, 12
Output Buffer and Turn-Off Delay	t_{OFF}	0	30	0	40	ns	18
Row Address Strobe Precharge Time	t_{RP}	120	–	140	–	ns	–
Row Address Strobe Pulse Width	t_{RAS}	150	10000	200	10000	ns	–
Column Address Strobe Pulse Width	t_{CAS}	75	10000	110	10000	ns	–
Row to Column Strobe Lead Time	t_{RCD}	30	75	35	90	ns	13
Row Address Setup Time	t_{ASR}	0	–	0	–	ns	–
Row Address Hold Time	t_{RAH}	25	–	30	–	ns	–
Column Address Setup Time	t_{ASC}	0	–	0	–	ns	–
Column Address Hold Time	t_{CAH}	45	–	55	–	ns	–
Column Address Hold Time Referenced to $\overline{RAS}$	t_{AR}	120	–	155	–	ns	–
Transition Time (Rise and Fall)	t_T	3	50	3	50	ns	6

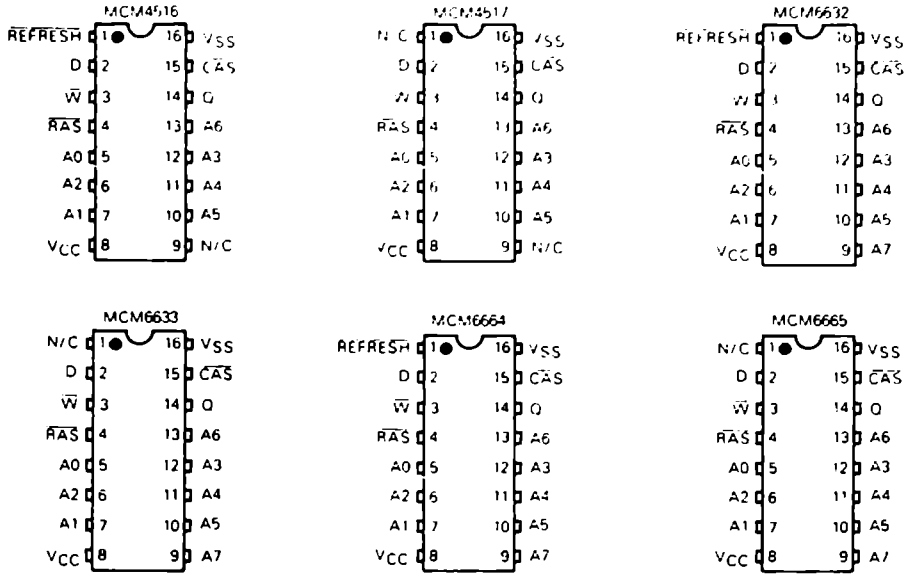
AC OPERATING CONDITIONS AND CHARACTERISTICS

(See Notes 2, 3, 6 and Figure 1)
(Read, Write, and Read-Modify-Write Cycles)
(Full Operating Voltage and Temperature Range Unless Otherwise Noted)

Parameter	Symbol	MCM6632-15		MCM6632-20		Units	Notes
		Min	Max	Min	Max		
Read Command Setup Time	t_{RCS}	0	–	0	–	ns	
Read Command Hold Time	t_{RCH}	10	–	10	–	ns	14
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	30	–	35	–	ns	14
Write Command Hold Time	t_{WCH}	45	–	55	–	ns	–
Write Command Hold Time Referenced to $\overline{RAS}$	t_{WCR}	120	–	155	–	ns	–
Write Command Pulse Width	t_{WP}	45	–	55	–	ns	–
Write Command to Row Strobe Lead Time	t_{RWL}	45	–	55	–	ns	–
Write Command to Column Strobe Lead Time	t_{CWL}	45	–	55	–	ns	–
Data-in Setup Time	t_{DS}	0	–	0	–	ns	15
Data-in Hold Time	t_{DH}	45	–	55	–	ns	15
Data-in Hold Time Referenced to $\overline{RAS}$	t_{DHR}	120	–	155	–	ns	–
Column to Row Strobe Precharge Time	t_{CRP}	−10	–	−10	–	ns	–
$\overline{RAS}$ Hold Time	t_{RSH}	75	–	110	–	ns	–
Refresh Period	t_{RFSH}	–	2 0	–	2 0	ms	–
$\overline{WRITE}$ Command Setup Time	t_{WCS}	−10	–	−10	–	ns	16
$\overline{CAS}$ to $\overline{WRITE}$ Delay	t_{CWD}	45	–	55	–	ns	16
$\overline{RAS}$ to $\overline{WRITE}$ Delay	t_{RWD}	125	–	160	–	ns	16
$\overline{CAS}$ Hold Time	t_{CSH}	150	–	200	–	ns	–
$\overline{RAS}$ to $\overline{REFRESH}$ Delay	t_{RFD}	0	–	0	–	ns	–
$\overline{REFRESH}$ Period (Battery Backup Mode)	t_{FBP}	2000	–	2000	–	ns	–
$\overline{REFRESH}$ to $\overline{RAS}$ Precharge Time (Battery Backup Mode)	t_{FBR}	390	–	460	–	ns	–
$\overline{REFRESH}$ Cycle Time (Auto Pulse Mode)	t_{FC}	330	–	380	–	ns	
$\overline{REFRESH}$ Pulse Period (Auto Period Mode)	t_{FP}	60	2000	60	2000	ns	–
$\overline{REFRESH}$ to $\overline{RAS}$ Setup Time (Auto Pulse Mode)	t_{FSR}	30	–	30	–	ns	–
$\overline{REFRESH}$ to $\overline{RAS}$ Delay Time (Auto Pulse Mode)	t_{FRD}	390	–	460	–	ns	–
$\overline{REFRESH}$ Inactive Time	t_{FI}	30	–	30	–	ns	–
$\overline{RAS}$ to $\overline{REFRESH}$ Lead Time	t_{FRL}	390	–	460	–	ns	–

NOTES:
1. All voltages referenced to V_{SS}.
2. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
3. An initial pause of 100 µs is required after power up followed by any 8 $\overline{RAS}$ cycles before proper device operation is guaranteed.
4. Current is a function of cycle rate and output loading; maximum current is measured at the fastest cycle rate with the output open.
5. Output is disabled (open-circuit) and $\overline{RAS}$ and $\overline{CAS}$ are both at a logic 1.
6. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transmit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
7. Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: $C = \frac{I\Delta t}{\Delta V}$
8. The specifications for t_{RC} (min), and t_{RWC} (min) are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$) is assured.
9. AC measurements assume $t_T = 5.0$ ns.
10. Assumes that $t_{RCD} \le t_{RCD}$ (Max).
11. Assumes that $t_{RCD} \ge t_{RCD}$ (Max).
12. Measured with a current load equivalent to 2 TTL loads (−200 µA, −4 mA) and 100 pF ($V_{OH} = 2.0$ V, $V_{OL} = -0.8$ V).
13. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
14. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
15. These parameters are referenced to $\overline{CAS}$ leading edge in random write cycles and to $\overline{WRITE}$ leading edge in delayed write or read-modify-write cycles.
16. t_{WCS}, t_{CWD}, and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \ge t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \ge t_{CWD}$ (min) and $t_{RWD} \ge t_{RWD}$ (min), the cycle is a read-write cycle and the data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
17. Addresses, data-in and $\overline{WRITE}$ are don't care. Data-out depends on the state of $\overline{CAS}$. If $\overline{CAS}$ remains low, the previous output will remain valid. $\overline{CAS}$ is allowed to make an active to inactive transition during the pin #1 refresh cycle. When $\overline{CAS}$ is brought high, the output will assume a high-impedance state.
18. t_{off} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

PIN ASSIGNMENT COMPARISON



PIN VARIATIONS

Pin Number	MCM4116	MCM4516	MCM4517	MCM6632	MCM6663	MCM6664	MCM6665
1	V_{BB} (– 5 V)	$\overline{\text{REFRESH}}$	N/C	$\overline{\text{REFRESH}}$	N/C	$\overline{\text{REFRESH}}$	N/C
8	V_{DD} (+ 12 V)	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}
9	V_{CC} (+ 5 V)	N/C	N/C	A7	A7	A7	A7

On-Chip Refresh Features/Benefits

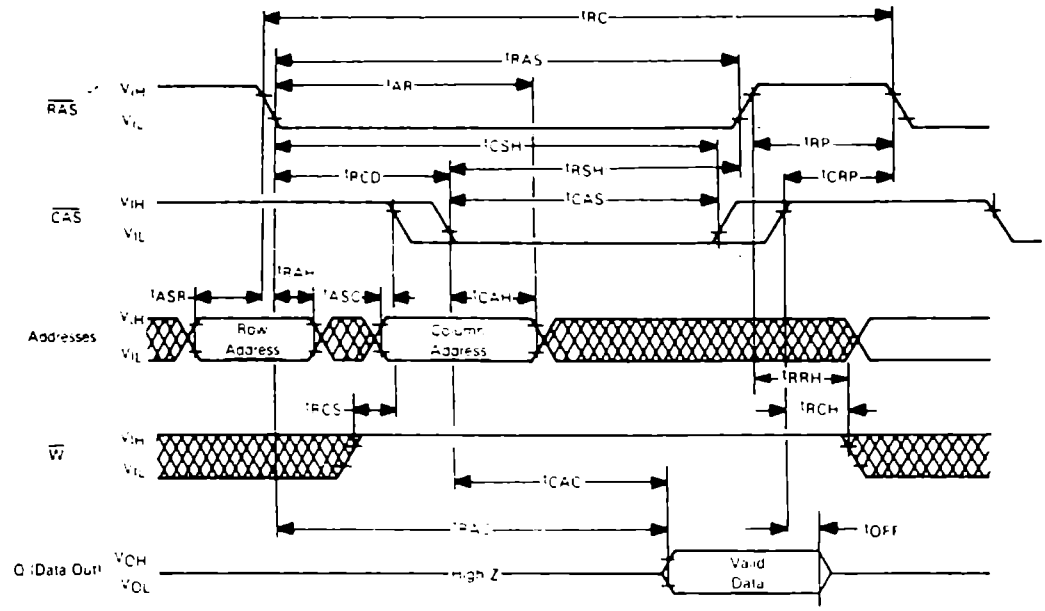
Reduce System Refresh Controller Design Problem
Reduce System Parts Count
Reduce System Noise Increasing System Reliability
Reduce System Power During Refresh

ORDERING INFORMATION

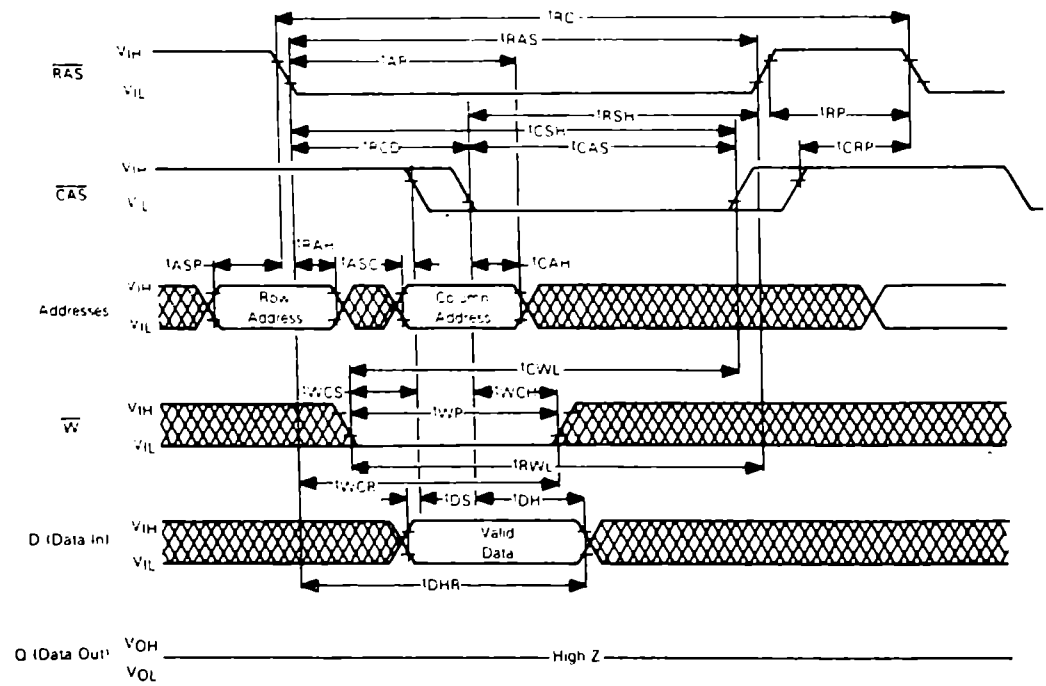
Part Number	Description	Speed	Marking*
MCM6632L15	32K Dynamic	150	MCM66320L15/MCM66321L15
MCM66320L15	Random Access	150	MCM66320L15
MCM66321L15	Memory	150	MCM66321L15
MCM6632L20	Sidebraze	200	MCM66320L20/MCM66321L20
MCM66320L20	Package "L"	200	MCM66320L20
MCM66321L20		200	MCM66321L20

*MCM66320 = Tie A7 CAS (A15) Low "0"
MCM66321 = Tie A7 CAS (A15) High "1"

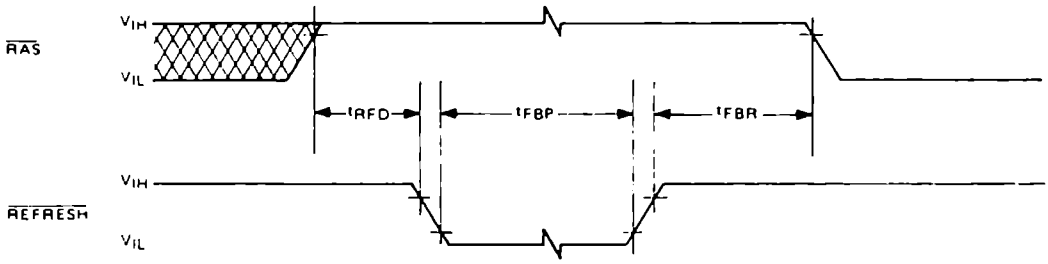
READ CYCLE TIMING



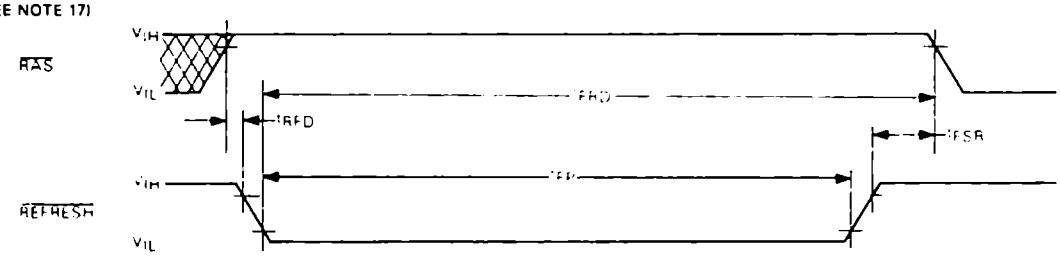
WRITE CYCLE TIMING



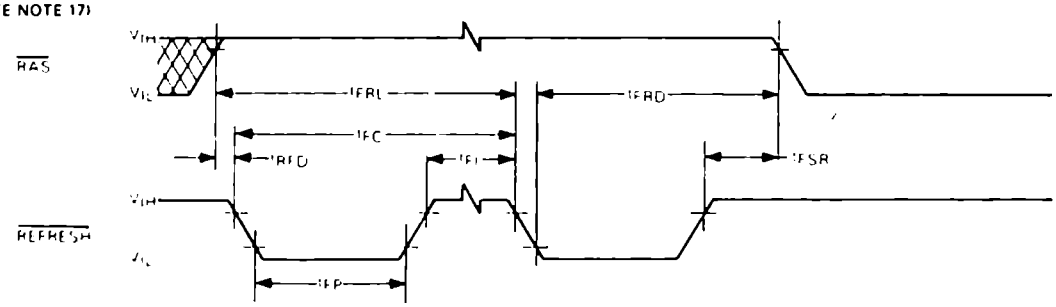
SELF REFRESH MODE (Battery Backup)
(SEE NOTE 17)



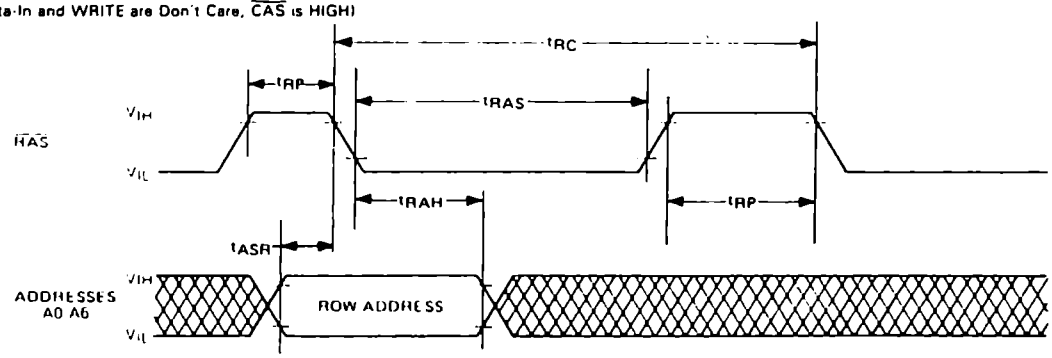
AUTOMATIC PULSE REFRESH CYCLE – SINGLE PULSE
(SEE NOTE 17)



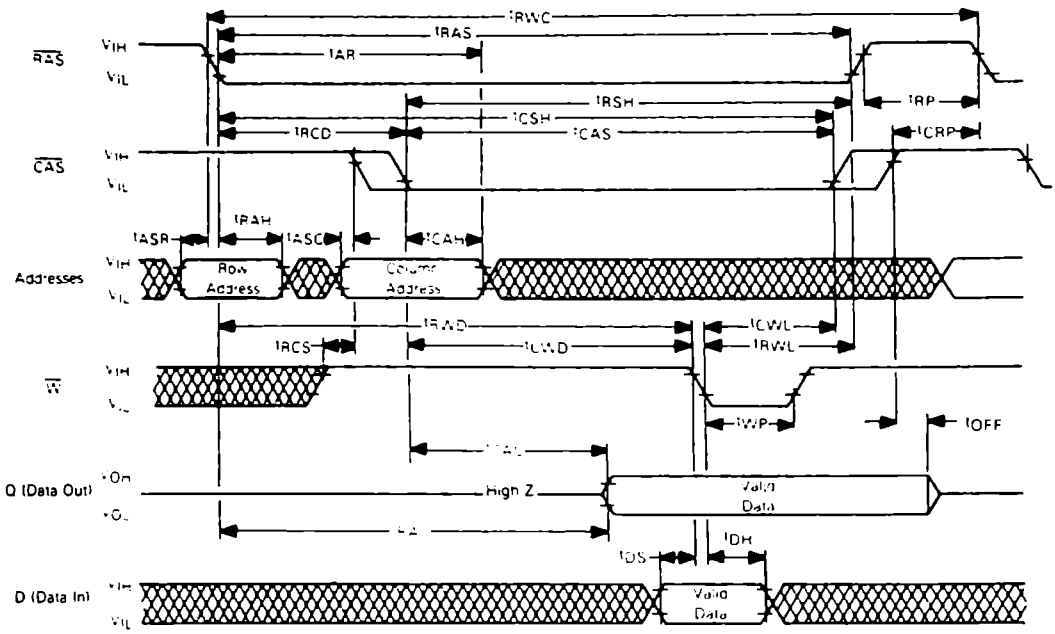
AUTOMATIC PULSE REFRESH CYCLE – MULTIPLE PULSE
(SEE NOTE 17)



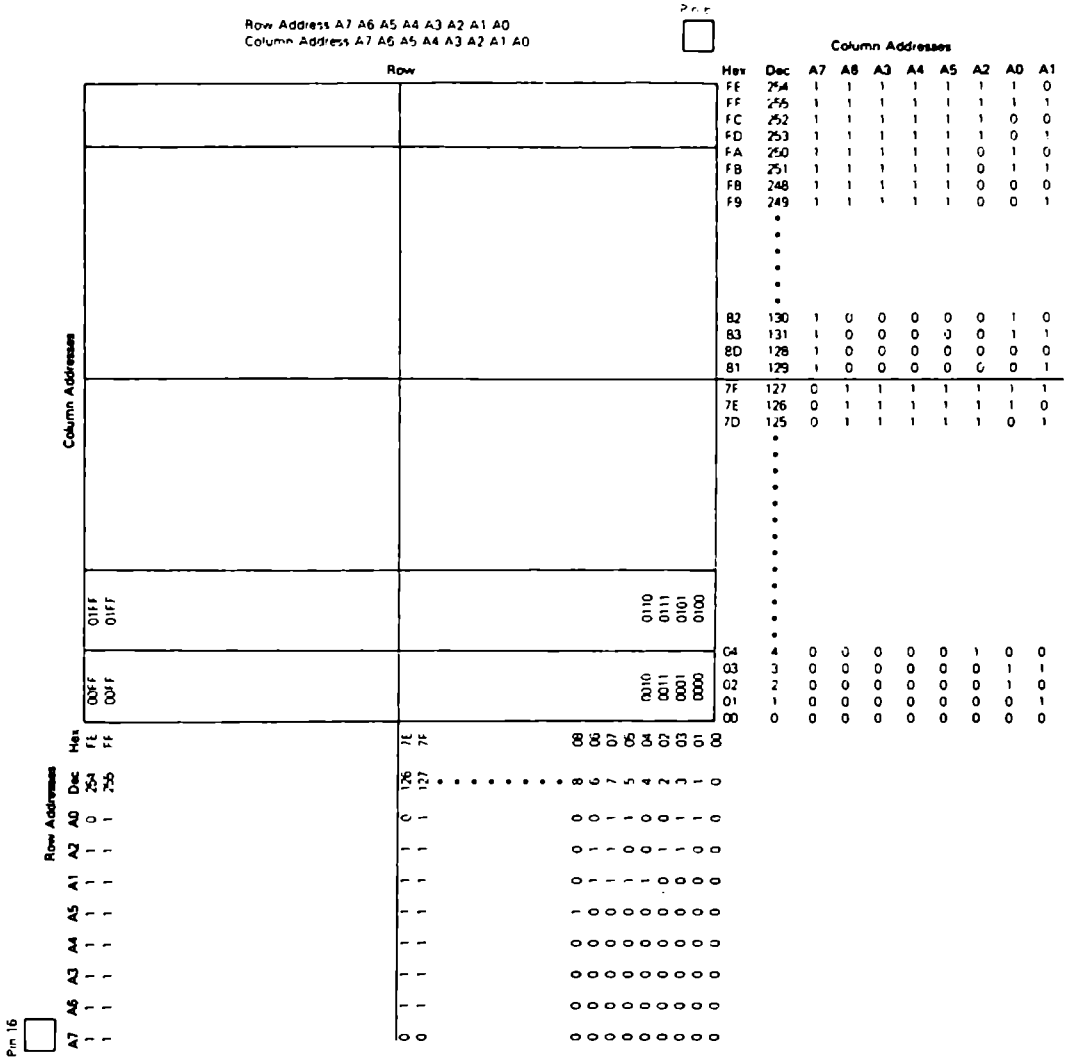
RAS-ONLY REFRESH CYCLE
(Data-In and WRITE are Don't Care, $\overline{CAS}$ is HIGH)



READ-WRITE/READ-MODIFY-WRITE CYCLE



MCM6664 BIT ADDRESS MAP



$\overline{\text{Data Stored}} = D_{in} \bullet A_{0X} \bullet A_{1Y}$

Column Address A1	Row Address A0	Data Stored
0	0	Inverted
0	1	True
1	0	True
1	1	Inverted

MOTOROLA

MCM6633

32,768-BIT DYNAMIC RAM

The MCM6633 is a 32,768 bit, high-speed, dynamic Random-Access Memory. Organized as 32,768 one-bit words and fabricated using HMOS high-performance N-channel silicon-gate technology. This new breed of 5-volt only dynamic RAM combines high performance with low cost and improved reliability.

By multiplexing row- and column-address inputs, the MCM6633 requires only eight address lines and permits packaging in standard 16-pin dual-in-line packages. Complete address decoding is done on chip with address latches incorporated. Data out is controlled by $\overline{CAS}$ allowing for greater system flexibility.

All inputs and outputs, including clocks, are fully TTL compatible. The MCM6633 incorporates a one-transistor cell design and dynamic storage techniques.

- Organized as 32,768 Words of 1 Bit
- Single +5 V Operation
- Fast 150 ns Operation
- Low Power Dissipation
  - 275 mW Maximum (Active)
  - 30 mW Maximum (Standby)
- Three-State Data Output
- Internal Latches for Address and Data Input
- Early-Write Output Capability
- 16K Compatible 128-Cycle, 2 ms Refresh
- $\overline{RAS}$-only Refresh Mode
- $\overline{CAS}$ Controlled Output
- Upward Pin Compatible from the 16K RAM (MCM4116, MCM4516, MCM4517)
- One Half of the 64K RAM MCM6665
- The Operating Half of the MCM6633 is Indicated by Device Marking
  - MCM66330 Tie A7 $\overline{CAS}$ (A15) Low "0"
  - MCM66331 Tie A7 $\overline{CAS}$ (A15) High "1"

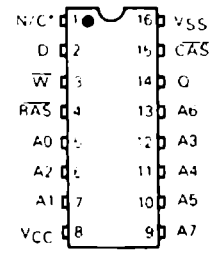
MOS

(N-CHANNEL, SILICON-GATE)

32,768-BIT DYNAMIC RANDOM ACCESS MEMORY

L SUFFIX
CERAMIC PACKAGE
CASE 690

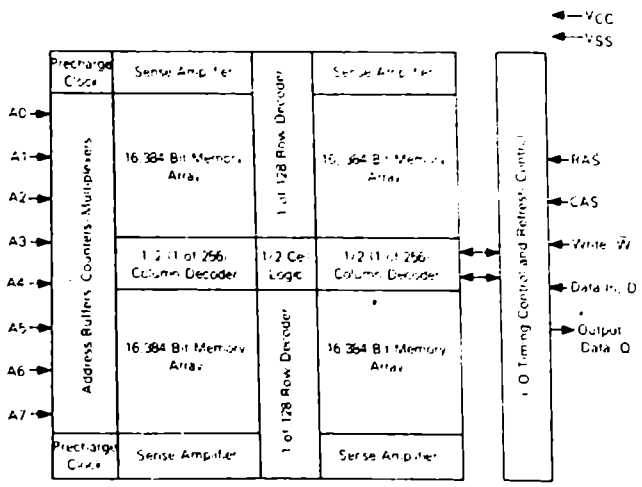
PIN ASSIGNMENT



*For maximum compatibility with MCM6632 and MCM6664, a V_{CC} trace should go to pin #1.

PIN NAMES	
A0-A7	Address Input
D	Data In
Q	Data Out
$\overline{W}$	Read/Write Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
V_{CC}	Power (+5 V)
V_{SS}	Ground

BLOCK DIAGRAM



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

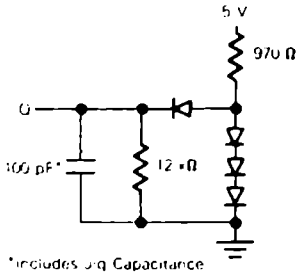
DS9825/9-80

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS} (Except V_{CC})	V_{in}, V_{out}	-2 to +7	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{in}, V_{out}	-1 to +7	V
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C
Power Dissipation	P_D	1	W
Data Out Current	I_{out}	50	mA

NOTE Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

FIGURE 1 – OUTPUT LOAD



*Includes j-g Capacitance

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted.)

RECOMMENDED OPERATING CONDITIONS

Parameter		Symbol	Min	Typ	Max	Unit	Notes
Supply Voltage	MCM6633L15/MCM6633L20	V_{CC}	4.5	5.0	5.5	Vdc	1
	MCM6633L15-5/MCM6633L20-5	V_{CC}	4.75	5.0	5.25		
		V_{SS}	0	0	0		
Logic 1 Voltage, All Inputs		V_{IH}	2.4	–	7.0	Vdc	1
Logic 0 Voltage		V_{IL}	-2.0	–	0.8	Vdc	1

DC CHARACTERISTICS

Characteristic	Symbol	Min	Max	Units	Notes
V_{CC} Power Supply Current (t_{RC} min.)	I_{CC1}	–	50	mA	4
Standby V_{CC} Power Supply Current	I_{CC2}	–	5	mA	5
V_{CC} Power Supply Current During $\overline{RAS}$ Only Refresh Cycles	I_{CC3}	–	40	mA	–
Input Leakage Current (any input) $0 \le V_{in} \le 5.5$ (Except Pin 1)	$I_{I(L)}$	–	10	µA	–
Output Leakage Current ($0 \le V_{out} \le 5.5$; $\overline{CAS}$ at Logic 1)	$I_{O(L)}$	–	10	µA	–
Output Logic 1 Voltage @ I_{out} = -4 mA	V_{OH}	2.4	–	V	–
Output Logic 0 Voltage @ I_{out} = 4 mA	V_{OL}	–	0.4	V	–

AC OPERATING CONDITIONS AND CHARACTERISTICS

(See Notes 2, 3, 6, and Figure 1)

(Read, Write, and Read-Modify-Write Cycles)

(Full Operating Voltage and Temperature Range Unless Otherwise Noted)

Parameter	Symbol	MCM6633-15		MCM6633-20		Units	Notes
		Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RC}	300	–	350	–	ns	8, 9
Read-Write Cycle Time	t_{RWC}	300	–	350	–	ns	8, 9
Access Time from Row Address Strobe	t_{RAC}	–	150	–	200	ns	10, 12
Access Time from Column Address Strobe	t_{CAC}	–	75	–	110	ns	11, 12
Output Buffer and Turn-Off Delay	t_{OFF}	0	30	0	40	ns	17
Row Address Strobe Precharge Time	t_{RP}	120	–	140	–	ns	–
Row Address Strobe Pulse Width	t_{RAS}	150	10000	200	10000	ns	–
Column Address Strobe Pulse Width	t_{CAS}	75	10000	110	10000	ns	–
Row to Column Strobe Lead Time	t_{RCD}	30	75	35	90	ns	13
Row Address Setup Time	t_{ASR}	0	–	0	–	ns	–
Row Address Hold Time	t_{RAH}	25	–	30	–	ns	–
Column Address Setup Time	t_{ASC}	0	–	0	–	ns	–
Column Address Hold Time	t_{CAH}	45	–	55	–	ns	–
Column Address Hold Time Referenced to $\overline{RAS}$	t_{AR}	120	–	155	–	ns	–
Transition Time (Rise and Fall)	t_T	3	50	3	50	ns	6

AC OPERATING CONDITIONS AND CHARACTERISTICS

(See Notes 2, 3, 6, and Figure 1)

(Read, Write, and Read-Modify-Write Cycles)

(Full Operating Voltage and Temperature Range Unless Otherwise Noted)

Parameter	Symbol	MCM6633-15		MCM6633-20		Units	Notes
		Min	Max	Min	Max		
Read Command Setup Time	t_{RCS}	0	–	0	–	ns	–
Read Command Hold time	t_{RCH}	10	–	10	–	ns	14
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	30	–	35	–	ns	14
Write Command Hold Time	t_{WCH}	45	–	55	–	ns	–
Write Command Hold Time Referenced to $\overline{RAS}$	t_{WCR}	120	–	155	–	ns	–
Write Command Pulse Width	t_{WP}	45	–	55	–	ns	–
Write Command to Row Strobe Lead Time	t_{RWL}	45	–	55	–	ns	–
Write Command to Column Strobe Lead Time	t_{CWL}	45	–	55	–	ns	–
Data-in Setup Time	t_{DS}	0	–	0	–	ns	15
Data-in Hold Time	t_{DH}	45	–	55	–	ns	15
Data-in Hold Time Referenced to $\overline{RAS}$	t_{DHR}	120	–	155	–	ns	–
Column to Row Strobe Precharge Time	t_{CRP}	– 10	–	– 10	–	ns	–
$\overline{RAS}$ Hold Time	t_{RSH}	75	–	110	–	ns	–
Refresh Period	t_{RFSH}	–	2.0	–	2.0	ms	–
$\overline{WRITE}$ Command Setup Time	t_{WCS}	– 10	–	– 10	–	ns	16
$\overline{CAS}$ to $\overline{WRITE}$ Delay	t_{CWD}	45	–	55	–	ns	16
$\overline{RAS}$ to $\overline{WRITE}$ Delay	t_{RWD}	125	–	160	–	ns	16
$\overline{CAS}$ Hold Time	t_{CSH}	150	–	200	–	ns	–

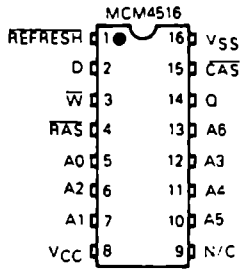
CAPACITANCE (f = 1.0 MHz, T_A = 25°C, V_{CC} = 5 V, Periodically Sampled Rather Than 100% Tested)

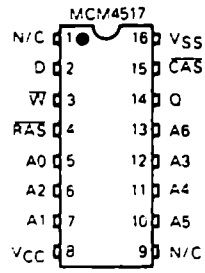
Parameter	Symbol	Typ	Max	Units	Notes
Input Capacitance (A0-A7), D	C_{i1}	4	5	pF	7
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	C_{i2}	8	10	pF	7
Output Capacitance (O) ($\overline{CAS}$ = V_{IH} to disable output)	C_o	5	7	pF	7

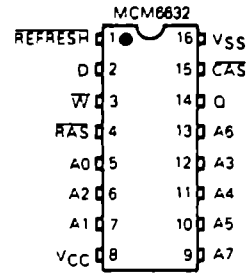
NOTES

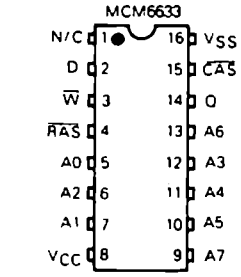
1. All voltages referenced to V_{SS}.
2. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
3. An initial pause of 100 µs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is guaranteed.
4. Current is a function of cycle rate and output loading; maximum current is measured at the fastest cycle rate with the output open.
5. Output is disabled (open-circuit) and $\overline{RAS}$ and $\overline{CAS}$ are both at a logic 1.
6. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
7. Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation $C = \frac{I\Delta_t}{\Delta V}$.
8. The specifications for t_{RC} (min) and t_{RWC} (min) are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
9. AC measurements assume t_T = 5.0 ns.
10. Assumes that $t_{RCD} \leq t_{RCD}$ (max).
11. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
12. Measured with a current load equivalent to 2 TTL loads (– 200 µA, – 4 mA) and 100 pF (V_{OH} = 2.0 V, V_{OL} = – 0.8 V).
13. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
14. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
15. These parameters are referenced to $\overline{CAS}$ leading edge in random write cycles and to $\overline{WRITE}$ leading edge in delayed write or read-modify-write cycles.
16. t_{WCS}, t_{CWD}, and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min), the cycle is a read-write cycle and the data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
17. t_{off} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

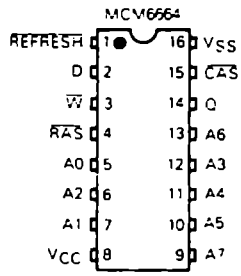
PIN ASSIGNMENT COMPARISON

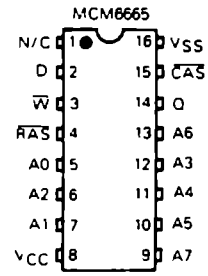












PIN VARIATIONS

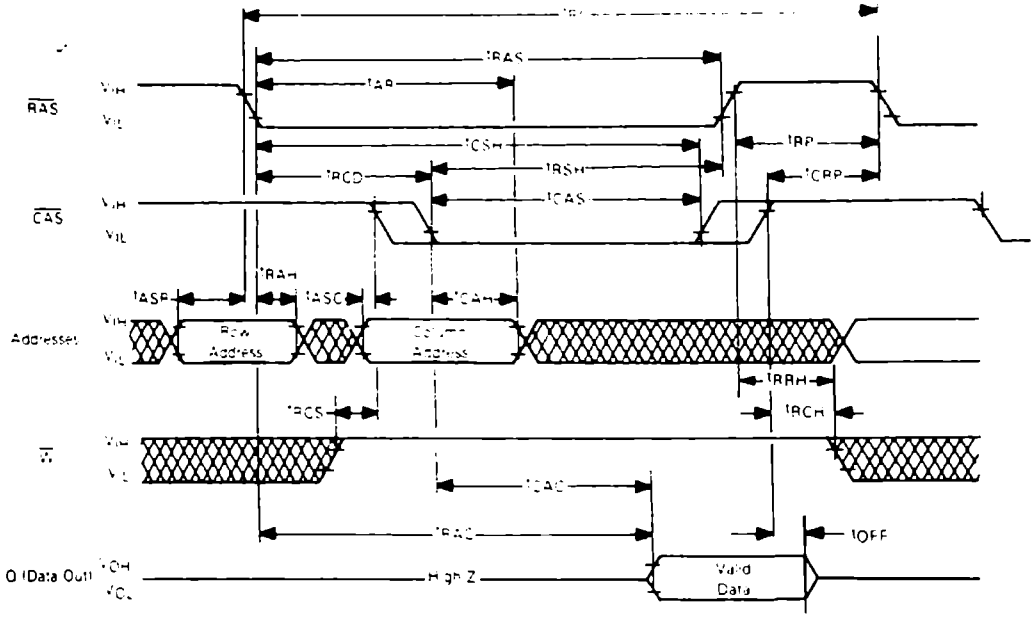
Pin Number	MCM4116	MCM4516	MCM4517	MCM6632	MCM6663	MCM6664	MCM6665
1	V_{BB} (−5 V)	$\overline{\text{REFRESH}}$	N/C	$\overline{\text{REFRESH}}$	N/C	$\overline{\text{REFRESH}}$	N/C
8	V_{DD} (+12 V)	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}
9	V_{CC} (+5 V)	N/C	N/C	A7	A7	A7	A7

ORDERING INSTRUCTIONS

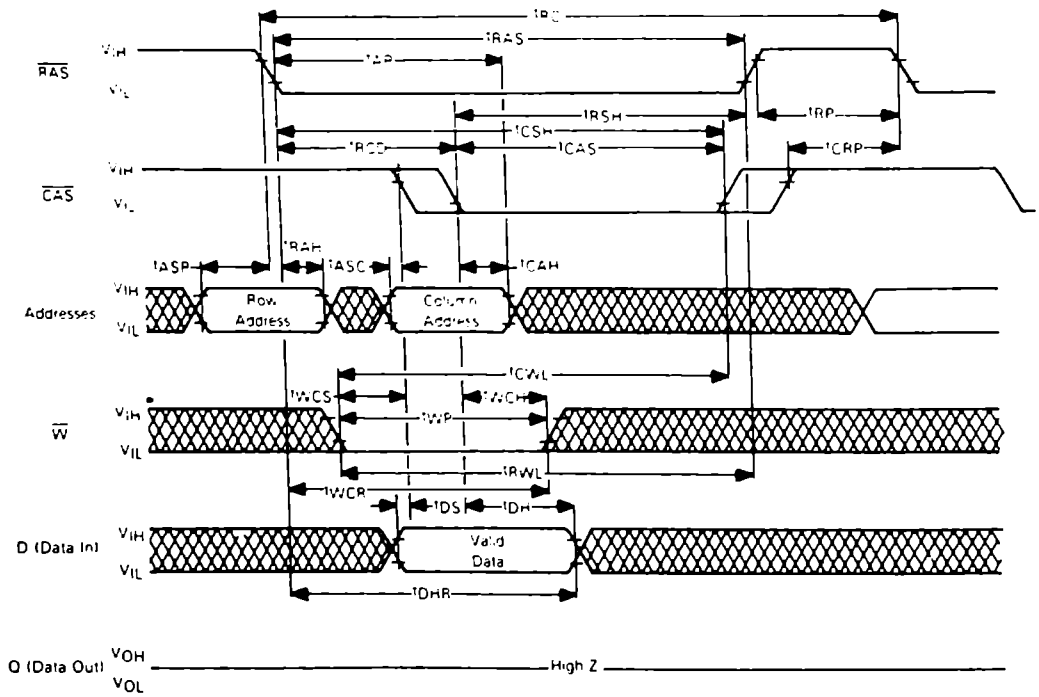
PART NUMBER	DESCRIPTION	SPEED	MARKING*
MCM6633L15	32K RAM Sidebraze Package "L"	150	66330L15/66331L15
MCM66330L15		150	66330L15
MCM66331L15		150	66331L15
MCM6633L20		200	66330L20/66331L20
MCM66330L20		200	66330L20
MCM66331L20		200	66331L20

*MCM66330L20 = Tie A7 $\overline{\text{CAS}}$ (A15) Low "0"
MCM66331L20 = Tie A7 $\overline{\text{CAS}}$ (A15) High "1"

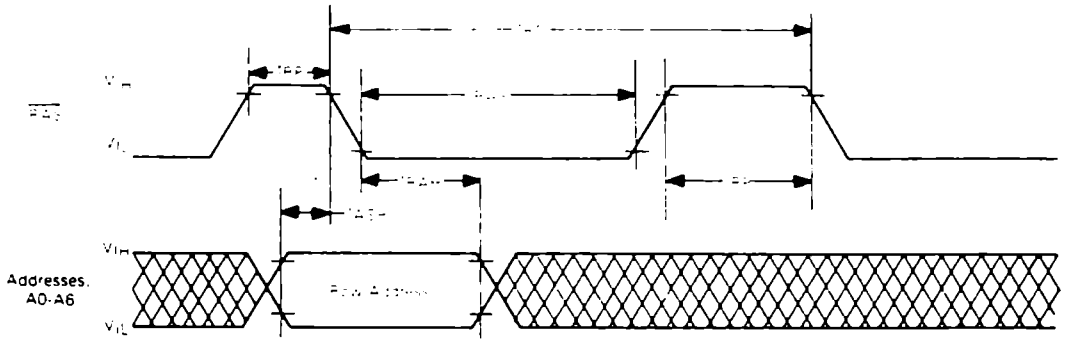
READ CYCLE TIMING



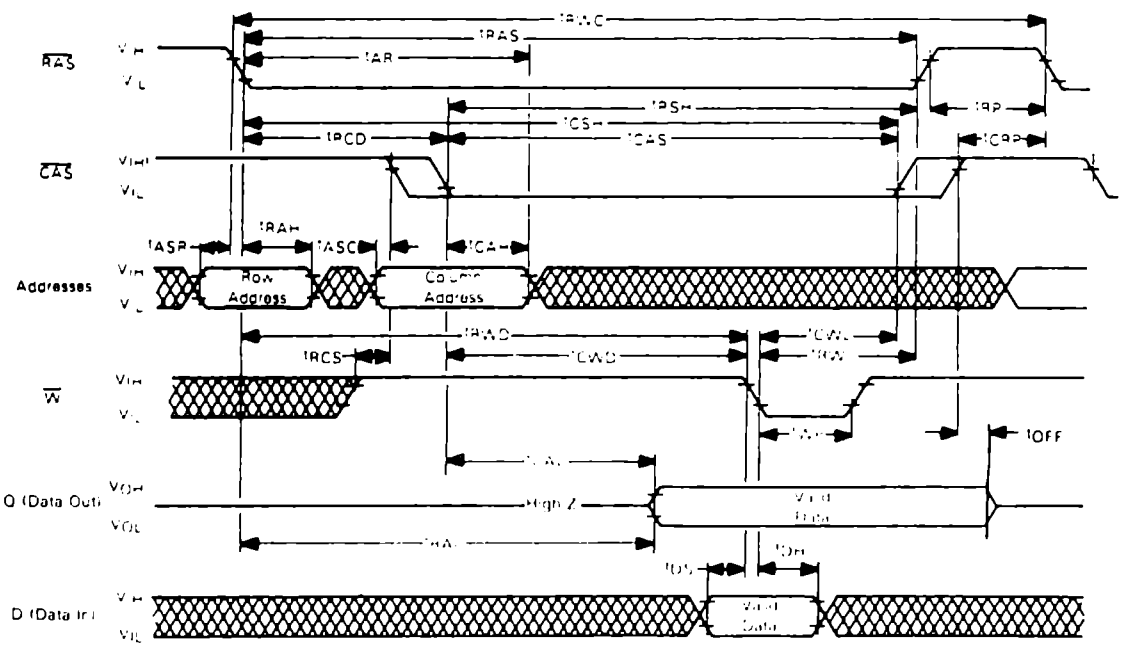
WRITE CYCLE TIMING



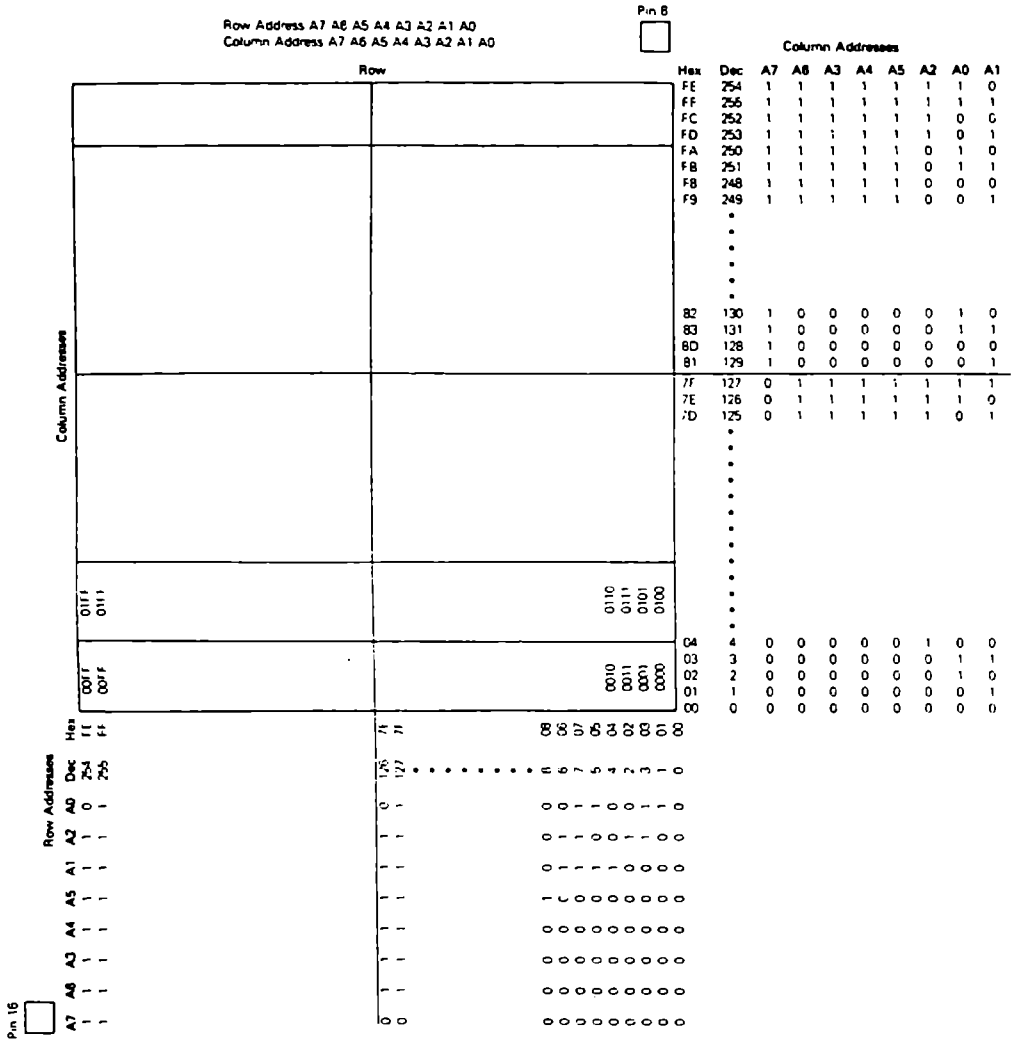
RAS ONLY REFRESH CYCLE
(Data-In and $\overline{\text{Write}}$ are Don't Care, $\overline{\text{CAS}}$ is HIGH)



READ-WRITE/READ-MODIFY-WRITE CYCLE



MCM6665 BIT ADDRESS MAP



$\overline{\text{Data Stored}} = D_{in} \bullet A_{0X} \bullet A_{1Y}$

Column Address A1	Row Address A0	Data Stored
0	0	Inverted
0	1	True
1	0	True
1	1	Inverted

MOTOROLA

MCM6664

65,536-BIT DYNAMIC RAM

The MCM6664 is a 65,536 bit, high-speed, dynamic Random-Access Memory. Organized as 65,536 one-bit words and fabricated using HMOS high-performance N-channel silicon-gate technology. This new breed of 5-volt only dynamic RAM combines high performance with low cost and improved reliability.

By multiplexing row- and column-address inputs, the MCM6664 requires only eight address lines and permits packaging in standard 16-pin dual-in-line packages. Complete address decoding is done on chip with address latches incorporated. Data out is controlled by $\overline{CAS}$ allowing for greater system flexibility.

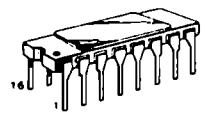
All inputs and outputs, including clocks, are fully TTL compatible. The MCM6664 incorporates a one-transistor cell design and dynamic storage techniques. In addition to the $\overline{RAS}$-only refresh mode, refresh control function available on pin 1 provides automatic and self-refresh modes.

- Organized as 65,536 Words of 1 Bit
- Single +5 V Operation
- Fast 150 ns Operation
- Low Power Dissipation
  - 275 mW Maximum (Active)
  - 30 mW Maximum (Standby)
- Three-State Data Output
- Internal Latches for Address and Data Input
- Early-Write Common I/O Capability
- 16K Compatible 128-Cycle, 2 ms Refresh
- Control on Pin 1 for Automatic and Self Refresh
- $\overline{RAS}$-only Refresh Mode
- $\overline{CAS}$ Controlled Output
- Upward Pin Compatible from the 16K RAM (MCM4116)

MOS

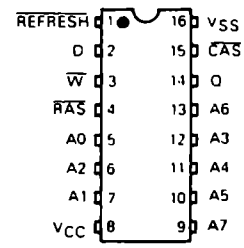
(N-CHANNEL, SILICON-GATE)

65,536-BIT DYNAMIC RANDOM ACCESS MEMORY



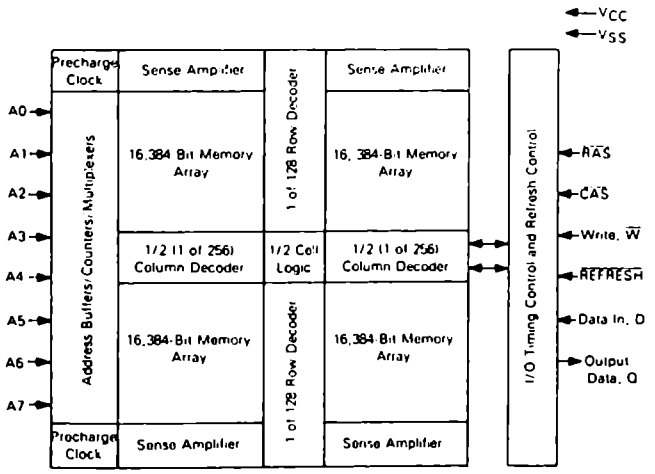
L SUFFIX
CERAMIC PACKAGE
CASE 690

PIN ASSIGNMENT



PIN NAMES	
$\overline{REFRESH}$	Refresh
A0-A7	Address Input
D	Data In
Q	Data Out
$\overline{W}$	Read/Write Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
V_{CC}	Power (+5 V)
V_{SS}	Ground

BLOCK DIAGRAM



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields, however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

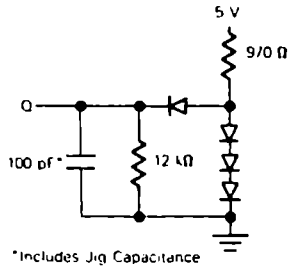
DS9822/9-80

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS} (except V_{CC})	V_{in}, V_{out}	−2 to +7	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{in}, V_{out}	−1 to +7	V
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Power Dissipation	P_D	1.0	W
Data Out Current	I_{out}	50	mA

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

FIGURE 1 — OUTPUT LOAD



*Includes Jig Capacitance

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted.)

RECOMMENDED OPERATING CONDITIONS

Parameter		Symbol	Min	Typ	Max	Unit	Notes
Supply Voltage	MCM6664-15, -20	V_{CC}	4.5	5.0	5.5	V	1
		V_{SS}	0	0	0	V	1
Logic 1 Voltage, All Inputs		V_{IH}	2.4	–	V_{CC} + 1	V	1
Logic 0 Voltage, All Inputs		V_{IL}	−2.0	–	0.8	V	1

DC CHARACTERISTICS

Characteristic	Symbol	Min	Max	Units	Notes
V_{CC} Power Supply Current (t_{RC} min)	I_{CC1}	–	50	mA	4
Standby V_{CC} Power Supply Current	I_{CC2}	–	5	mA	5
V_{CC} Power Supply Current: During $\overline{RAS}$ Only Refresh Cycles	I_{CC3}		40	mA	–
Input Leakage Current (any input except $\overline{REFRESH}$; $V_{SS} \le V_{in} \le V_{CC}$)	$I_{I(L)}$	–	10	μA	–
$\overline{REFRESH}$ Input Current ($V_F = V_{SS}$)	I_F		125	μA	
Output Leakage Current ($\overline{CAS}$ at logic 1, $0 \le V_{out} \le 5.5$)	$I_{O(L)}$		10	μA	
Output Logic 1 Voltage @ I_{out} = −4 mA	V_{OH}	2.4	–	V	
Output Logic 0 Voltage @ I_{out} = 4 mA	V_{OL}	–	0.4	V	

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, V_{CC} = 5 V, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Typ	Max	Units	Notes
Input Capacitance (A0–A7, D)	C_{I1}	4	5	pF	7
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$)	C_{I2}	8	10	pF	7
Output Capacitance (Q) ($\overline{CAS}$ = V_{IH} to disable output)	C_O	5	7	pF	7

AC OPERATING CONDITIONS AND CHARACTERISTICS

(See Notes 2, 3, 6 and Figure 1)

(Read, Write, and Read-Modify-Write Cycles)

(Full Operating Voltage and Temperature Range Unless Otherwise Noted)

Parameter	Symbol	MCM6664-15		MCM6664-20		Units	Notes
		Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RC}	300		350		ns	8, 9
Read-Write Cycle Time	t_{RWC}	300		350		ns	8, 9
Access Time from Row Address Strobe	t_{RAC}	–	150	–	200	ns	10, 12
Access Time from Column Address Strobe	t_{CAC}	–	75	–	110	ns	11, 12
Output Buffer and Turn-Off Delay	t_{OFF}	0	30	0	40	ns	18
Row Address Strobe Precharge Time	t_{RP}	120	–	140	–	ns	–
Row Address Strobe Pulse Width	t_{RAS}	150	10000	200	10000	ns	
Column Address Strobe Pulse Width	t_{CAS}	75	10000	110	10000	ns	–
Row to Column Strobe Lead Time	t_{RCD}	30	75	35	90	ns	13
Row Address Setup Time	t_{ASR}	0		0		ns	–
Row Address Hold Time	t_{RAH}	25		30		ns	–
Column Address Setup Time	t_{ASC}	0		0		ns	
Column Address Hold Time	t_{CAH}	45		55		ns	–
Column Address Hold Time Referenced to $\overline{RAS}$	t_{AR}	120		155		ns	–
Transition Time (Rise and Fall)	t_T	3	50	3	50	ns	6

AC OPERATING CONDITIONS AND CHARACTERISTICS

(See Notes 2, 3, 6, and Figure 1)

(Read, Write, and Read Modify Write Cycles)

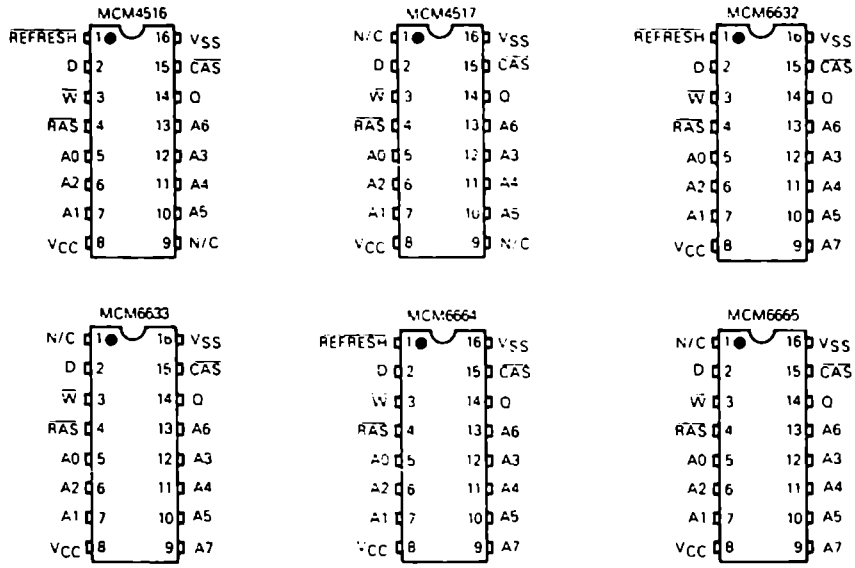
(Full Operating Voltage and Temperature Range Unless Otherwise Noted)

Parameter	Symbol	MCM6664-15		MCM6664-20		Units	Notes
		Min	Max	Min	Max		
Read Command Setup Time	t_{RCS}	0	-	0		ns	-
Read Command Hold Time	t_{RCH}	10		10		ns	14
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	30		35		ns	14
Write Command Hold Time	t_{WCH}	45	-	55	-	ns	-
Write Command Hold Time Referenced to $\overline{RAS}$	t_{WCR}	120		155		ns	-
Write Command Pulse Width	t_{WP}	45		55	-	ns	-
Write Command to Row Strobe Lead Time	t_{RWL}	45	-	55	-	ns	-
Write Command to Column Strobe Lead Time	t_{CWL}	45	-	55	-	ns	-
Data in Setup Time	t_{DS}	0	-	0	-	ns	15
Data in Hold Time	t_{DH}	45	-	55	-	ns	15
Data in Hold Time Referenced to $\overline{RAS}$	t_{DHR}	120		155	-	ns	-
Column to Row Strobe Precharge Time	t_{CRP}	10	-	-10		ns	-
$\overline{RAS}$ Hold Time	t_{RSH}	75	-	110	-	ns	-
Refresh Period	t_{RFSH}		2.0	-	2.0	ms	-
$\overline{WRITE}$ Command Setup Time	t_{WCS}	-10	-	-10	-	ns	16
$\overline{CAS}$ to $\overline{WRITE}$ Delay	t_{CWD}	45	-	55	-	ns	16
$\overline{RAS}$ to $\overline{WRITE}$ Delay	t_{RWD}	125		160	-	ns	16
$\overline{CAS}$ Hold Time	t_{CSH}	150	-	200	-	ns	-
$\overline{RAS}$ to $\overline{REFRESH}$ Delay	t_{RFD}	0	-	0	-	ns	-
$\overline{REFRESH}$ Period (Battery Backup Model)	t_{FBP}	2000	-	2000	-	ns	-
$\overline{REFRESH}$ to $\overline{RAS}$ Precharge Time (Battery Backup Model)	t_{FBR}	390	-	460	-	ns	-
$\overline{REFRESH}$ Cycle Time (Auto Pulse Mode)	t_{FC}	330	-	360	-	ns	-
$\overline{REFRESH}$ Pulse Period (Auto Period Mode)	t_{FP}	60	2000	60	2000	ns	-
$\overline{REFRESH}$ to $\overline{RAS}$ Setup Time (Auto Pulse Mode)	t_{FSR}	30	-	30	-	ns	-
$\overline{REFRESH}$ to $\overline{RAS}$ Delay Time (Auto Pulse Mode)	t_{FRD}	390	-	460	-	ns	-
$\overline{REFRESH}$ Inactive Time	t_{FI}	30	-	30	-	ns	-
$\overline{RAS}$ to $\overline{REFRESH}$ Lead Time	t_{FRL}	390	-	460	-	ns	-

NOTES

1. All voltages referenced to V_{SS}
2. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}
3. An initial pause of 100 µs is required after power up followed by any 8 $\overline{RAS}$ cycles before proper device operation is guaranteed.
4. Current is a function of cycle rate and output loading; maximum current is measured at the fastest cycle rate with the output open.
5. Output is disabled (open-circuit) and $\overline{RAS}$ and $\overline{CAS}$ are both at a logic 1.
6. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transmit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
7. Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: $C = \frac{I\Delta t}{\Delta V}$
8. The specifications for t_{RC} (min), and t_{RWC} (min) are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
9. AC measurements assume t_T = 5.0 ns
10. Assumes that $t_{RCD} \leq t_{RCD}$ (Max)
11. Assumes that $t_{RCD} \geq t_{RCD}$ (Max)
12. Measured with a current load equivalent to 2 TTL (-200 µA, -4 mA) loads and 100 pF (V_{OH} = 2.0 V, V_{OL} = -0.8 V).
13. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
14. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
15. These parameters are referenced to $\overline{CAS}$ leading edge in random write cycles and to $\overline{WRITE}$ leading edge in delayed write or read-modify-write cycles.
16. t_{WCS}, t_{CWD}, and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min), the cycle is a read-write cycle and the data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
17. Addresses, data in and $\overline{WRITE}$ are don't care. Data-out depends on the state of $\overline{CAS}$. If $\overline{CAS}$ remains low, the previous output will remain valid. $\overline{CAS}$ is allowed to make an active to inactive transition during the pin #1 refresh cycle. When $\overline{CAS}$ is brought high, the output will assume a high impedance state.
18. t_{off} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

PIN ASSIGNMENT COMPARISON



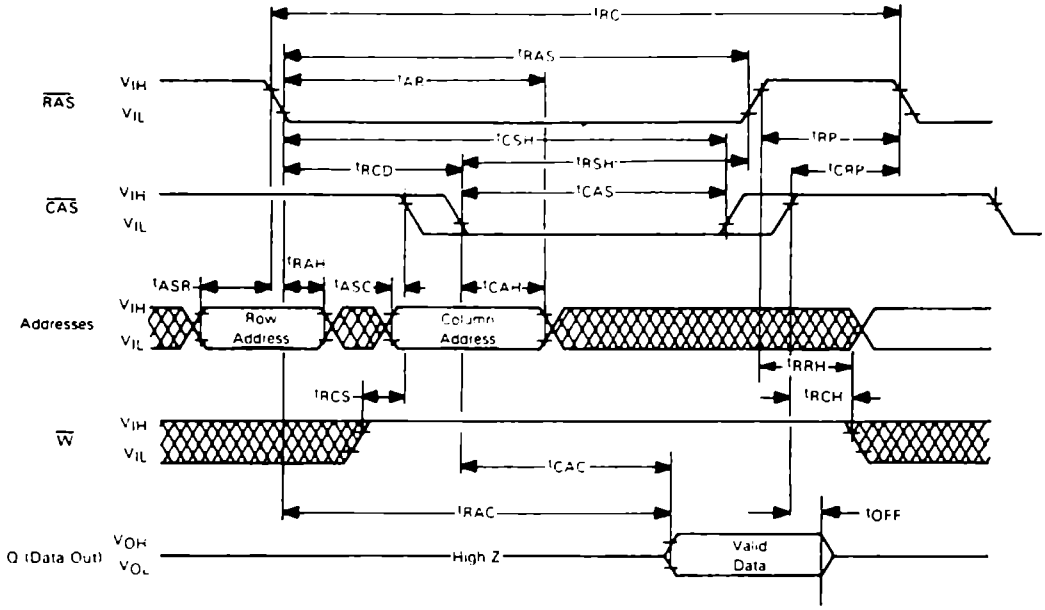
PIN VARIATIONS

Pin Number	MCM4116	MCM4516	MCM4517	MCM6632	MCM6663	MCM6664	MCM6665
1	V_{BB} (−5 V)	$\overline{\text{REFRESH}}$	N/C	$\overline{\text{REFRESH}}$	N/C	$\overline{\text{REFRESH}}$	N/C
8	V_{DD} (+12 V)	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}
9	V_{CC} (+5 V)	N/C	N/C	A7	A7	A7	A7

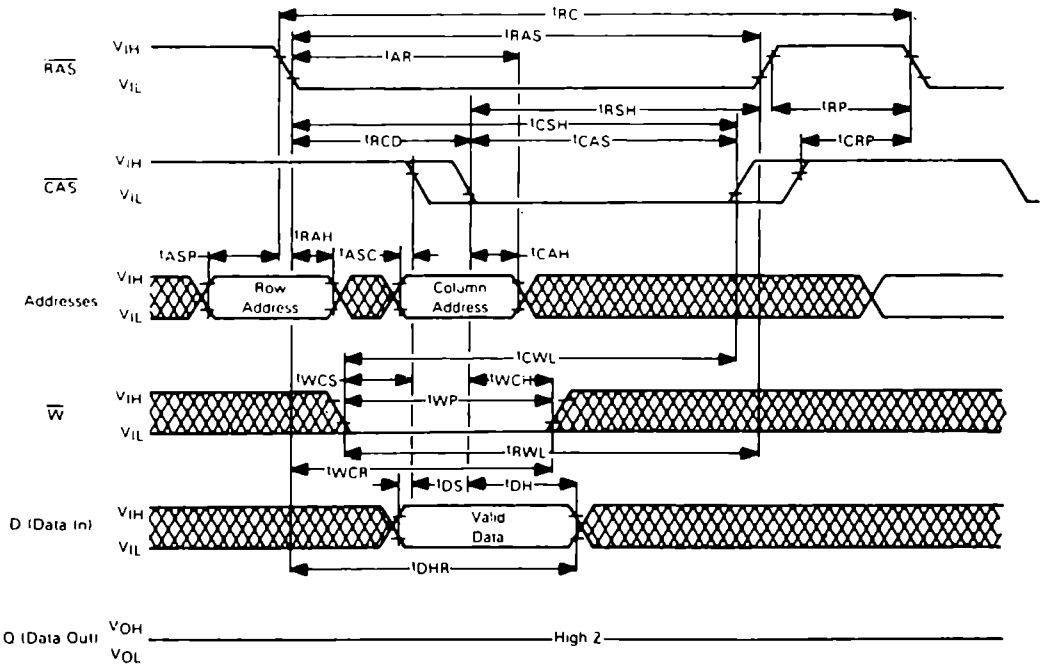
On-Chip Refresh Features/Benefits

Reduce System Refresh Controller Design Problem
Reduce System Parts Count
Reduce System Noise Increasing System Reliability
Reduce System Power During Refresh

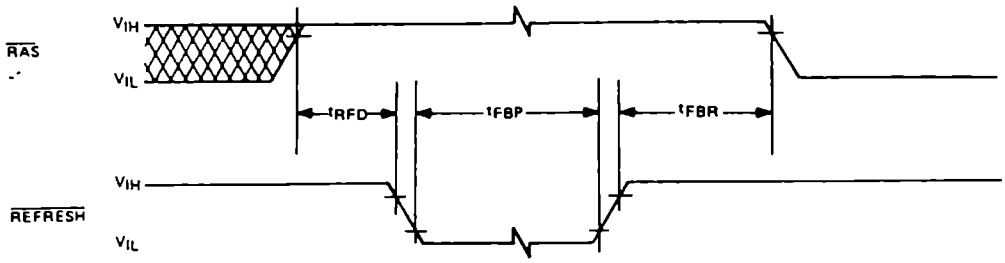
READ CYCLE TIMING



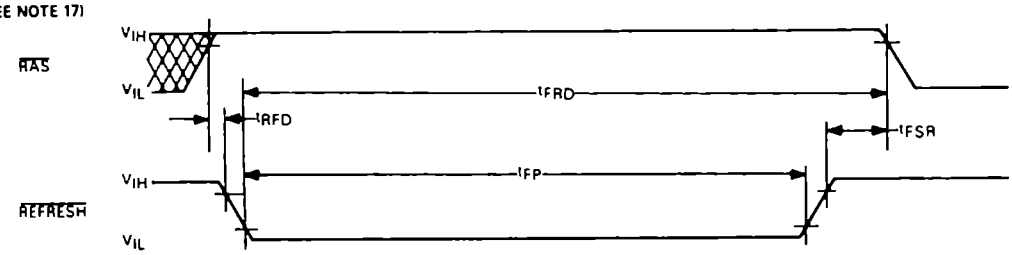
WRITE CYCLE TIMING



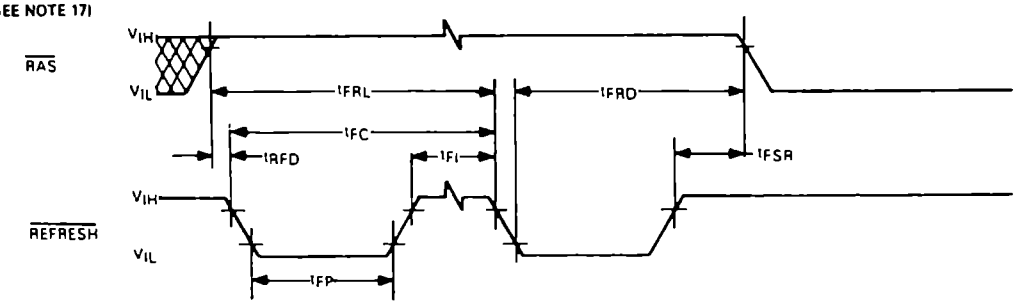
SELF REFRESH MODE (Battery Backup)
(SEE NOTE 17)



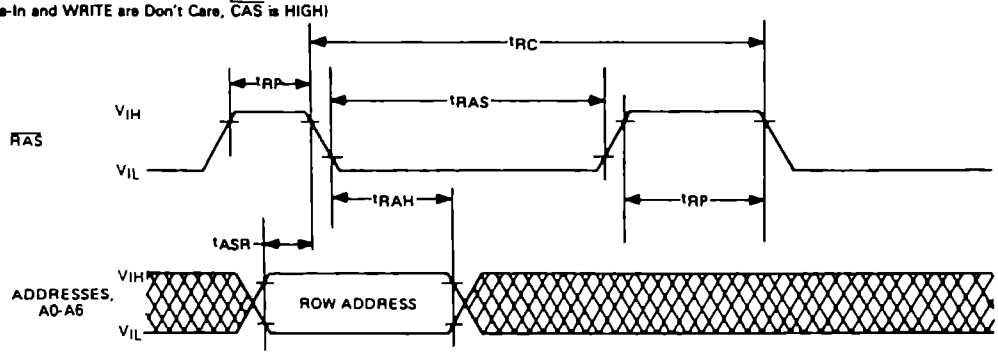
AUTOMATIC PULSE REFRESH CYCLE — SINGLE PULSE
(SEE NOTE 17)



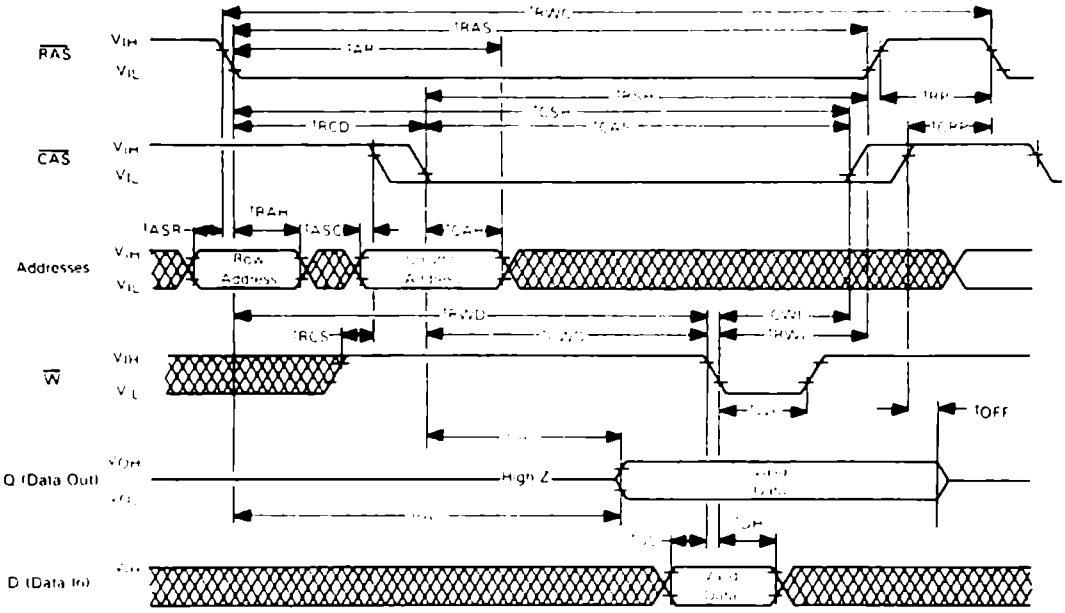
AUTOMATIC PULSE REFRESH CYCLE — MULTIPLE PULSE
(SEE NOTE 17)



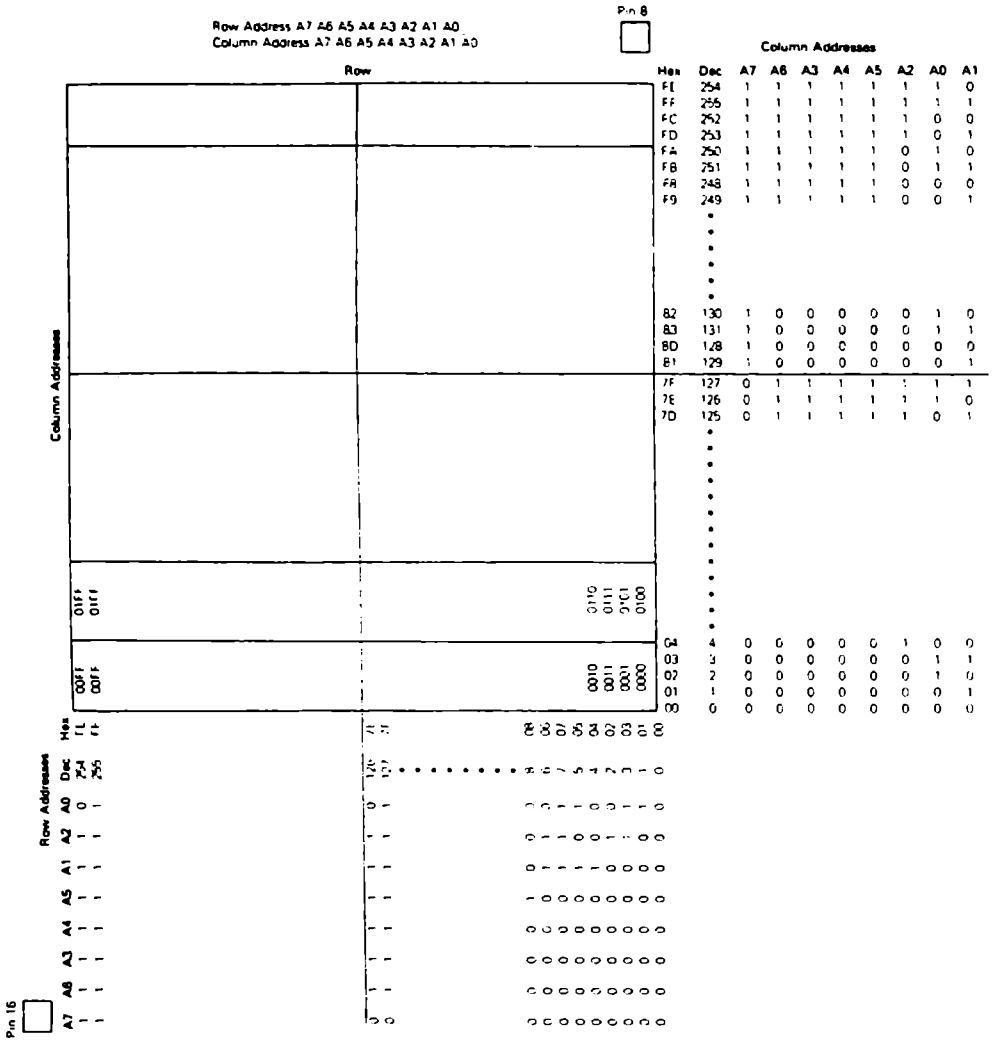
RAS-ONLY REFRESH CYCLE
(Data-In and WRITE are Don't Care, $\overline{CAS}$ is HIGH)



READ-WRITE/READ-MODIFY WRITE CYCLE



MCM6664 BIT ADDRESS MAP



$\overline{\text{Data Stored}} = D_{in} \bullet A_{0X} \bullet A_{1Y}$

Column Address A1	Row Address A0	Data Stored
0	0	Inverted
0	1	True
1	0	True
1	1	Inverted

MOTOROLA

MCM6665

65,536-BIT DYNAMIC RAM

The MCM6665 is a 65,536 bit, high speed, dynamic Random-Access Memory. Organized as 65,536 one-bit words and fabricated using HMOS high-performance N-channel, silicon-gate technology. This new breed of 5-volt only dynamic RAM combines high performance with low cost and improved reliability.

By multiplexing row- and column address inputs, the MCM6665 requires only eight address lines and permits packaging in standard 16 pin dual-in-line packages. Complete address decoding is done on-chip with address latches incorporated. Data out is controlled by $\overline{CAS}$ allowing for greater system flexibility.

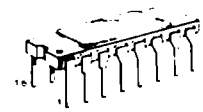
All inputs and outputs, including clocks, are fully TTL compatible. The MCM6665 incorporates a one-transistor cell design and dynamic storage techniques.

- Organized as 65,536 Words of 1 Bit
- Single +5 V Operation
- Fast 150 ns Operation
- Low Power Dissipation
  - 275 mW Maximum (Active)
  - 30 mW Maximum (Standby)
- Three-State Data Output
- Internal Latches for Address and Data Input
- Early-Write Common I/O Capability
- 16K Compatible 128 Cycle, 2 ms Refresh
- $\overline{RAS}$-only Refresh Mode
- $\overline{CAS}$ Controlled Output
- Upward Pin Compatible from the 16K RAM (MCM4116, MCM4517)

MOS

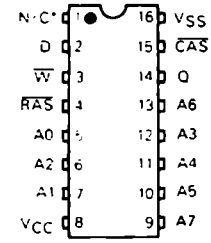
(N-CHANNEL, SILICON-GATE)

65,536-BIT DYNAMIC RANDOM ACCESS MEMORY



L SUFFIX
CERAMIC PACKAGE
CASE 690

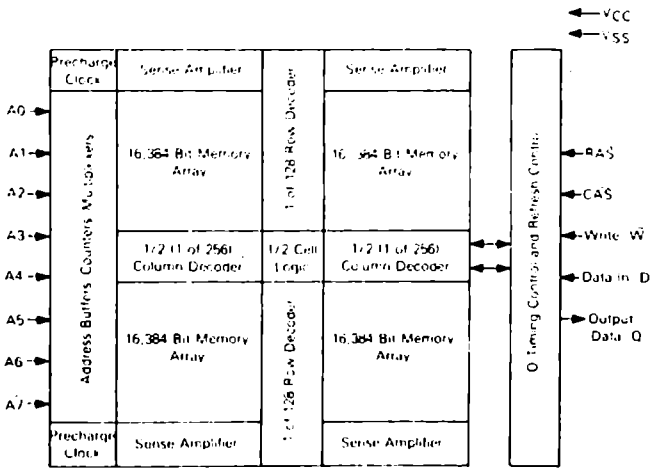
PIN ASSIGNMENT



*For maximum compatibility with MCM6632 and MCM6664 a V_{CC} trace should go to pin #1.

PIN NAMES	
A0-A7	Address Input
D	Data In
Q	Data Out
$\overline{W}$	Read/Write Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
V_{CC}	Power (+5 V)
V_{SS}	Ground

BLOCK DIAGRAM



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields, however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

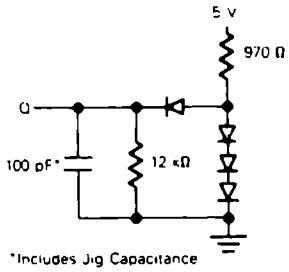
DS9824/9-80

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS} (Except V_{CC})	V_{in}, V_{out}	−2 to +7	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{in}, V_{out}	−1 to +7	V
Storage Temperature Range	T_{stg}	−65 to +150	°C
Power Dissipation	P_D	1	W
Data Out Current	I_{out}	50	mA

NOTE Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

FIGURE 1 – OUTPUT LOAD



*Includes Jig Capacitance

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted.)

RECOMMENDED OPERATING CONDITIONS

Parameter		Symbol	Min	Typ	Max	Unit	Notes
Supply Voltage	MCM6665L15/MCM6665L20	V_{CC}	4.5	5.0	5.5	V	1
	MCM6665L15-5/MCM6665L20-5	V_{CC}	4.75	5.0	5.25	V	1
		V_{SS}	0	0	0	V	
Logic 1 Voltage, All Inputs		V_{IH}	2.4	–	V_{CC}+1	V	1
Logic 0 Voltage, All Inputs		V_{IL}	−2.0	–	0.8	V	1

DC CHARACTERISTICS (Full Operating Voltage and Temperature Ranges Unless Otherwise Noted)

Characteristic	Symbol	Min	Max	Units	Notes
V_{CC} Power Supply Current (t_{RC} min)	I_{CC1}	–	50	mA	4
Standby V_{CC} Power Supply Current	I_{CC2}	–	5	mA	5
V_{CC} Power Supply Current During $\overline{RAS}$ Only Refresh Cycles	I_{CC3}	–	40	mA	–
Input Leakage Current (any input) ($0 \le V_{in} \le 5.5$) (Except Pin 1)	$I_{I(LI)}$	–	10	µA	–
Output Leakage Current ($0 \le V_{out} \le 5.5$) ($\overline{CAS}$ at Logic 1)	$I_{O(LI)}$	–	10	µA	–
Output Logic 1 Voltage @ I_{out} = −4 mA	V_{OH}	2.4	–	V	–
Output Logic 0 Voltage @ I_{out} = 4 mA	V_{OL}	–	0.4	V	–

AC OPERATING CONDITIONS AND CHARACTERISTICS

(See Notes 2, 3, 6, and Figure 1)

(Read, Write, and Read-Modify-Write Cycles)

(Full Operating Voltage and Temperature Range Unless Otherwise Noted)

Parameter	Symbol	MCM6665-15		MCM6665-20		Units	Notes
		Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RC}	300	–	350	–	ns	8, 9
Read Write Cycle Time	t_{RWC}	300	–	350	–	ns	8, 9
Access Time from Row Address Strobe	t_{RAC}	–	150	–	200	ns	10, 12
Access Time from Column Address Strobe	t_{CAC}	–	75	–	110	ns	11, 12
Output Buffer and Turn-Off Delay	t_{OFF}	0	30	0	40	ns	17
Row Address Strobe Precharge Time	t_{RP}	120	–	140	–	ns	–
Row Address Strobe Pulse Width	t_{RAS}	150	10000	200	10000	ns	–
Column Address Strobe Pulse Width	t_{CAS}	75	10000	110	10000	ns	–
Row to Column Strobe Lead Time	t_{RCD}	30	75	35	90	ns	13
Row Address Setup Time	t_{ASR}	0	–	0	–	ns	–
Row Address Hold Time	t_{RAH}	25	–	30	–	ns	–
Column Address Setup Time	t_{ASC}	0	–	0	–	ns	–
Column Address Hold Time	t_{CAH}	45	–	55	–	ns	–
Column Address Hold Time Referenced to $\overline{RAS}$	t_{AR}	120	–	155	–	ns	–
Transition Time (Rise and Fall)	t_T	3	50	3	50	ns	6

AC OPERATING CONDITIONS AND CHARACTERISTICS

(See Notes 2, 3, 6, and Figure 1)

(Read, Write, and Read-Modify-Write Cycles)

(Full Operating Voltage and Temperature Range Unless Otherwise Noted)

Parameter	Symbol	MCM6665-15		MCM6665-20		Units	Notes
		Min	Max	Min	Max		
Read Command Setup Time	t_{RCS}	0	–	0	–	ns	–
Read Command Hold time	t_{RCH}	10	–	10	–	ns	14
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	30	–	35	–	ns	14
Write Command Hold Time	t_{WCH}	45	–	55	–	ns	–
Write Command Hold Time Referenced to $\overline{RAS}$	t_{WCR}	120	–	155	–	ns	–
Write Command Pulse Width	t_{WP}	45	–	55	–	ns	–
Write Command to Row Strobe Lead Time	t_{RWL}	45	–	55	–	ns	–
Write Command to Column Strobe Lead Time	t_{CWL}	45	–	55	–	ns	–
Data in Setup Time	t_{DS}	0	–	0	–	ns	15
Data in Hold Time	t_{DH}	45	–	55	–	ns	15
Data in Hold Time Referenced to $\overline{RAS}$	t_{DHR}	120	–	155	–	ns	–
Column to Row Strobe Precharge Time	t_{CRP}	– 10	–	– 10	–	ns	–
$\overline{RAS}$ Hold Time	t_{RSH}	75	–	110	–	ns	–
Refresh Period	t_{RFSH}	–	2.0	–	2.0	ms	–
$\overline{WRITE}$ Command Setup Time	t_{WCS}	– 10	–	– 10	–	ns	16
$\overline{CAS}$ to $\overline{WRITE}$ Delay	t_{CWD}	45	–	55	–	ns	16
$\overline{RAS}$ to $\overline{WRITE}$ Delay	t_{RWD}	125	–	160	–	ns	16
$\overline{CAS}$ Hold Time	t_{CSH}	150	–	200	–	ns	–

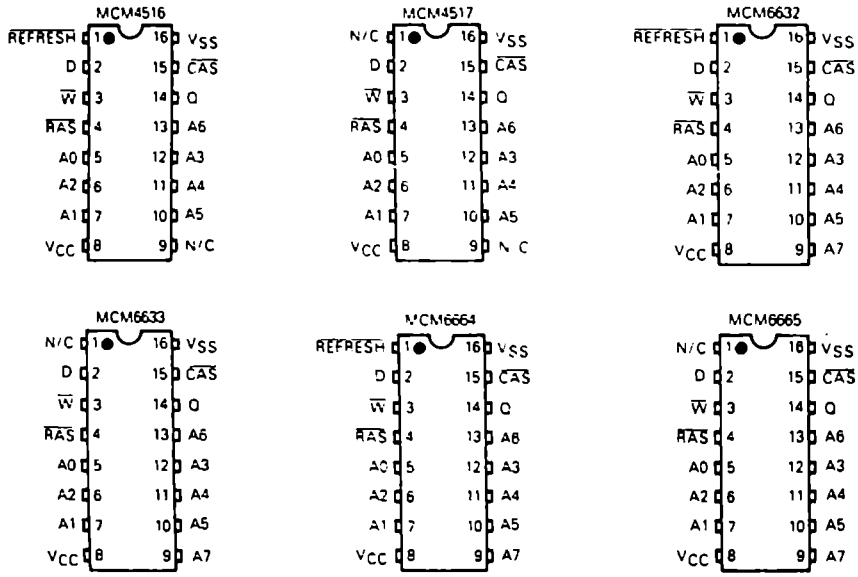
CAPACITANCE (f = 1.0 MHz, T_A = 25°C, V_{CC} = 5 V. Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Typ	Max	Units	Notes
Input Capacitance (A0-A7), D	C_{I1}	4	5	pF	7
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	C_{I2}	8	10	pF	7
Output Capacitance (Q) ($\overline{CAS}$ = V_{IH} to disable output)	C_O	5	7	pF	7

NOTES

1. All voltages referenced to V_{SS}
2. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
3. An initial pause of 100 µs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation guaranteed.
4. Current is a function of cycle rate and output loading; maximum current is measured at the fastest cycle rate with the output open.
5. Output is disabled (open circuit) and $\overline{RAS}$ and $\overline{CAS}$ are both at a logic 1.
6. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
7. Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation $C = \frac{I\Delta_t}{\Delta V}$
8. The specifications for t_{RC} (min), and t_{RWC} (min) are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
9. AC measurements assume t_T = 5.0 ns.
10. Assumes that $t_{RCD} \leq t_{RCD}$ (max).
11. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
12. Measured with a current load equivalent to 2 TTL loads (+ 200 µA, – 4 mA) and 100 pF (V_{OH} = 2.0 V, V_{OL} = – 0.8 V).
13. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
14. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
15. These parameters are referenced to $\overline{CAS}$ leading edge in random write cycles and to $\overline{WRITE}$ leading edge in delayed write or read-modify-write cycles.
16. t_{WCS}, t_{CWD}, and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min), the cycle is a read-write cycle and the data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
17. t_{off} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

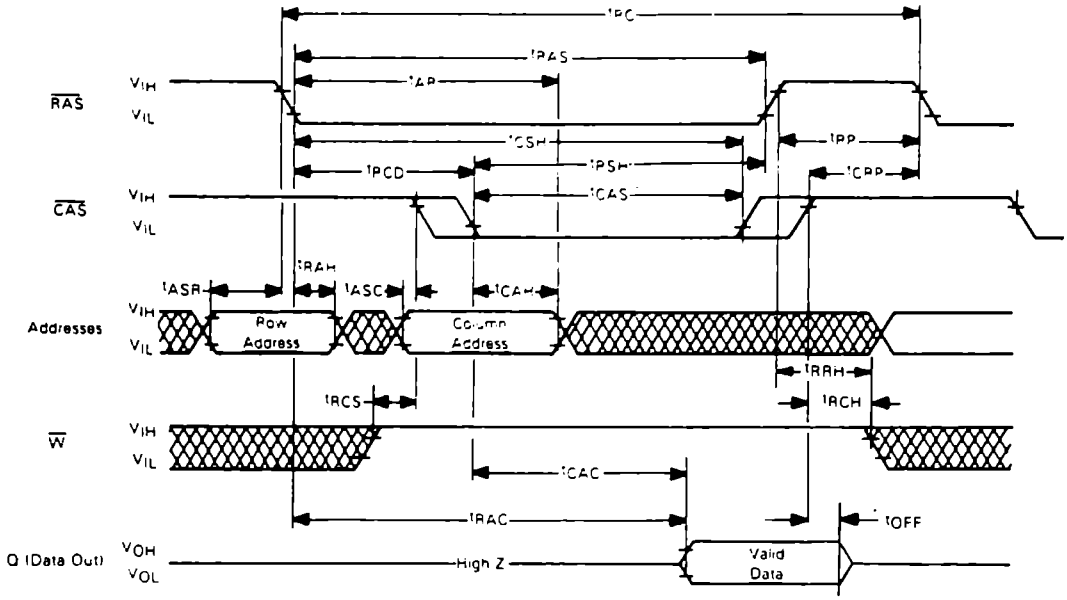
PIN ASSIGNMENT COMPARISON



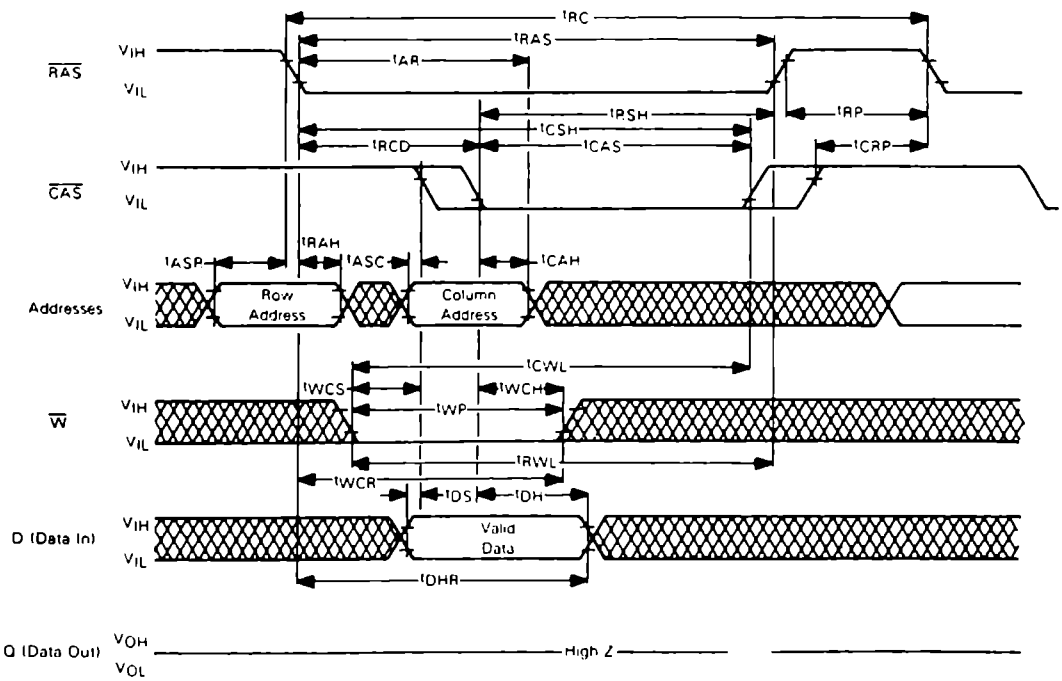
PIN VARIATIONS

Pin Number	MCM4116	MCM4516	MCM4517	MCM6632	MCM6633	MCM6664	MCM6665
1	V_{BB} (−5 V)	REFRESH	N/C	REFRESH	N/C	REFRESH	N/C
8	V_{DD} (+12 V)	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}
9	V_{CC} (+5 V)	N/C	N/C	A7	A7	A7	A7

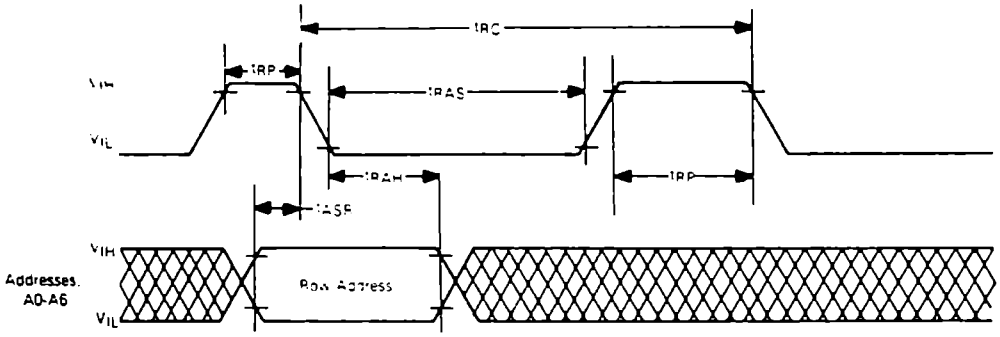
READ CYCLE TIMING



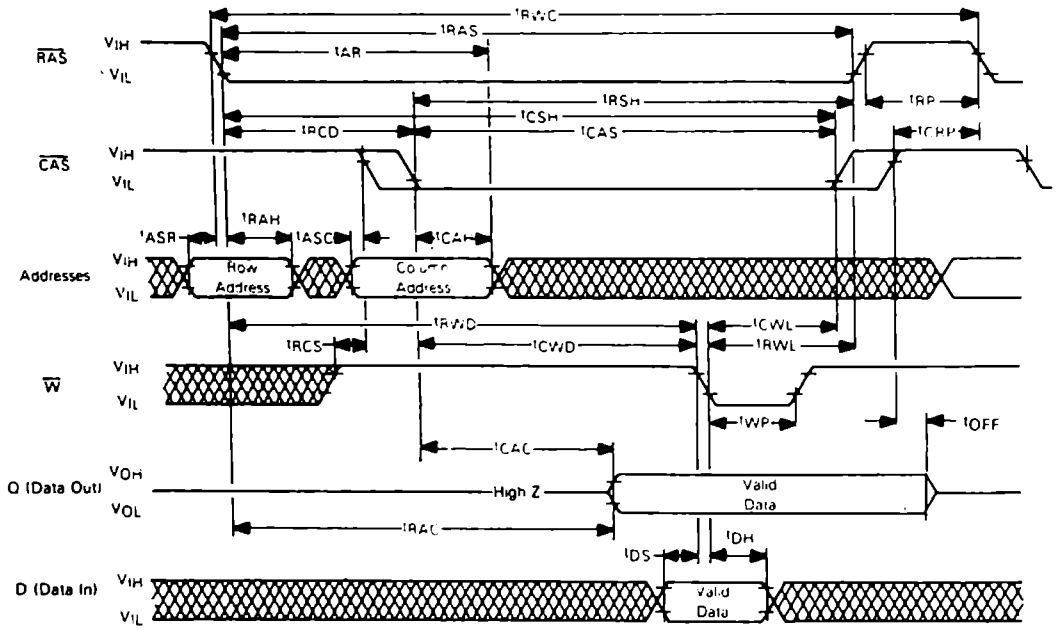
WRITE CYCLE TIMING



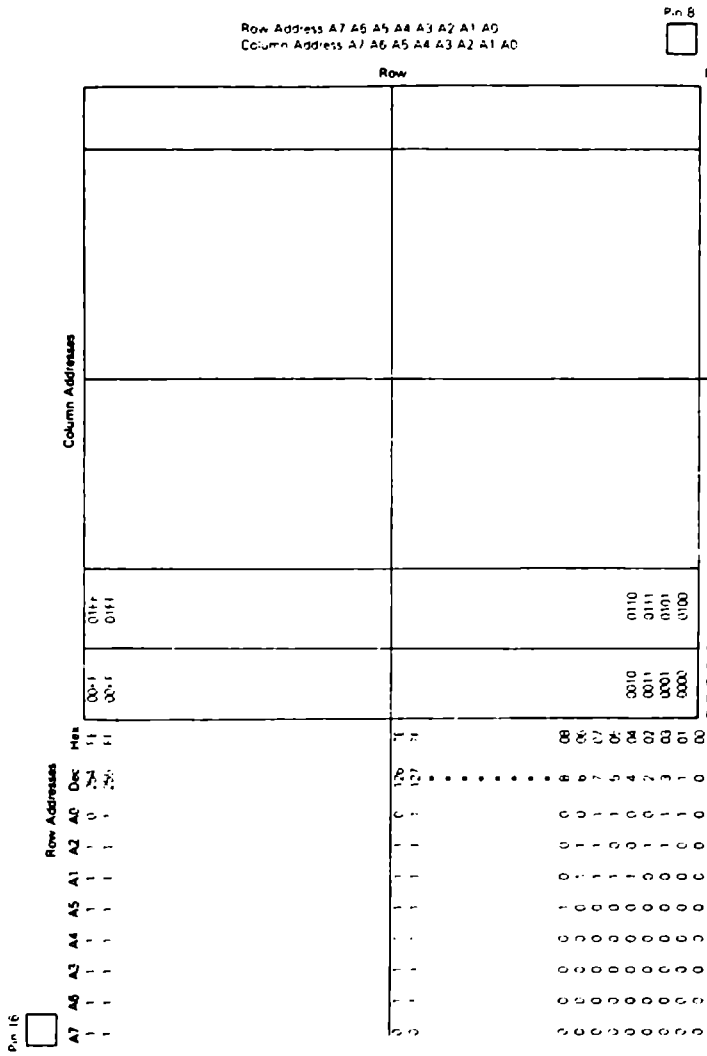
RAS-ONLY REFRESH CYCLE
(Data-in and Write are Don't Care, $\overline{CAS}$ is HIGH)



READ-WRITE/READ-MODIFY-WRITE CYCLE



MCM6665 BIT ADDRESS MAP



Hex	Dec	A7	A6	A3	A4	A5	A2	A0	A1
FE	254	1	1	1	1	1	1	1	0
FF	255	1	1	1	1	1	1	1	1
FC	252	1	1	1	1	1	1	0	0
FD	253	1	1	1	1	1	1	0	1
FA	250	1	1	1	1	1	0	1	0
FB	251	1	1	1	1	1	0	1	1
F8	248	1	1	1	1	1	0	0	0
F9	249	1	1	1	1	1	0	0	1
•	•								
•	•								
•	•								
82	130	1	0	0	0	0	0	1	0
83	131	1	0	0	0	0	0	1	1
80	128	1	0	0	0	0	0	0	0
81	129	1	0	0	0	0	0	0	1
7F	127	0	1	1	1	1	1	1	1
7E	126	0	1	1	1	1	1	1	0
7D	125	0	1	1	1	1	1	0	1
•	•								
•	•								
•	•								
04	4	0	0	0	0	0	1	0	0
03	3	0	0	0	0	0	0	1	1
02	2	0	0	0	0	0	0	1	0
01	1	0	0	0	0	0	0	0	1
00	0	0	0	0	0	0	0	0	0

$\overline{\text{Data Stored}} = D_{in} \bullet A_{0X} \bullet A_{1Y}$

Column Address A1	Row Address A0	Data Stored
0	0	Inverted
0	1	True
1	0	True
1	1	Inverted

MOTOROLA

MCM6665L25

65,536-BIT DYNAMIC RAM

The MCM6665 is a 65,536 bit, high speed, dynamic Random-Access Memory. Organized as 65,536 one-bit words and fabricated using HMOS high performance N-channel silicon-gate technology. This new breed of 5-volt only dynamic RAM combines high performance with low cost and improved reliability.

By multiplexing row- and column-address inputs, the MCM6665 requires only eight address lines and permits packaging in standard 16 pin dual-in-line packages. Complete address decoding is done on chip with address latches incorporated. Data out is controlled by $\overline{CAS}$ allowing for greater system flexibility.

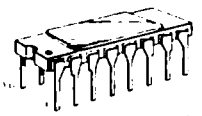
All inputs and outputs, including clocks, are fully TTL compatible. The MCM6665 incorporates a one-transistor cell design and dynamic storage techniques.

- Organized as 65,536 Words of 1 Bit
- Single +5 V Operation
- 250 ns Operation
- Low Power Dissipation
  - 275 mW Maximum (Active)
  - 30 mW Maximum (Standby)
- Three State Data Output
- Internal Latches for Address and Data Input
- Early-Write Output Capability
- 16K Compatible 128 Cycle, 2 ms Refresh
- $\overline{RAS}$ only Refresh Mode
- $\overline{CAS}$ Controlled Output Providing Latched or Unlatched Data
- Upward Pin Compatible from the 16K RAM (MCM4116, MCM4516, MCM4517)

MOS

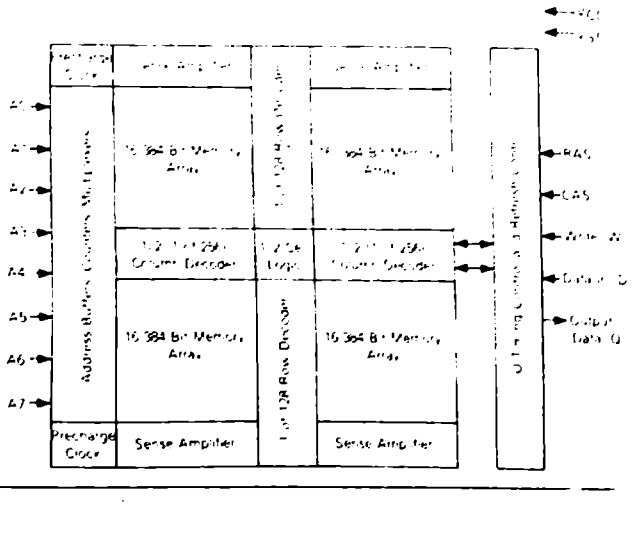
N-CHANNEL, SILICON-GATE

65,536-BIT
DYNAMIC RANDOM ACCESS
MEMORY

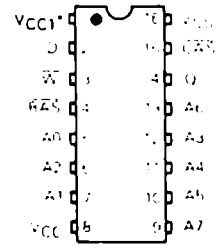


L SUFFIX

BLOCK DIAGRAM



PIN ASSIGNMENT



*V_{CC1} does not draw any current but must be tied to V_{CC} to inactivate internal refresh circuitry

PIN NAMES	
A0-A7	Address Input
D	Data In
Q	Data Out
$\overline{W}$	Read/Write Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
V_{CC}	Power (+5 V)
V_{SS}	Ground

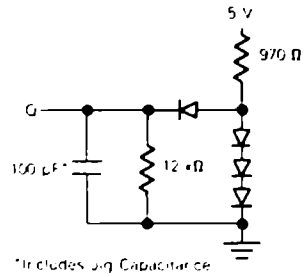
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS} (Except V_{CC})	V_{in}, V_{out}	−2 to +7	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{in}, V_{out}	−1 to +7	V
Operating Temperature Range	T_A	0 to +50	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Power Dissipation	P_D	1.0	W
Data Out Current	I_{out}	50	mA

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

FIGURE 1 – OUTPUT LOAD



*Includes Jig Capacitance

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted.)

RECOMMENDED OPERATING CONDITIONS

Parameter		Symbol	Min	Typ	Max	Unit	Notes
Supply Voltage	MCM6665L25	V_{CC} V_{SS}	4.5 0	5.0 0	5.5 0	V	1
Logic 1 Voltage, All Inputs		V_{IH}	2.4	–	V_{CC} + 1.0	V	1
Logic 0 Voltage, All Inputs		V_{IL}	−2.0	–	0.8	V	1

DC CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit	Notes
V_{CC} Power Supply Current (t_{RC} min)	I_{CC}	–	50	mA	4
Standby V_{CC} Power Supply Current	I_{CC2}	–	5	mA	5
V_{CC} Power Supply Current During $\overline{RAS}$ Only Refresh Cycles	I_{CC3}	–	40	mA	–
Input Leakage Current (any input) ($0 \le V_{in} \le 5.5$) (Except Pin 1)	$I_{I(L)}$	–	10	µA	–
Input Leakage Current (Pin 1) ($V_{in} = V_{CC}$)	$I_{I(L)}$	–	10	µA	–
Output Leakage Current ($0 \le V_{out} \le 5.5$) (Except Pin 1)	$I_{O(L)}$	–	10	µA	5, 6
Output Logic 1 Voltage @ I_{out} = −4 mA	V_{OH}	2.4	–	V	–
Output Logic 0 Voltage @ I_{out} = 4 mA	V_{OL}	–	0.4	V	–

AC OPERATING CONDITIONS AND CHARACTERISTICS

(Full Operating Voltage and Temperature Range Unless Otherwise Noted)
(See Notes 2, 3, 9, 14)
(Read, Write, and Read-Modify-Write Cycles)

Parameter	Symbol	Min	Max	Unit	Notes
Random Read or Write Cycle Time	t_{RC}	450	–	ns	8, 9
Read Write Cycle Time	t_{RWC}	450	–	ns	8, 9
Access Time from Row Address Strobe	t_{RAC}	–	250	ns	10, 12
Access Time from Column Address Strobe	t_{CAC}	–	145	ns	11, 12
Output Buffer and Turn-Off Delay	t_{OFF}	0	50	ns	17
Row Address Strobe Precharge Time	t_{RP}	190	–	ns	–
Row Address Strobe Pulse Width	t_{RAS}	250	10000	ns	–
Column Address Strobe Pulse Width	t_{CAS}	145	10000	ns	–
Row to Column Strobe Lead Time	t_{RCD}	55	105	ns	13
Row Address Setup Time	t_{ASR}	0	–	ns	–
Row Address Hold Time	t_{RAH}	45	–	ns	–
Column Address Setup Time	t_{ASC}	0	–	ns	–
Column Address Hold Time	t_{CAH}	75	–	ns	–
Column Address Hold Time Referenced to $\overline{RAS}$	t_{AR}	200	–	ns	–
Transition Time (Rise and Fall)	t_T	3.0	50	ns	6

AC OPERATING CONDITIONS AND CHARACTERISTICS

(Full Operating Voltage and Temperature Range Unless Otherwise Noted)
(See Notes 2, 3, 9, 14)
(Read, Write, and Read-Modify-Write Cycles)

Parameter	Symbol	Min	Max	Units	Notes
Read Command Setup Time	t_{RCS}	0	–	ns	–
Read Command Hold Time	t_{RCH}	10	–	ns	14
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	40	–	ns	14
Write Command Hold Time	t_{WCH}	75	–	ns	–
Write Command Hold Time Referenced to $\overline{RAS}$	t_{WCR}	200	–	ns	–
Write Command Pulse Width	t_{WP}	70	–	ns	–
Write Command to Row Strobe Lead Time	t_{RWL}	70	–	ns	–
Write Command to Column Strobe Lead Time	t_{CWL}	70	–	ns	–
Data in Setup Time	t_{DS}	0	–	ns	15
Data in Hold Time	t_{DH}	75	–	ns	15
Data in Hold Time Referenced to $\overline{RAS}$	t_{DHR}	200	–	ns	–
Column to Row Strobe Precharge Time	t_{CRP}	−10	–	ns	–
$\overline{RAS}$ Hold Time	t_{RSH}	145	–	ns	–
Refresh Period	t_{RFSH}	–	2.0	ms	–
$\overline{WRITE}$ Command Setup Time	t_{WCS}	−10	–	ns	16
$\overline{CAS}$ to $\overline{WRITE}$ Delay	t_{CWD}	70	–	ns	16
$\overline{RAS}$ to $\overline{WRITE}$ Delay	t_{RWD}	195	–	ns	16
$\overline{CAS}$ Hold Time	t_{CSH}	250	–	ns	–

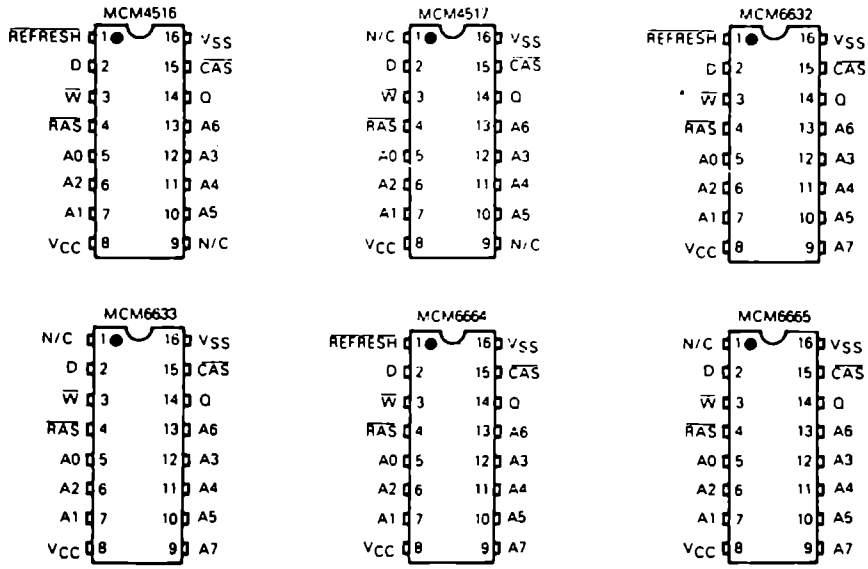
CAPACITANCE (f = 1.0 MHz, T_A = 25°C, V_{CC} = 5 V, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Typ	Max	Units	Notes
Input Capacitance (A0-A7), D	C_{I1}	4.0	5.0	pF	7
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	C_{I2}	8.0	10.0	pF	7
Output Capacitance (Q)	C_O	5.0	7.0	pF	7

NOTES

1. All voltages referenced to V_{SS}.
2. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
3. An initial pause of 100 µs is required after power up followed by any 8 $\overline{RAS}$ cycles before proper device operation is guaranteed.
4. Current is a function of cycle rate and output loading; maximum current is measured at the fastest cycle rate with the output open.
5. Output is disabled (open circuit) and $\overline{RAS}$ and $\overline{CAS}$ are held at a logic 1.
6. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
7. Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: $C = \frac{\Delta t}{\Delta V}$
8. The specifications for t_{RC} (min) and t_{RWC} (min) are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
9. AC measurements assume t_T = 5.0 ns.
10. Assumes that $t_{RCD} \le t_{RCD}$ (max).
11. Assumes that $t_{RCD} \ge t_{RCD}$ (min).
12. Measured with a current load equivalent to 2 TTL loads (+ 200 µA, − 4 mA) and 100 pF (V_{OH} = 2.0 V, V_{OL} = − 0.8 V).
13. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
14. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
15. These parameters are referenced to $\overline{CAS}$ leading edge in random write cycles and to $\overline{WRITE}$ leading edge in delayed write or read-modify-write cycles.
16. t_{WCS}, t_{CWD}, and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \ge t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle. If $t_{CWD} \ge t_{CWD}$ (min) and $t_{RWD} \ge t_{RWD}$ (min), the cycle is a read-write cycle and the data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
17. t_{off} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

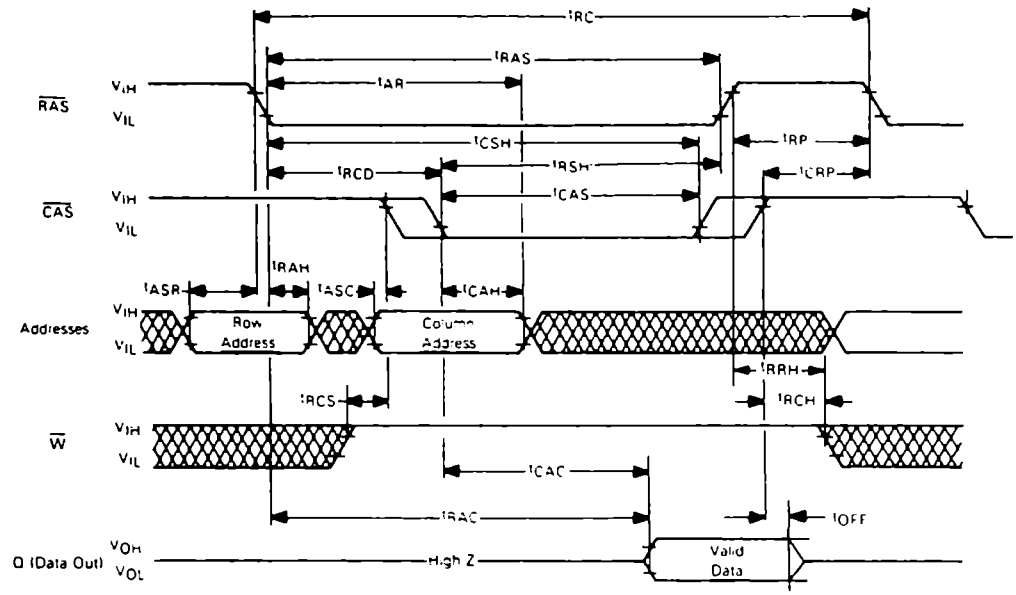
PIN ASSIGNMENT COMPARISON



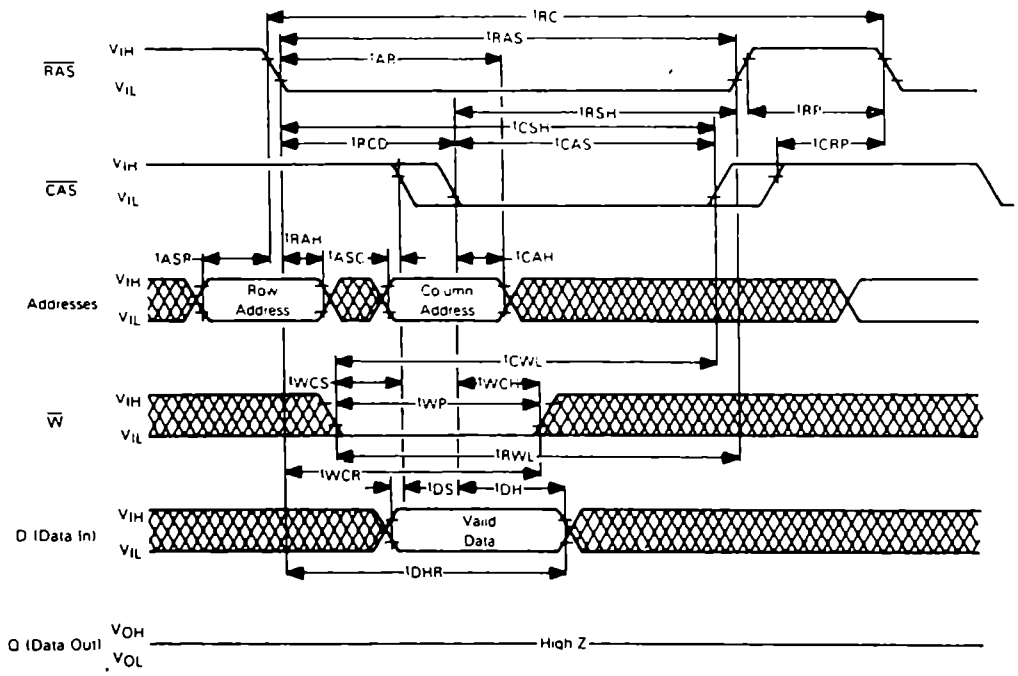
PIN VARIATIONS

Pin Number	MCM4116	MCM4516	MCM4517	MCM6632	MCM6633	MCM6664	MCM6665
1	V_{BB} (−5 V)	REFRESH	N/C	REFRESH	N/C	REFRESH	N/C
8	V_{DD} (+12 V)	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}
9	V_{CC} (+5 V)	N/C	N/C	A7	A7	A7	A7

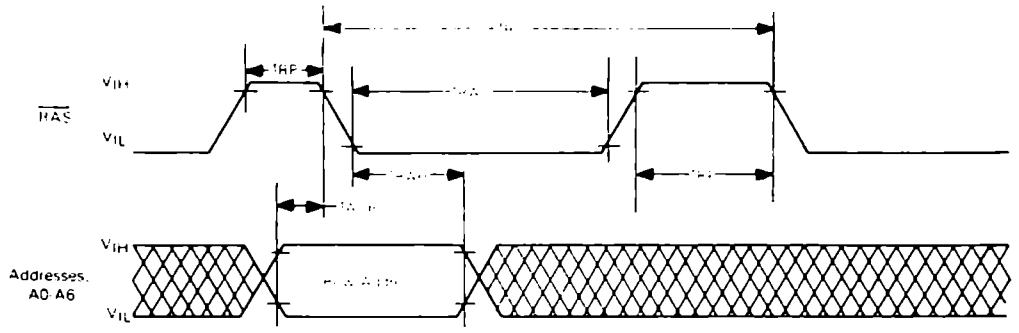
READ CYCLE TIMING



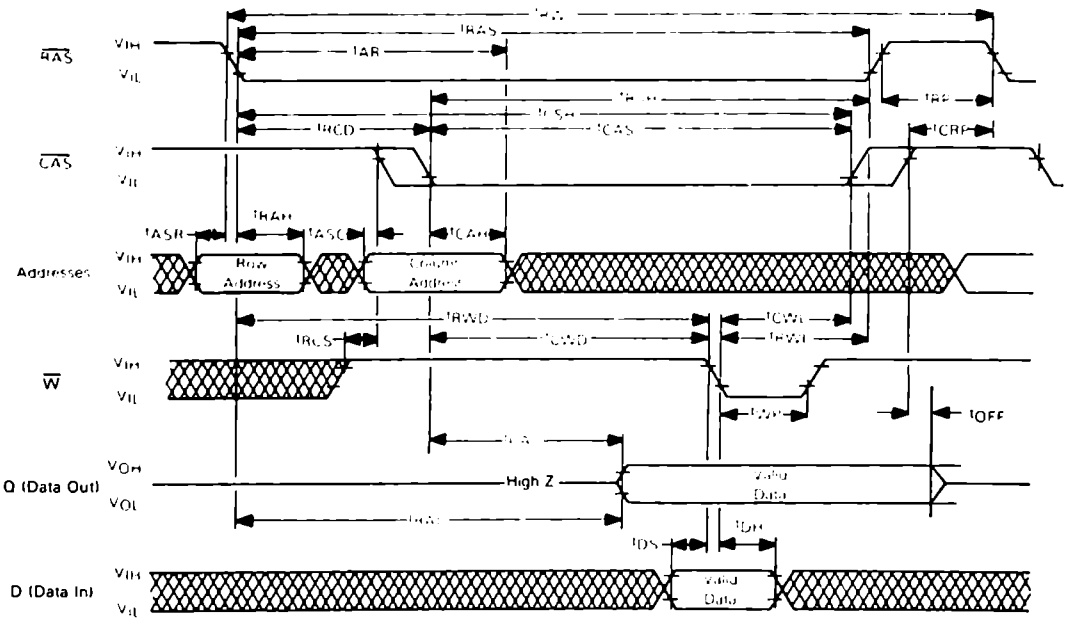
WRITE CYCLE TIMING



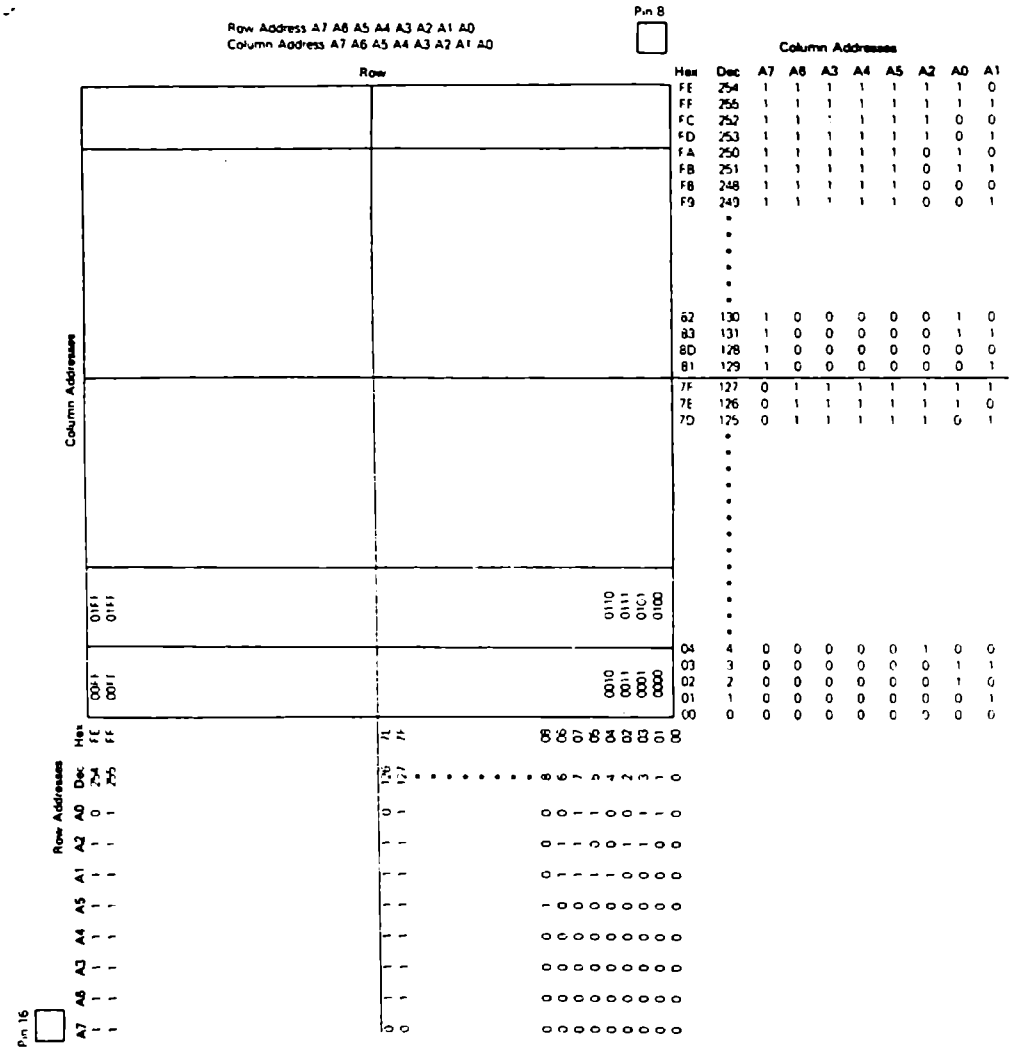
RAS ONLY REFRESH CYCLE
(Data-in and Write are Don't Care, $\overline{CAS}$ is HIGH)



READ-WRITE/READ-MODIFY-WRITE CYCLE



MCM6665 BIT ADDRESS MAP



$\overline{\text{Data Stored}} = D_{in} \bullet A_{0X} \bullet A_{1Y}$

Column Address A1	Row Address A0	Data Stored
0	0	Inverted
0	1	True
1	0	True
1	1	Inverted

MOTOROLA

MCM2114
MCM21L14

MOS

(N-CHANNEL, SILICON-GATE)

4096-BIT STATIC RANDOM ACCESS MEMORY

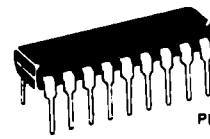
4096-BIT STATIC RANDOM ACCESS MEMORY

The MCM2114 is a 4096 bit random access memory fabricated with high density, high reliability N-channel silicon-gate technology. For ease of use, the device operates from a single power supply, is directly compatible with TTL and DTL, and requires no clocks or refreshing because of fully static operation. Data access is particularly simple since address setup times are not required. The output data has the same polarity as the input data.

The MCM2114 is designed for memory applications where simple interfacing is the design objective. The MCM2114 is assembled in 18-pin dual-in-line packages with the industry standard pin-out. A separate chip select ($\overline{S}$) lead allows easy selection of an individual package when the three-state outputs are OR-tied.

The MCM2114 series has a maximum current of 100 mA. Low power versions (i.e., MCM21L14 series) are available with a maximum current of only 70 mA.

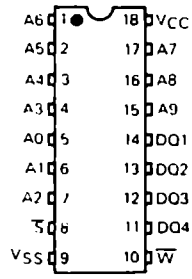
- 1024 Words by 4 Bit Organization
- Industry Standard 18-Pin Configuration
- Single +5 Volt Supply
- No Clock or Timing Strobe Required
- Fully Static, Cycle Time = Access Time
- Maximum Access Time
  - MCM2114-20/MCM21L14-20 200 ns
  - MCM2114-25/MCM21L14-25 250 ns
  - MCM2114-30/MCM21L14-30 300 ns
  - MCM2114-45/MCM21L14-45 450 ns
- Fully TTL Compatible
- Common Data Input and Output
- Three-State Outputs for OR-Ties
- Low Power Version Available



P SUFFIX
PLASTIC PACKAGE
CASE 707

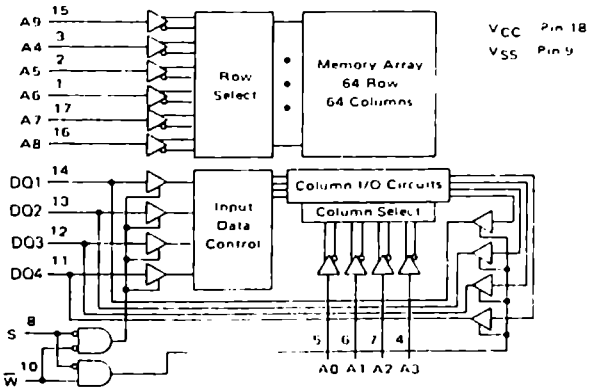
L SUFFIX
CERAMIC PACKAGE
CASE 680

PIN ASSIGNMENT



PIN NAMES	
A0-A9	Address Input
$\overline{W}$	Write Enable
$\overline{S}$	Chip Select
DQ1-DQ4	Data Input/Output
V_{CC}	Power (+5 V)
V_{SS}	Ground

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Value	Unit
Temperature Under Bias	- 10 to + 80	°C
Voltage on Any Pin With Respect to V_{SS}	- 0.5 to + 7.0	V
DC Output Current	5.0	mA
Power Dissipation	1.0	Watt
Operating Temperature Range	0 to + 70	°C
Storage Temperature Range	- 65 to + 150	°C

NOTE Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted.)

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
	V_{SS}	0	0	0	
Logic 1 Voltage, All Inputs	V_{IH}	2.0		6.0	V
Logic 0 Voltage, All Inputs	V_{IL}	- 0.5		0.8	V

DC CHARACTERISTICS

Parameter	Symbol	MCM2114			MCM21L14			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Load Current (All Input Pins, V_{in} = 0 to 5.5 V)	I_{LI}	-	-	10	-	-	10	µA
I/O Leakage Current ($\overline{S}$ = 2.4 V, V_{DO} = 0.4 V to V_{CC})	I_{LOI}			10		-	10	µA
Power Supply Current (V_{in} = 5.5 V, I_{DO} = 0 mA, T_A = 25°C)	I_{CC1}		80	95	-		65	mA
Power Supply Current (V_{in} = 5.5 V, I_{DO} = 0 mA, T_A = 0°C)	I_{CC2}	-		100			70	mA
Output Low Current (V_{OL} = 0.4 V)	I_{OL}	2.1	6.0		2.1	6.0		mA
Output High Current (V_{OH} = 2.4 V)	I_{OH}		- 1.4	1.0		- 1.4	- 1.0	mA

NOTE: Duration not to exceed 30 seconds.

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, periodically sampled rather than 100% tested)

Characteristic	Symbol	Max	Unit
Input Capacitance (V_{in} = 0 V)	C_{in}	5.0	pF
Input/Output Capacitance (V_{DO} = 0 V)	$C_{I/O}$	5.0	pF

Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: $C = I\Delta t/\Delta V$

AC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted.)

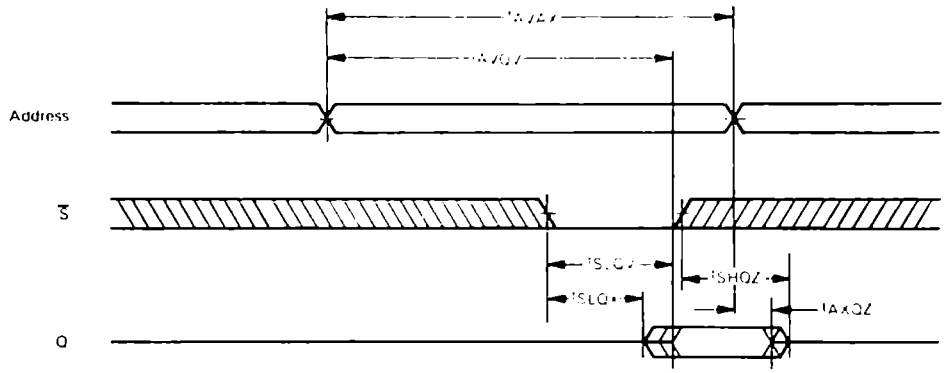
Input Pulse Levels 0.8 Volts to 2.4 Volts
Input Rise and Fall Times 10 ns
Input and Output Timing Levels 1.5 Volts
Output Load 1 TTL Gate and C_L = 100 pF

READ (NOTE 1), WRITE (NOTE 2) CYCLES

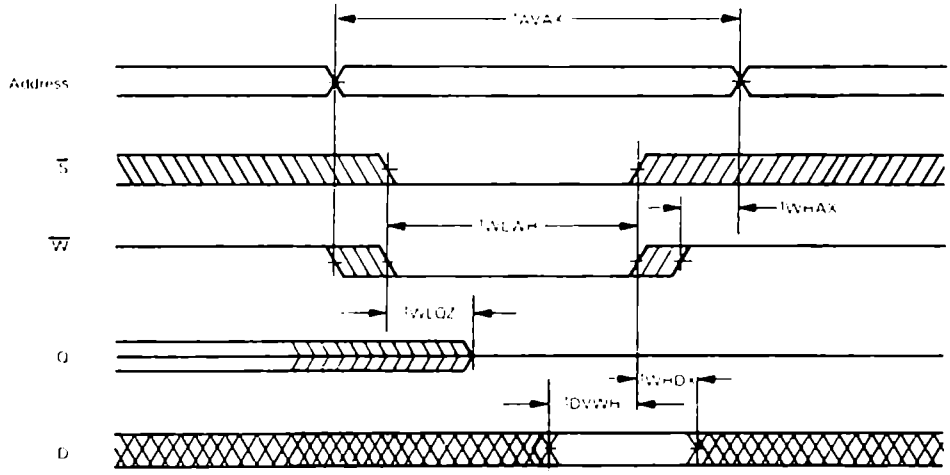
Parameter	Symbol	MCM2114-20 MCM21L14-20		MCM2114-25 MCM21L14-25		MCM2114-30 MCM21L14-30		MCM2114-45 MCM21L14-45		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Address Valid to Address Don't Care	t_{AVAX}	200		250		300		450		ns
Address Valid to Output Valid	t_{AVQV}		200		250		300		450	ns
Chip Select Low to Data Valid	t_{SLQV}		70		85		100		120	ns
Chip Select Low to Output Don't Care	t_{SLQX}	20		20		20		20		ns
Chip Select High to Output High Z	t_{SHQZ}		60		70		80		100	ns
Address Don't Care to Output High Z	t_{AXQZ}	60		60		60		60		ns
Write Low to Write High	t_{WLWH}	120		135		150		200		ns
Write High to Address Don't Care	t_{WHAX}	20		20		20		20		ns
Write Low to Output High Z	t_{WLQZ}		60		70		80		100	ns
Data Valid to Write High	t_{DVWH}	120		135		150		200		ns
Write High to Data Don't	t_{WHDX}	0		0		0		0		ns

NOTES 1. A Read occurs during the overlap of a low $\overline{S}$ and a high $\overline{W}$.
2. A Write occurs during the overlap of a low $\overline{S}$ and a low $\overline{W}$.

READ CYCLE TIMING ($\overline{W}$ HELD HIGH)



WRITE CYCLE TIMING (NOTE 3)



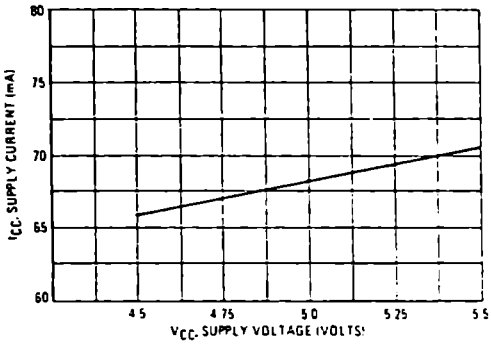
3. If the $\overline{S}$ low transition occurs simultaneously with the $\overline{W}$ low transition, the output buffers remain in a high impedance state.

WAVEFORMS

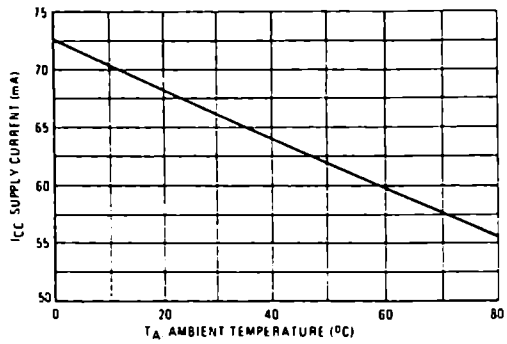
Waveform Symbol	Input	Output
	MUST BE VALID	WILL BE VALID
	CHANGE FROM H TO L	WILL CHANGE FROM H TO L
	CHANGE FROM L TO H	WILL CHANGE FROM L TO H
	DON'T CARE ANY CHANGE PERMITTED	CHANGING STATE UNKNOWN
		HIGH IMPEDANCE

TYPICAL CHARACTERISTICS

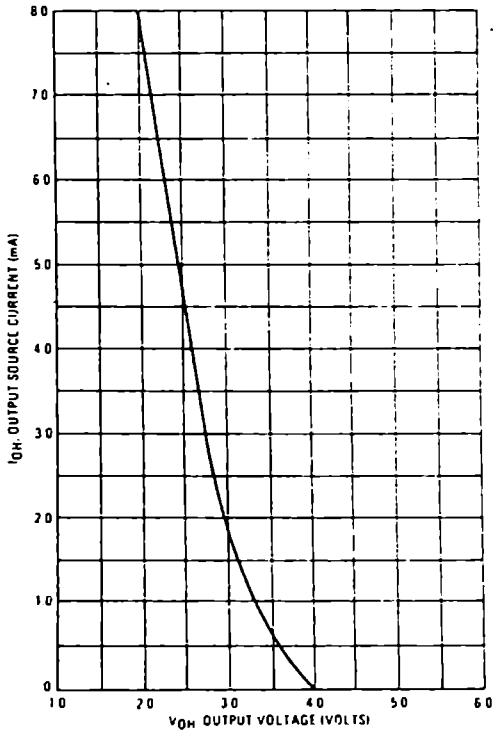
SUPPLY CURRENT versus SUPPLY VOLTAGE



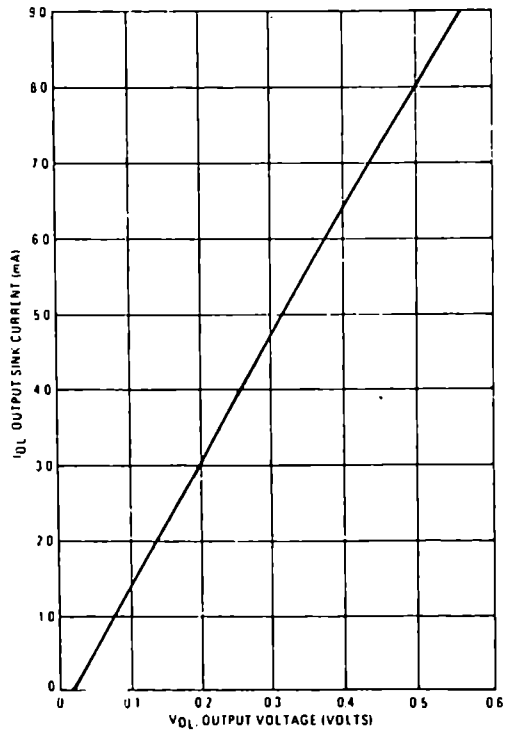
SUPPLY CURRENT versus AMBIENT TEMPERATURE



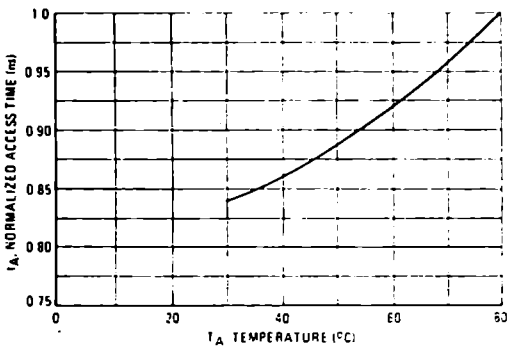
OUTPUT SOURCE CURRENT versus OUTPUT VOLTAGE



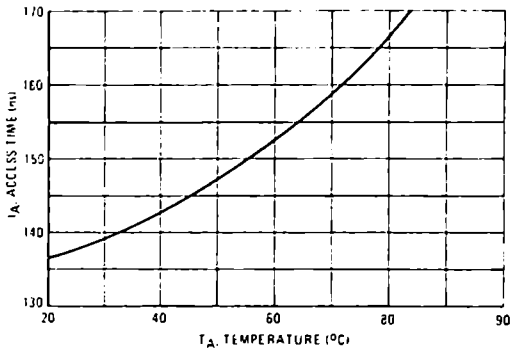
OUTPUT SINK CURRENT versus OUTPUT VOLTAGE



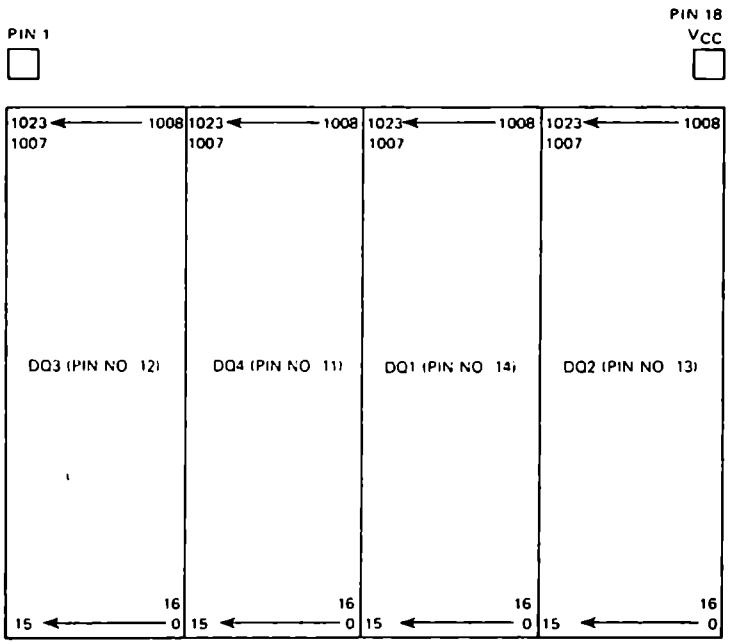
NORMALIZED ACCESS TIME versus TEMPERATURE



TYPICAL ACCESS TIME versus TEMPERATURE



MCM2114/MCM21L14 BIT MAP



To determine the precise location on the die of a word in memory, reassign address numbers to the address pins as in the table below. The bit locations can then be determined directly from the bit map.

PIN NUMBER	REASSIGNED ADDRESS NUMBER	PIN NUMBER	REASSIGNED ADDRESS NUMBER
1	A6	6	A1
2	A5	7	A2
3	A4	15	$\overline{A9}$
4	A3	16	$\overline{A8}$
5	A0	17	$\overline{A7}$

MOTOROLA

MCM2115A
MCM21L15A
MCM2125A
MCM21L25A

1024 × 1 STATIC RAM

The MCM2115A and MCM2125A families are high-speed, 1024 words by one-bit, random-access memories fabricated using HMOS, high-performance N-channel silicon-gate technology. Both open collector (MCM2115A) and three-state output (MCM2125A) are available. The devices use fully static circuitry throughout and require no clocks or timing strobes. Data out has the same polarity as the input data.

Access times are fully compatible with the industry-produced 1K Bipolar RAMs, yet offer up to 50% reduction in power over their Bipolar equivalents.

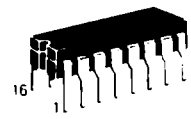
All inputs and output are directly TTL compatible. The chip select allows easy selection of an individual device when outputs are OR-tied.

- Organized as 1024 Words of 1 Bit
- Single +5 V Operation
- Maximum Access Time of 45 ns, 55 ns, and 70 ns available
- Low Operating Power Dissipation
- Pin Compatible to 93415A (2115A) and 93425A (2125A)
- TTL Inputs and Outputs
- Uncommitted Collector (2115A) and Three-State (2125A) Output

MOS

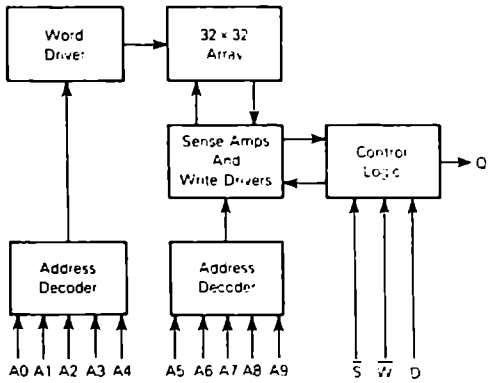
(N-CHANNEL, SILICON-GATE)

1024-BIT STATIC
RANDOM ACCESS
MEMORY

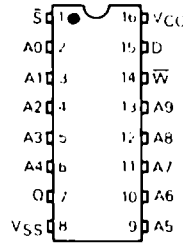


C SUFFIX
FRIT SEAL
CERAMIC PACKAGE
CASE 620-06

BLOCK DIAGRAM



PIN ASSIGNMENT



TRUTH TABLE

Inputs			Output 2115A Family	Output 2125A Family	Mode
S̄	W̄	D	Q	Q	
H	X	X	H	High Z	Not Selected
L	L	L	H	High Z	Write "0"
L	L	H	H	High Z	Write "1"
L	H	X	Data Out	Data Out	Read

PIN NAMES

A	Address
D	Data Input
Q	Data Output
S̄	Chip Select
VCC	+5 V Supply
VSS	Ground
W̄	Write Enable

DS9819/5-80

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Value	Unit
Temperature Under Bias	- 10 to + 80	°C
Voltage on Any Pin With Respect to V_{SS}	- 0.5 to + 7.0	Vdc
DC Output Current	20	mA
Power Dissipation	1.0	Watt
Operating Temperature Range	0 to + 70	°C
Storage Temperature Range	- 65 to + 150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

NOTE Permanent damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted.)

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC} V_{SS}	4.75 0	5.0 0	5.25 0	V
Logic 1 Voltage, All Inputs	V_{IH}	2.1		6	V
Logic 0 Voltage, All Inputs	V_{IL}	- 0.3	-	0.8	V

DC OPERATING CHARACTERISTICS

Parameter	Symbol	MCM2115A		MCM21L15A		MCM2125A		MCM21L25A		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Input Low Current (All Input Pins, V_{in} = 0 to 5.5 V)	I_{IL}	-	- 40	-	- 40		- 40	-	- 40	µA
Input High Current	I_{IH}	-	40		40	-	40	-	40	µA
Output Leakage Current (V_{out} = 0.5/2.4 V)	I_{OL}	-		-			50	-	50	µA
Output Leakage Current (V_{out} = 4.5 V)	I_{CEX}	-	100	-	100	-	-	-	-	µA
Power Supply Current (S = V_{IL}, Outputs Open, T_A = 25°C)	I_{CC}	-	125	-	75	-	125	-	75	mA
Output Low Voltage (I_{OL} = 7.0 mA, 2125A, 16 mA 2115A)	V_{OL}	-	0.45	-	0.45	-	0.45	-	0.45	V
Output High Voltage (I_{OH} = - 4.0 mA)	V_{OH}	-	-	-	-	2.4	-	2.4	-	V
Current Short Circuit to Ground	I_{OS}		-	-	-	-	- 100	-	- 100	mA

MCM2115A FAMILY AC OPERATING CONDITIONS AND CHARACTERISTICS, READ, WRITE CYCLES

(T_A = 0 to 70°C, V_{CC} = 5.0 V ± 5%)

Parameter	Symbol	MCM2115A-45		MCM2115A-55		MCM2115A-70		Units
		Min	Max	Min	Max	Min	Max	
Chip Select Low Output Valid	t_{SLQV}	5	30	5	35	5	40	ns
Chip Select High to Output Invalid	t_{SHQZ}	-	30	-	35	-	40	ns
Address Valid to Output Valid	t_{AVQV}	-	45	-	55	-	70	ns
Address Valid to Output Invalid	t_{AVQX}	10	-	10	-	10	-	ns
Write Low to Output Disable	t_{WLQZ}	-	30	-	35	-	40	ns
Write High to Output Valid	t_{WHQV}	0	30	0	35	0	45	ns
Write Low to Write High (Write Pulse Width)	t_{WLWH}	30	-	40	-	50	-	ns
Data Valid to Write Low	t_{DVWL}	5	-	5	-	5	-	ns
Write High to Data Don't Care (Data Hold)	t_{WHDX}	5	-	5	-	5	-	ns
Address Valid to Write Low (Address Setup)	t_{AVWL}	5	-	5	-	15	-	ns
Write High to Address Don't Care	t_{WHAX}	5	-	5	-	5	-	ns
Chip Select Low to Write Low	t_{SLWL}	5	-	5	-	5	-	ns
Write High to Chip Select High	t_{WHSH}	5	-	5	-	5	-	ns
Address Valid to Address Don't Care	t_{AVAX}	-	45	-	55	-	70	ns
Chip Select Low to Chip Select High	t_{SLSH}	-	45	-	55	-	70	ns

MCM21L15A FAMILY AC OPERATING CONDITIONS AND CHARACTERISTICS, READ, WRITE CYCLES

(T_A = 0 to 70°C, V_{CC} = 5.0 V ±5%)

Parameter	Symbol	MCM21L15A-45		MCM21L15A-70		Units
		Min	Max	Min	Max	
Chip Select Low to Output Valid	t_{SLQV}	5	30	5	30	ns
Chip Select High to Output Invalid	t_{SHQZ}	–	30	–	30	ns
Address Valid to Output Valid	t_{AVQV}	–	45	–	70	ns
Address Valid to Output Invalid	t_{AVQX}	10	–	10	–	ns
Write Low to Output Disable	t_{WLQZ}	–	25	–	25	ns
Write High to Output Valid	t_{WHQV}	0	25	0	25	ns
Write Low to Write High (Write Pulse Width)	t_{WLWH}	30	–	30	–	ns
Data Valid to Write Low	t_{DVWL}	0	–	0	–	ns
Write High to Data Don't Care	t_{WHDX}	5	–	5	–	ns
Address Valid to Write Low (Address Setup)	t_{AVWL}	5	–	5	–	ns
Write High to Address Don't Care	t_{WHAX}	5	–	5	–	ns
Chip Select Low to Write Low	t_{SLWL}	5	–	5	–	ns
Write High to Chip Select High	t_{WHSH}	5	–	5	–	ns
Address Valid to Address Don't Care	t_{AVAX}	–	45	–	70	ns
Chip Select Low to Chip Select High	t_{SLSH}	–	45	–	70	ns

MCM2125A FAMILY AC OPERATING CONDITIONS AND CHARACTERISTICS, READ, WRITE CYCLES

(T_A = 0 to 70°C, V_{CC} = 5.0 V ±5%)

Parameter	Symbol	MCM2125A-45		MCM2125A-55		MCM2125A-70		Units
		Min	Max	Min	Max	Min	Max	
Chip Select Low to Output Valid	t_{SLQV}	5	30	5	35	5	40	ns
Chip Select High to Output High Z	t_{SHQZ}	–	30	–	35	–	40	ns
Address Valid to Output Valid	t_{AVQV}	–	45	–	55	–	70	ns
Address Valid to Output Invalid	t_{AVQX}	10	–	10	–	10	–	ns
Write Low to Output High Z	t_{WLQZ}	–	30	–	35	–	40	ns
Write High to Output Valid	t_{WHQV}	0	30	0	35	0	45	ns
Write Low to Write High (Write Pulse Width)	t_{WLWH}	30	–	40	–	50	–	ns
Data Valid to Write Low	t_{DVWL}	5	–	5	–	5	–	ns
Write High to Data Don't Care	t_{WHDX}	5	–	5	–	5	–	ns
Address Valid to Write Low (Address Setup)	t_{AVWL}	5	–	5	–	15	–	ns
Write High to Address Don't Care	t_{WHAX}	5	–	5	–	5	–	ns
Chip Select Low to Write Low	t_{SLWL}	5	–	5	–	5	–	ns
Write High to Chip Select High	t_{WHSH}	5	–	5	–	5	–	ns
Address Valid to Address Don't Care	t_{AVAX}	–	45	–	55	–	70	ns
Chip Select Low to Chip Select High	t_{SLSH}	–	45	–	55	–	70	ns

MCM21L25A FAMILY AC OPERATING CONDITIONS AND CHARACTERISTICS, READ, WRITE CYCLES

(T_A = 0 to 70°C, V_{CC} = 5.0 V ±5%)

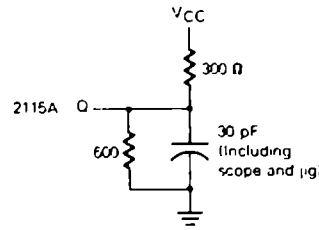
Parameter	Symbol	MCM21L25A-45		MCM21L25A-70		Units
		Min	Max	Min	Max	
Chip Select Low to Output Valid	t_{SLQV}	5	30	5	30	ns
Chip Select High to Output High Z	t_{SHQZ}	–	30	–	30	ns
Address Valid to Output Valid	t_{AVQV}	–	45	–	70	ns
Address Valid to Output Invalid	t_{AVQX}	10	–	10	–	ns
Write Low to Output High Z	t_{WLQZ}	–	25	–	25	ns
Write High to Output Valid	t_{WHQV}	0	25	0	25	ns
Write Low to Write High (Write Pulse Width)	t_{WLWH}	30	–	30	–	ns
Data Valid to Write Low	t_{DVWL}	0	–	0	–	ns
Write High to Data Don't Care	t_{WHDX}	5	–	5	–	ns
Address Valid to Write Low (Address Setup)	t_{AVWL}	5	–	5	–	ns
Write High to Address Don't Care	t_{WHAX}	5	–	5	–	ns
Chip Select Low to Write Low	t_{SLWL}	5	–	5	–	ns
Write High to Chip Select High	t_{WHSH}	5	–	5	–	ns
Address Valid to Address Don't Care	t_{AVAX}	–	45	–	70	ns
Chip Select Low to Chip Select High	t_{SLSH}	–	45	–	70	ns

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, periodically sampled rather than 100% tested.)

Characteristic	Symbol	Max	Unit
Input Capacitance (V_{in} = 0 V)	C_{in}	5	pF
Output Capacitance (V_{out} = 0 V)	C_{out}	8	pF

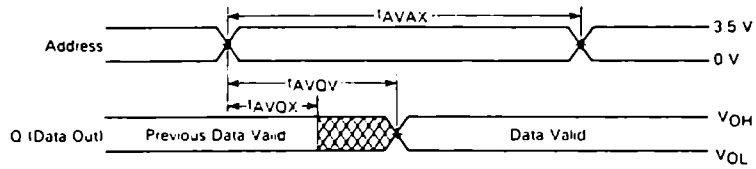
Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation $C = I\Delta_t/\Delta V$

OUTPUT LOAD

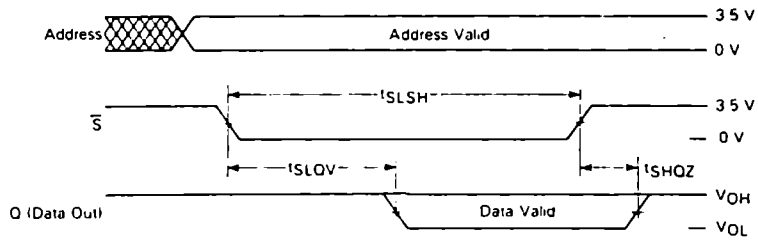


2115A FAMILY

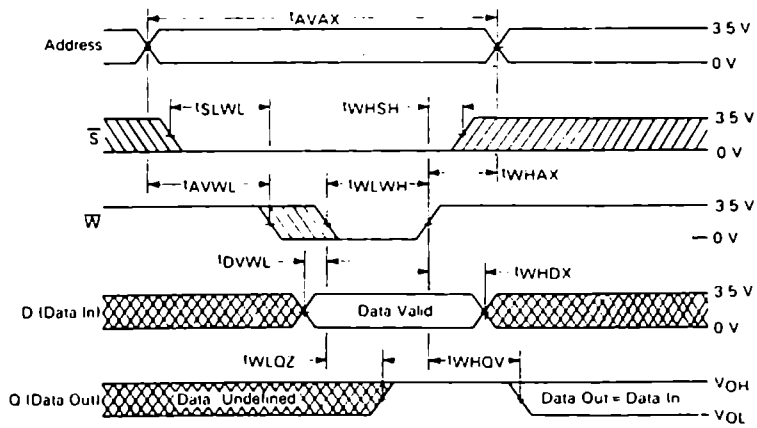
READ CYCLE TIMING 1
($\overline{S}$ Held Low, $\overline{W}$ Held High)



READ CYCLE TIMING 2
($\overline{W}$ Held High)



WRITE CYCLE TIMING

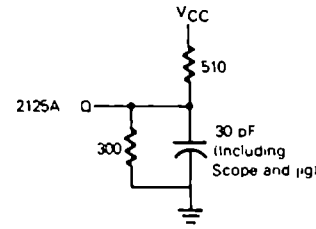


(All Time Measurements Referenced to 1.5 V)

WAVEFORMS

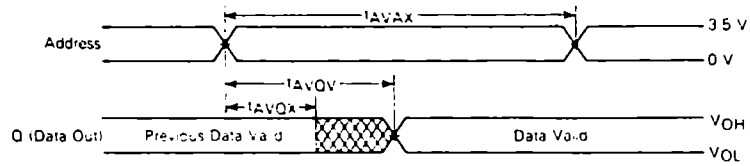
Waveform Symbol	Input	Output
	Must Be Valid	Will Be Valid
	Change From H to L	Will Change From H to L
	Change From L to H	Will Change From L to H
	Don't Care Any Change Permitted	Changing State Unknown
	–	High Impedance

OUTPUT LOAD

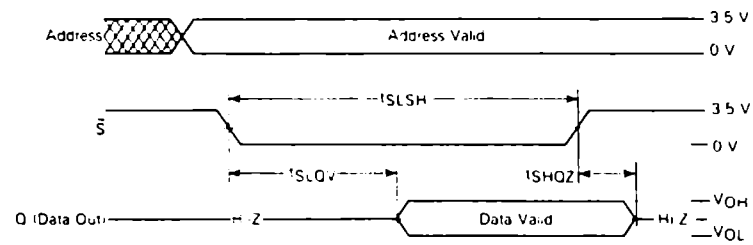


2125A FAMILY

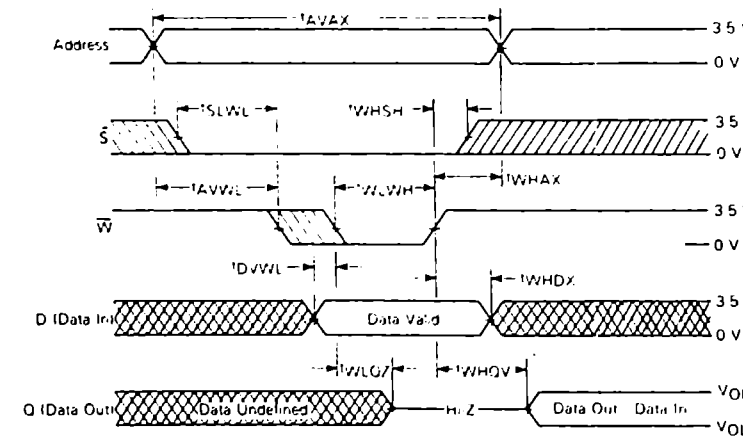
READ CYCLE TIMING 1
($\overline{S}$ Held Low, $\overline{W}$ Held High)



READ CYCLE TIMING 2
($\overline{W}$ Held High)



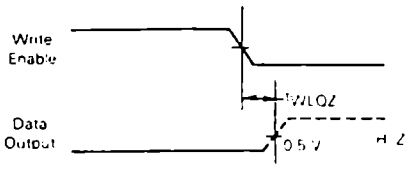
WRITE CYCLE TIMING



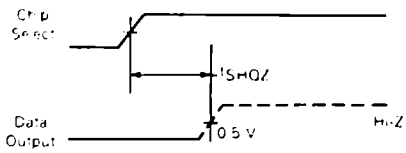
(All time measurements referenced to 1.5 V)

2115A FAMILY

WRITE ENABLE TO HIGH-Z DELAY

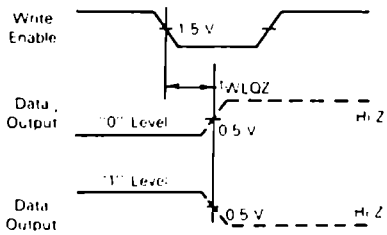


PROPAGATION DELAY FROM CHIP SELECT TO HIGH-Z

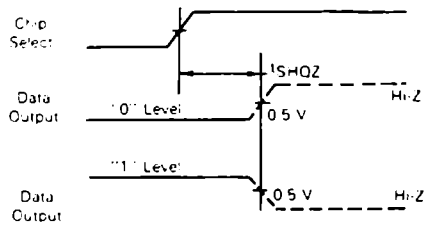


2125A FAMILY

WRITE ENABLE TO HIGH-Z DELAY



PROPAGATION DELAY FROM CHIP SELECT TO HIGH-Z



MOTOROLA

MCM2115H
MCM2125H

Product Preview

1024 x 1 STATIC RAM

The MCM2115H and MCM2125H families are high-speed, 1024 words by one-bit, random-access memories fabricated using HMOS, high-performance N-channel silicon-gate technology. Both open collector (MCM2115H) and three-state output (MCM2125H) are available. The devices use fully static circuitry throughout and require no clocks or refreshing to operate. Data out has the same polarity as the input data.

Access times are fully compatible with the industry-produced 1K Bipolar RAMs, yet offer up to 50% reduction in power over their Bipolar equivalents.

All inputs and outputs are directly TTL compatible. A separate chip select allows easy selection of an individual device when outputs are OR-tied.

- Organized as 1024 Words of 1 Bit
- Single +5 V Operation
- Maximum Access Time of 20 ns, 25 ns, 30 ns, and 35 ns Available
- Low Operating Power Dissipation
- Pin Compatible to 93415A (2115H) and 93425A (2125H)
- TTL Inputs and Outputs
- Uncommitted Collector (2115H) and Three-State (2125H) Output

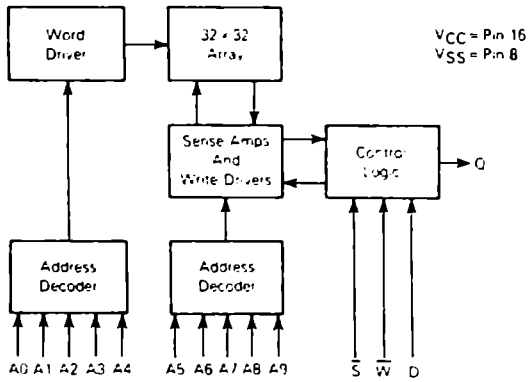
MOS

(N-CHANNEL, SILICON-GATE)

1024-BIT STATIC RANDOM ACCESS MEMORY

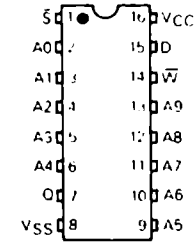
C SUFFIX
FRIT-SEAL
CERAMIC PACKAGE
CASE 620-06

BLOCK DIAGRAM



V_{CC} = Pin 16
V_{SS} = Pin 8

PIN ASSIGNMENT



PIN NAMES	
A	Address
D	Data Input
Q	Data Output
$\overline{S}$	Chip Select
V_{CC}	+5 V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

TRUTH TABLE

Inputs			Output 2115H Family	Output 2125H Family	Mode
$\overline{S}$	$\overline{W}$	D	Q	Q	
H	X	X	H	High Z	Not Selected
L	L	L	H	High Z	Write "0"
L	L	H	H	High Z	Write "1"
L	H	X	Data Out	Data Out	Read

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NP321/11-80

MOTOROLA

MCM2147

4096-BIT STATIC RANDOM ACCESS MEMORY

The MCM2147 is a 4096 bit static random access memory organized as 4096 words by 1-bit using Motorola's N-channel silicon gate MOS technology. It uses a design approach which provides the simple timing features associated with fully static memories and the reduced standby power associated with semi-static and dynamic memories. This means low standby power without the need for clocks, nor reduced data rates due to cycle times that exceed access times.

$\overline{E}$ controls the power-down feature. It is not a clock but rather a chip select that affects power consumption. In less than a cycle time after $\overline{E}$ goes high, deselect mode, the part automatically reduces its power requirements and remains in this low-power standby mode as long as $\overline{E}$ remains high. This feature results in system power savings as great as 85% in larger systems, where most devices are deselected. The automatic power-down feature causes no performance degradation.

The MCM2147 is in an 16 pin dual in-line package with the industry standard pinout. It is TTL compatible in all respects. The data out has the same polarity as the input data. A data input and a separate three-state output provide flexibility and allow easy OR-ties.

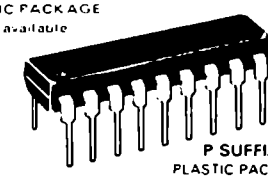
- Fully Static Memory – No Clock or Timing Strobe Required
- Single +5 V Supply
- High Density 18 Pin Package
- Automatic Power-Down
- Directly TTL Compatible – All Inputs and Outputs
- Separate Data Input and Output
- Three-State Output
- Access Time – MCM2147-55 = 55 ns max
  MCM2147-70 = 70 ns max
  MCM2147-85 = 85 ns max
  MCM2147-100 = 100 ns max

MOS

N CHANNEL, SILICON GATE

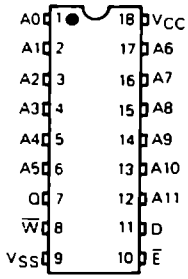
4096-BIT STATIC RANDOM ACCESS MEMORY

C SUFFIX
FRIT SEAL
CERAMIC PACKAGE
also available



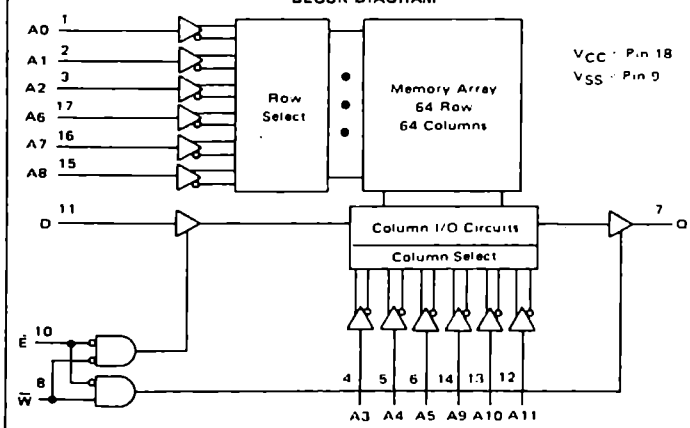
P SUFFIX
PLASTIC PACKAGE
CASE 707-02

PIN ASSIGNMENT



PIN NAMES	
A0-A11	Address Input
$\overline{W}$	Write Enable
$\overline{E}$	Chip Enable
D	Data Input
Q	Data Output
V_{CC}	Power (+5 V)
V_{SS}	Ground

BLOCK DIAGRAM



TRUTH TABLE

$\overline{E}$	$\overline{W}$	Mode	Output	Power
H	X	Not Selected	High Z	Standby
L	L	Write	High Z	Active
L	H	Read	Data Out	Active

DS9821/10-80

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Value	Unit
Temperature Under Bias	-10 to +85	°C
Voltage on Any Pin With Respect to V_{CC}	-0.5 to +7.0	Vdc
DC Output Current	20	mA
Power Dissipation	1.0	Watt
Operating Temperature Range	0 to +70	°C
Storage Temperature Range	-65 to +150	°C

Note. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC} V_{SS}	4.5 0	5.0 0	5.5 0	V
Logic 1 Voltage, All Inputs	V_{IH}	2.0	–	V_{CC}	V
Logic 0 Voltage, All Inputs	V_{IL}	-0.3	–	0.8	V

DC CHARACTERISTICS

Parameter	Symbol	MCM2147-55			MCM2147-70			MCM2147-85			MCM2147-100			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Load Current (All Input Pins, V_{in} = 0 to 5.5 V)	I_{IL}	–	0.01	10	–	0.01	10	–	0.01	10	–	0.01	10	μA
Output Leakage Current ($\overline{E}$ = 2.0 V, V_{out} = 0 to 5.5 V)	I_{OL}	–	0.1	50	–	0.1	50	–	0.1	50	–	0.1	50	μA
Power Supply Current ($\overline{E}$ = V_{IL}, Outputs Open, T_A = 25°C)	I_{CC1}	–	120	170	–	100	150	–	95	130	–	90	110	mA
Power Supply Current ($\overline{E}$ = V_{IL}, Outputs Open, T_A = 0°C)	I_{CC2}	–	–	180	–	–	160	–	–	140	–	–	120	mA
Standby Current ($\overline{E}$ = V_{IH})	I_{SB}	–	15	30	–	10	20	–	15	25	–	10	20	mA
Input Low Voltage	V_{IL}	-0.3	–	0.8	-0.3	–	0.8	-0.3	–	0.8	-0.3	–	0.8	V
Input High Voltage	V_{IH}	2.0	–	6.0	2.0	–	6.0	2.0	–	6.0	2.0	–	6.0	V
Output Low Voltage (I_{OL} = 8.0 mA)	V_{OL}	–	–	0.4	–	–	0.4	–	–	0.4	–	–	0.4	V
Output High Voltage (I_{OH} = -4.0 mA)	V_{OH}	2.4	–	–	2.4	–	–	2.4	–	–	2.4	–	–	V

Typical values are for T_A = 25°C and V_{CC} = +5.0 V.

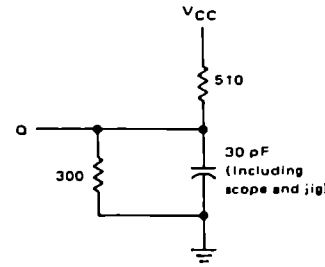
CAPACITANCE

(f = 1.0 MHz, T_A = 25°C, periodically sampled rather than 100% tested.)

Characteristic	Symbol	Max	Unit
Input Capacitance (V_{in} = 0 V)	C_{in}	5.0	pF
Output Capacitance (V_{out} = 0 V)	C_{out}	10	pF

Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: $C = \frac{t\Delta_t}{\Delta V}$.

FIGURE 1 – OUTPUT LOAD



AC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature unless otherwise noted)

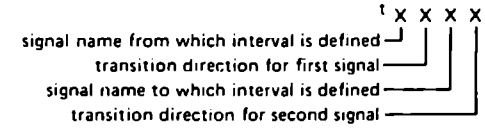
Input Pulse Levels	0 Volt to 3.5 Volts	Input and Output Timing Levels	1.5 Volts
Input Rise and Fall Times	10 ns	Output Load	See Figure 1

READ, WRITE CYCLES

Parameter	Symbol	MCM2147-55		MCM2147-70		MCM2147-85		MCM2147-100		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Address Valid to Address Don't Care (Cycle Time When Chip Enable is Held Active)	t_{AVAX}	55	–	70	–	85	–	100	–	ns
Chip Enable Low to Chip Enable High	t_{ELEH}	55	–	70	–	85	–	100	–	ns
Address Valid to Output Valid (Access)	t_{AVQV}	–	55	–	70	–	85	–	100	ns
Chip Enable Low to Output Valid (Access)	t_{ELQV1}*	–	55	–	70	–	85	–	100	ns
	t_{ELQV2}*	–	65	–	80	–	95	–	110	ns
Address Valid to Output Invalid	t_{AVQX}	10	–	10	–	10	–	10	–	ns
Chip Enable Low to Output Invalid	t_{ELQX}	10	–	10	–	10	–	10	–	ns
Chip Enable High to Output High Z	t_{EHQZ}	0	40	0	40	0	40	0	40	ns
Chip Selection to Power-Up Time	t_{PU}	0	–	0	–	0	–	0	–	ns
Chip Deselection to Power-Down Time	t_{PD}	0	30	0	30	0	30	0	30	ns
Address Valid to Chip Enable Low (Address Setup)	t_{AVEL}	0	–	0	–	0	–	0	–	ns
Chip Enable Low to Write High	t_{ELWH}	45	–	55	–	70	–	80	–	ns
Address Valid to Write High	t_{AVWH}	45	–	55	–	70	–	80	–	ns
Address Valid to Write Low (Address Setup)	t_{AVWL}	0	–	0	–	0	–	0	–	ns
Write Low to Write High (Write Pulse Width)	t_{WLWH}	35	–	40	–	55	–	65	–	ns
Write High to Address Don't Care	t_{WHAX}	10	–	15	–	15	–	15	–	ns
Data Valid to Write High	t_{DVWH}	25	–	30	–	45	–	55	–	ns
Write High to Data Don't Care (Data Hold)	t_{WHDX}	10	–	10	–	10	–	10	–	ns
Write Low to Output High Z	t_{WLQZ}	0	30	0	35	0	45	0	50	ns
Write High to Output Valid	t_{WHQV}	0	–	0	–	0	–	0	–	ns

*t_{ELQV1} is access from chip enable when the 2147 is deselected for at least 55 ns prior to this cycle. t_{ELQV2} is access from chip enable for 0 ns < deselect time < 55 ns. If deselect time = 0 ns, then $t_{ELQV} = t_{AVQV}$

TIMING PARAMETER ABBREVIATIONS


t X X X X
signal name from which interval is defined
transition direction for first signal
signal name to which interval is defined
transition direction for second signal

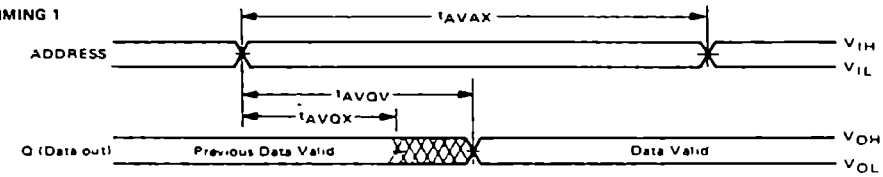
The transition definitions used in this data sheet are:

- H = transition to high
- L = transition to low
- V = transition to valid
- X = transition to invalid or don't care
- Z = transition to off (high impedance)

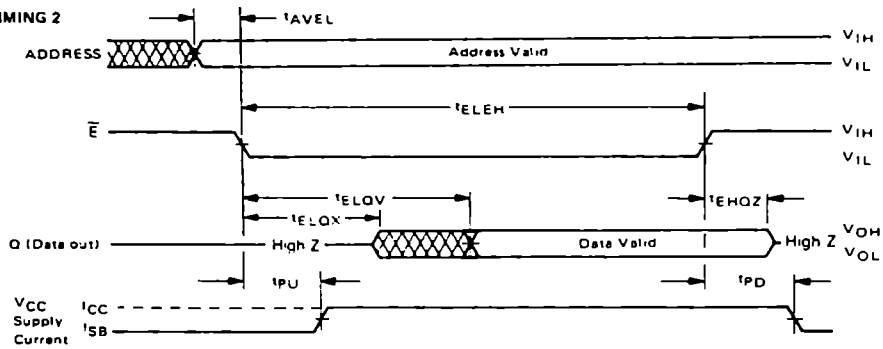
TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

READ CYCLE TIMING 1
($\overline{E}$ Hold Low)

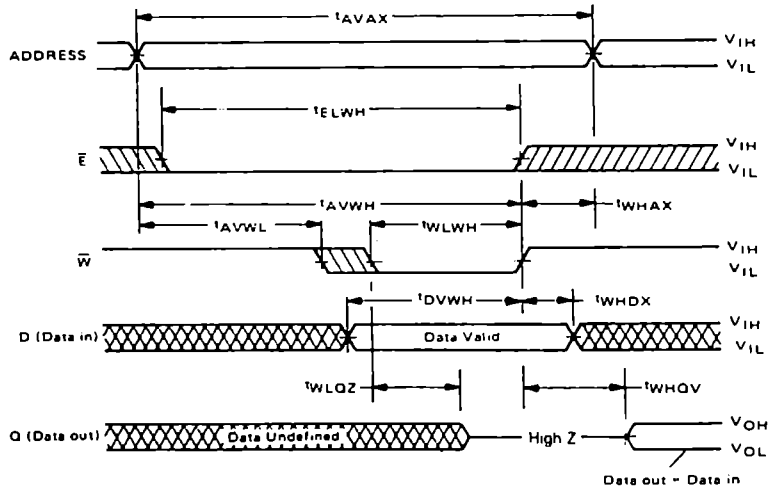


READ CYCLE TIMING 2



NOTE: $\overline{W}$ is high for Read Cycles

WRITE CYCLE TIMING



WAVEFORMS

Waveform Symbol	Input	Output
———	MUST BE VALID	WILL BE VALID
▨	CHANGE FROM H TO L	WILL CHANGE FROM H TO L
▨	CHANGE FROM L TO H	WILL CHANGE FROM L TO H
▨	DON'T CARE ANY CHANGE PERMITTED	CHANGING STATE UNKNOWN
———		HIGH IMPEDANCE

DEVICE DESCRIPTION

The MCM2147 is produced with a high-performance MOS technology which combines on-chip substrate bias generation with device scaling to achieve high speed. The speed-power product of this process is about four times better than earlier MOS processes.

This gives the MCM2147 its high speed, low power and ease-of-use. The low-power standby feature is controlled with the $\overline{E}$ input. *$\overline{E}$ is not a clock and does not have to be cycled.* This allows the user to tie $\overline{E}$ directly to system addresses and use the line as part of the normal decoding logic. Whenever the MCM2147 is deselected, it automatically reduces its power requirements.

SYSTEM POWER SAVINGS

The automatic power-down feature adds up to significant system power savings. Unselected devices draw low standby power and only the active devices draw active power. Thus the average power consumed by a device declines as the system size increases, asymptotically approaching the standby power level as shown in Figure 2.

The automatic power-down feature is obtained without any performance degradation, since access time from chip enable is the same as access time from address valid. Also the fully static design gives access time equal cycle time so multiple read or write operations are possible during a single select period. The resultant data rates are 14.3 MHz and 18 MHz for the MCM2147-70 and MCM2147-55 respectively.

DECOUPLING AND BOARD LAYOUT CONSIDERATIONS

The power switching characteristic of the MCM2147 requires careful decoupling. It is recommended that a 0.1 μF to 0.3 μF ceramic capacitor be used on every other device, with a 22 μF to 47 μF bulk electrolytic decoupler every 16 devices. The actual values to be used will depend on board layout, trace widths and duty cycle.

Power supply gridding is recommended for PC board layout. A very satisfactory grid can be developed on a two layer board with vertical traces on one side and horizontal traces on the other, as shown in Figure 3. If fast drivers are used, terminations are recommended on input signal lines to the MCM2147 because significant reflections are possible when driving their high impedance inputs. Terminations may be required to match the impedance of the line to the driver.

FIGURE 2 – AVERAGE DEVICE DISSIPATION versus MEMORY SIZE

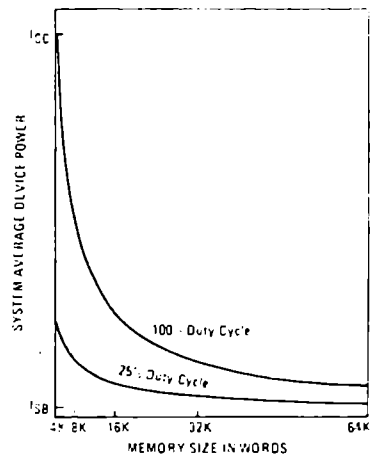
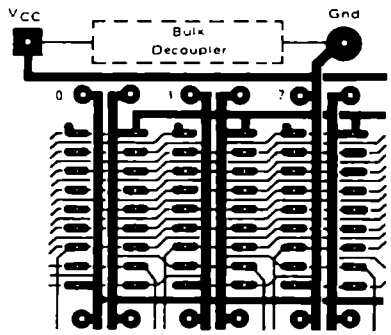


FIGURE 3 – PC LAYOUT



MOTOROLA

MCM2147H

Product Preview

4096-BIT STATIC RANDOM ACCESS MEMORY

The MCM2147H is a 4096-bit static random access memory organized as 4096 words by 1-bit using Motorola's high-performance N-channel silicon-gate MOS technology (HMOS). It uses a design approach which provides the simple timing features associated with fully static memories and the reduced standby power associated with semi-static and dynamic memories. This means low standby power without the need for clocks, nor reduced data rates due to cycle times that exceed access times.

$\overline{E}$ controls the power-down feature. It is not a clock but rather a chip select that affects power consumption. In less than a cycle time after $\overline{E}$ goes high, deselect mode, the part automatically reduces its power requirements and remains in this low-power standby mode as long as $\overline{E}$ remains high. This feature results in system power savings as great as 85% in larger systems, where most devices are deselected. The automatic power-down feature causes no performance degradation.

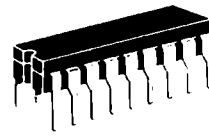
The MCM2147H is in an 18 pin dual in-line package with the industry standard pinout. It is TTL compatible in all respects. The data out has the same polarity as the input data. A data input and a separate three-state output provide flexibility and allow easy OR-ing.

- Fully Static Memory — No Clock or Timing Strobe Required
- HMOS Technology
- Single +5 V Supply
- High Density 18 Pin Package
- Automatic Power Down
- Directly TTL Compatible — All Inputs and Outputs
- Separate Data Input and Output
- Three-State Output
- Access Time
  - MCM2147H-35 = 35 ns Max
  - MCM2147H-45 = 45 ns Max
  - MCM2147H-55 = 55 ns Max

MOS

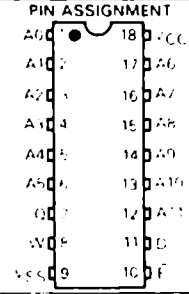
(N-CHANNEL, SILICON-GATE)

4096-BIT STATIC RANDOM ACCESS MEMORY



C SUFFIX
CERAMIC PACKAGE
CASE 726-02

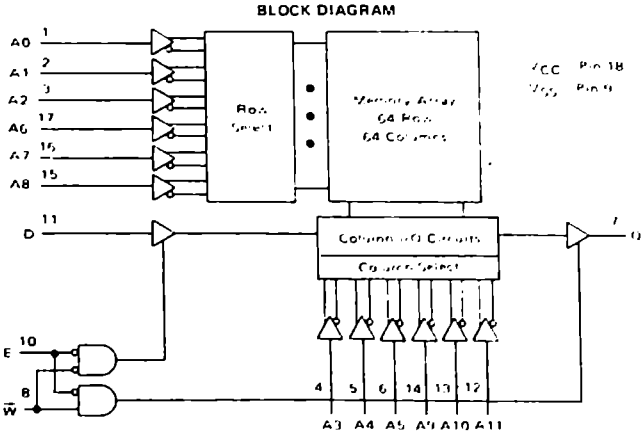
PIN ASSIGNMENT



PIN NAMES

A_0–A_{11}	Address Inputs
$\overline{W}$	Write Enable
$\overline{E}$	Chip Enable
D	Data Input
Q	Data Output
V_{CC}	Power (+5 V)
V_{SS}	Ground

BLOCK DIAGRAM



TRUTH TABLE

$\overline{E}$	$\overline{W}$	Mode	Output	Power
H	X	Not Selected	High Z	Standby
L	L	Write	High Z	Active
L	H	Read	Data Out	Active

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NP322/11 80

MOTOROLA

MCM2148

Advance Information

4096-BIT STATIC RANDOM ACCESS MEMORY

The MCM2148 is a 4096-bit random access memory fabricated using HMOS, high performance MOS technology. For ease of use, the device operates from a single power supply, is directly compatible with TTL and requires no clocks or refreshing because of fully static operation. Data access is particularly simple, since address setup times are not required. The output data has the same polarity as the input data.

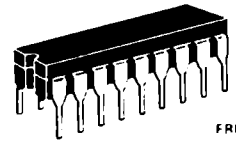
The MCM2148 is designed for memory applications where simple interfacing is the design objective. The MCM2148 is assembled in 18-pin dual-in-line packages with the industry standard pin-out. A separate chip select ($\overline{E}$) lead allows easy selection of an individual package when the three state outputs are OR-tied.

- 1024 Words by 4-Bit Organization
- HMOS Technology
- Industry Standard 18-Pin Configuration
- Single +5 Volt Supply
- No Clock or Timing Strobe Required
- Maximum Access Time
  - 70 ns MCM2148-70
  - 85 ns MCM2148-85
- Power Dissipation
  - 140 mA Maximum (Active)
  - 30 mA Maximum (Standby)
- Fully TTL/DTL Compatible
- Common Data Input and Output
- Three-State Outputs for OR-Ties
- Automatic Power Down

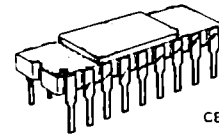
MOS

(N-CHANNEL, SILICON-GATE)

4096-BIT STATIC RANDOM ACCESS MEMORY

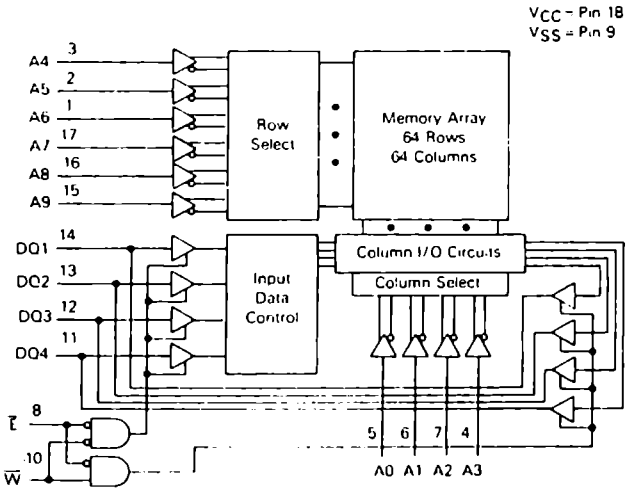


C SUFFIX
FRIT-SEAL PACKAGE
CASE 726

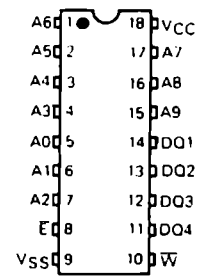


L SUFFIX
CERAMIC PACKAGE
CASE 680

BLOCK DIAGRAM



PIN ASSIGNMENT



PIN NAMES	
A0-A9	Address Input
$\overline{W}$	Write Enable
$\overline{E}$	Chip Select
DQ1-DQ4	Data Input/Output
V_{CC}	Power (+5 V)
V_{SS}	Ground

AD1851/9-80

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Value	Unit
Temperature Under Bias	– 10 to + 80	°C
Voltage on Any Pin With Respect to V_{SS}	– 3.5 to – 7.0	V
DC Output Current	20	mA
Power Dissipation	1.2	Watt
Operating Temperature Range	0 to + 70	°C
Storage Temperature Range	– 65 to + 150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields, however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

NOTE Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature ranges unless otherwise noted.)

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC} V_{SS}	4.5 0	5.0 0	5.5 0	V
Logic 1 Voltage, All Inputs	V_{IH}	2.0	–	6.0	V
Logic 0 Voltage, All Inputs	V_{IL}	– 3.0	–	0.8	V

DC CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit
Input Load Current (All Input Pins, V_{in} = 0 to 5.5 V, V_{CC} = Max)	I_{LI}	–	0.01	10	μA
Output Leakage Current ($\overline{E}$ = V_{IH}, V_{CC} = Max, V_{out} = 0 to 4.5 V)	$\|I_{LO}\|$	–	0.1	50	μA
Output Low Voltage (I_{OL} = 8 mA)	V_{OL}	–	–	0.4	mA
Output High Voltage (I_{OH} = – 2.0 mA)	V_{OH}	2.4	–	–	mA
Power Supply Current (V_{in} = 5.5, I_{DO} = 0 mA, T_A = 25°C, $\overline{E}$ = V_{IL})	I_{CC1}	–	100	135	mA
Power Supply Current (V_{in} = 5.5 V, I_{DO} = 0 mA, T_A = 0°C, $\overline{E}$ = V_{IL})	I_{CC2}	–	–	140	mA
Standby Current (V_{CC} = Min to Max, $\overline{E}$ = V_{IH})	I_{CC3}	–	12	30	mA
Peak Power on Current (V_{CC} = 0 to V_{CC} Min, $\overline{E}$ = V_{IH} min)*	I_{PO}	–	25	50	mA
Output Short Circuit Current (V_{Out} = GND to V_{CC})	I_{OS}	– 150	–	+ 150	mA

*A pullup resistor to V_{CC} on the $\overline{E}$ input is required to keep the device deselected, otherwise, power on current approaches I_{CC}.

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, periodically sampled rather than 100% tested.)

Characteristic	Symbol	Max	Unit
Input Capacitance (V_{in} = 0 V)	C_{in}	5	pf
Output Capacitance (V_{out} = 0 V)	C_{out}	7	pF

FIGURE 1

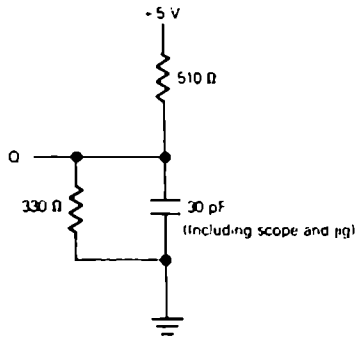
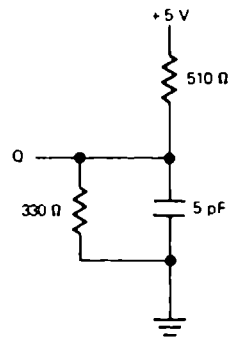


FIGURE 2



AC OPERATING CONDITIONS AND CHARACTERISTICS

(For operating voltage and temperature unless otherwise noted.)

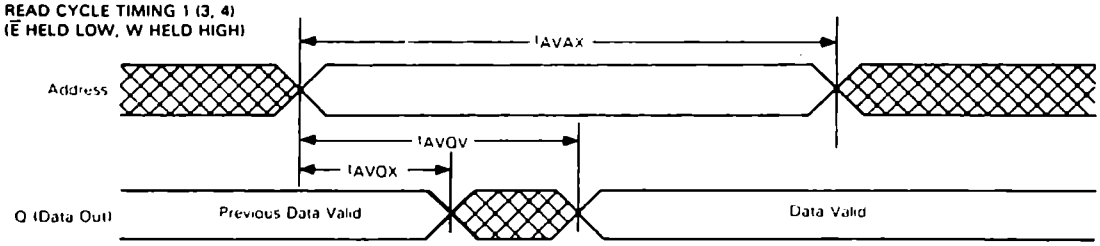
Input Pulse Levels	0 Volt to 3.0 Volts	Input and Output Timing Levels	1.5 Volts
Input Rise and Fall Times	10 ns	Output Load	See Figure 1

Parameter	Symbol	MCM2148-70		MCM2148-85		Unit	Notes
		Min	Max	Min	Max		
Address Valid to Address Don't Care (Cycle Time; $\overline{E} = V_{IL}$)	t_{AVAX}	70		85		ns	
Address Valid to Output Valid (Address Access Time)	t_{AVQV}		70		85	ns	
Address Valid to Output Undefined	t_{AVQX}	5		5		ns	
Chip Enable Low to Chip Enable High (Cycle Time)	t_{ELEH}	70		85		ns	
Chip Enable Low to Output Undefined	t_{ELQX}	25		25		ns	6
Chip Enable Low to Output Valid (Chip Select Access Time)	t_{ELQV1} t_{ELQV2}	- -	70 80	- -	85 95	ns ns	1 2
Chip Selection to Powerup Time	t_{PU}	0	-	0		ns	
Chip Deselection to Powerdown Time	t_{PD}		30		30	ns	
Chip Enable High to Output High Z	t_{EHQZ}	0	20	0	20	ns	6
Chip Enable Low to Write High	t_{ELWH}	65		80	-	ns	
Address Valid to Write Low (Address Setup)	t_{AVWL}	0		0	-	ns	
Write High to Address Don't Care	t_{WHAX}	5		5	-	ns	
Write Low to Write High (Write Pulse Width)	t_{WLWH}	50		60	-	ns	
Data Valid to Write High	t_{DVWH}	25	-	30		ns	
Write High to Data Don't Care	t_{WHDX}	5		5	-	ns	
Write Low to Output High Z	t_{WLQZ}	0	25	0	30	ns	6
Write High to Output Active	t_{WHQV}	0	-	0	-	ns	6

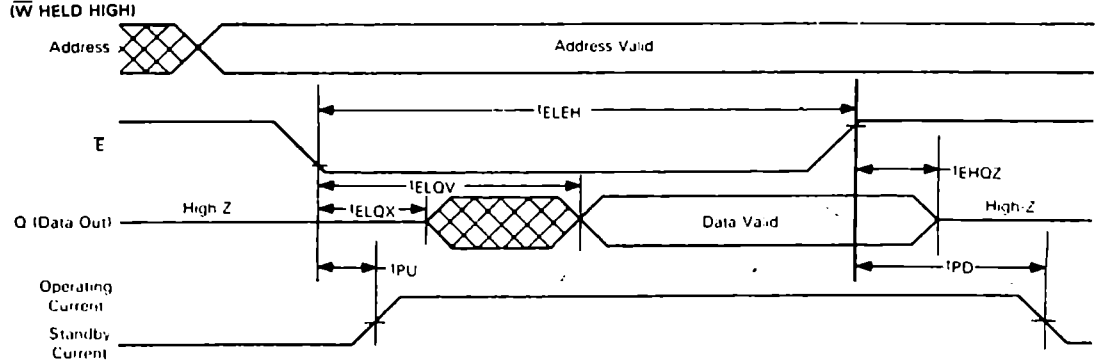
NOTES

1. Chip deselected for greater than 55 ns prior to $\overline{E}$ transition low.
2. Chip deselected for a finite time that is less than 55 ns prior to $\overline{E}$ transition low. (If the deselect time is 0 ns, the chip is by definition selected and access occurs according to Read Cycle 1.)
3. $\overline{W}$ is high for read cycles.
4. Device is continuously selected. $\overline{E} = V_{IL}$.
5. Addresses valid prior to or coincident with $\overline{E}$ transition low.
6. Transition is measured ±500 mV from high impedance with the load in Figure 2. This parameter is sampled and not 100% tested.

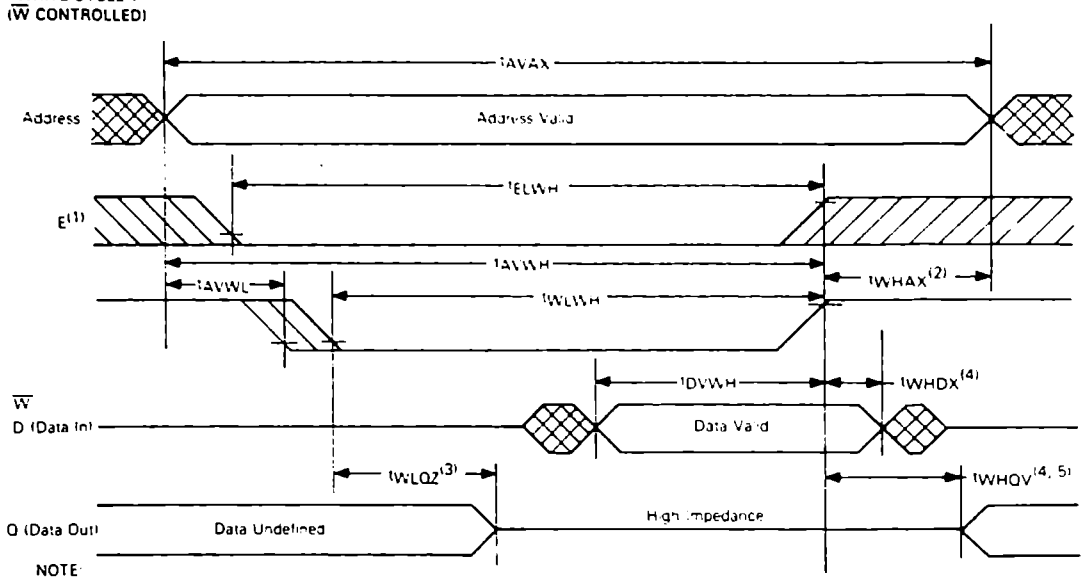
READ CYCLE TIMING 1 (3, 4)
($\overline{E}$ HELD LOW, W HELD HIGH)



READ CYCLE TIMING 2 (3, 5)
($\overline{W}$ HELD HIGH)



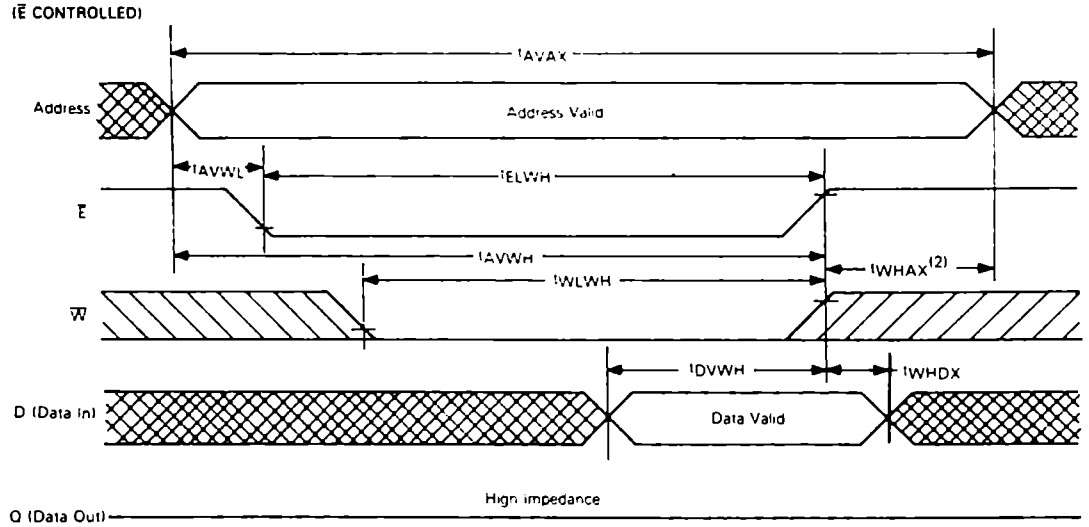
WRITE CYCLE 1
($\overline{W}$ CONTROLLED)



NOTE:

1. If $\overline{E}$ goes high simultaneously with $\overline{W}$ high, the output remains in a high impedance state.
2. tWHAX is measured from the earlier of $\overline{S}$ or $\overline{W}$ going high to the end of the write cycle.
3. During this period, DQ pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
4. If $\overline{S}$ is low during this period, the DQ pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
5. Q is the same phase of write data of this write cycle.

WRITE CYCLE 2
($\overline{E}$ CONTROLLED)



MOTOROLA

MCM2149

Product Preview

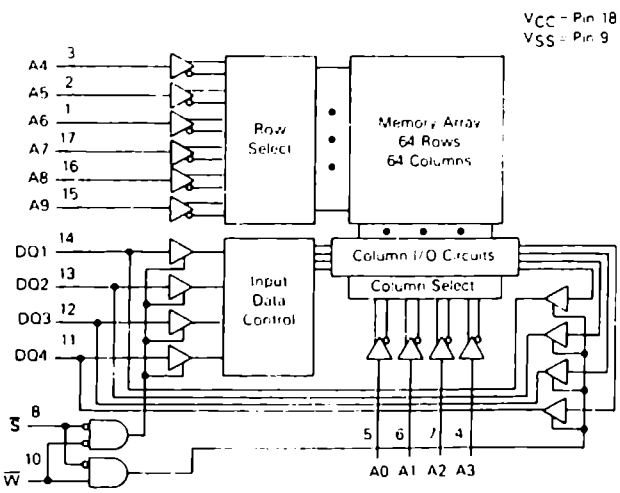
4096-BIT STATIC RANDOM ACCESS MEMORY

The MCM2149 is a 4096-bit random access memory fabricated using HMOS, high performance MOS technology. For ease of use, the device operates from a single power supply, is directly compatible with TTL and requires no clocks or refreshing because of fully static operation. Data access is particularly simple, since address setup times are not required. The output data has the same polarity as the input data.

The MCM2149 is designed for memory applications where simple interfacing is the design objective. The MCM2149 is assembled in 18-pin dual-in-line packages with the industry standard pin-out. A separate chip select ($\overline{S}$) lead allows easy selection of an individual package when the three-state outputs are OR-tied.

- 1024 Words by 4-Bit Organization
- HMOS Technology
- Industry Standard 18-Pin Configuration
- Single +5 Volt Supply
- No Clock or Timing Strobe Required
- Maximum Access Time
  MCM2149-70 = 70 ns Max.
  MCM2149-85 = 85 ns Max
- Chip Select Access Time
  MCM2149-70 = 30 ns Max.
  MCM2149-85 = 35 ns Max.
- Power Dissipation — 140 mA Maximum (Active)
- Fully TTL Compatible
- Common Data Input and Output
- Three-State Outputs for OR-Ties
- Automatic Power Down Version Available — MCM2148

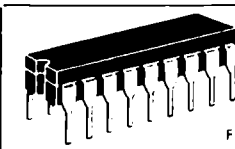
BLOCK DIAGRAM



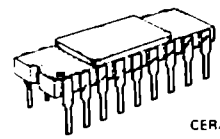
MOS

(N-CHANNEL, SILICON-GATE)

4096-BIT STATIC RANDOM ACCESS MEMORY

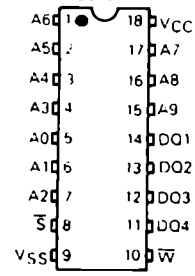


C SUFFIX
FRIT-SEAL PACKAGE
CASE 726-02



L SUFFIX
CERAMIC PACKAGE
CASE 680-06

PIN ASSIGNMENT



PIN NAMES	
A0 A9	Address Input
$\overline{W}$	Write Enable
$\overline{S}$	Chip Select
DQ1 DQ4	Data Input/Output
V_{CC}	Power (+5 V)
V_{SS}	Ground

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MOTOROLA

MCM2167

Product Preview

16,384-BIT STATIC RANDOM ACCESS MEMORY

The MCM2167 is a 16,384-bit static random access memory organized as 16,384 words by 1-bit using Motorola's N-channel silicon-gate MOS technology. It uses a design approach which provides the simple timing features associated with fully static memories and the reduced standby power associated with semi-static and dynamic memories. This means low standby power without the need for clocks, nor reduced data rates due to cycle times that exceed access times.

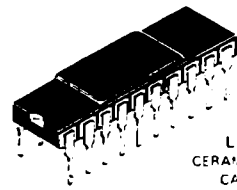
$\overline{E}$ controls the power-down feature. It is not a clock but rather a chip select that affects power consumption. In less than a cycle time after $\overline{E}$ goes high, deselect mode, the part automatically reduces its power requirements and remains in this low-power standby mode as long as $\overline{E}$ remains high. This feature results in sytem power savings as great as 85% in larger systems, where most devices are deselected. The automatic power-down feature causes no performance degradation.

The MCM2167 is in a 20 pin dual in-line package with the industry standard pinout. It is TTL compatible in all respects. The data out has the same polarity as the input data. A data input and a separate three-state output provide flexibility and allow easy OR-ties.

- Fully Static Memory – No Clock or Timing Strobe Required
- Single +5 V Supply
- High Density 20 Pin Package
- Automatic Power-Down
- Directly TTL Compatible – All Inputs and Three-State Output
- Separate Data Input and Output
- Access Time
  - MCM2167-55 – 55 ns max
  - MCM2167-70 – 70 ns max
  - MCM2167-85 – 85 ns max
  - MCM2167-100 – 100 ns max

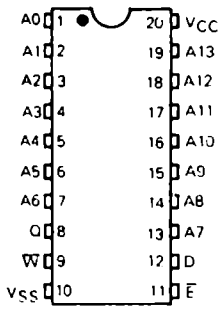
MOS
(N-CHANNEL, SILICON-GATE)

16,384-BIT STATIC RANDOM ACCESS MEMORY



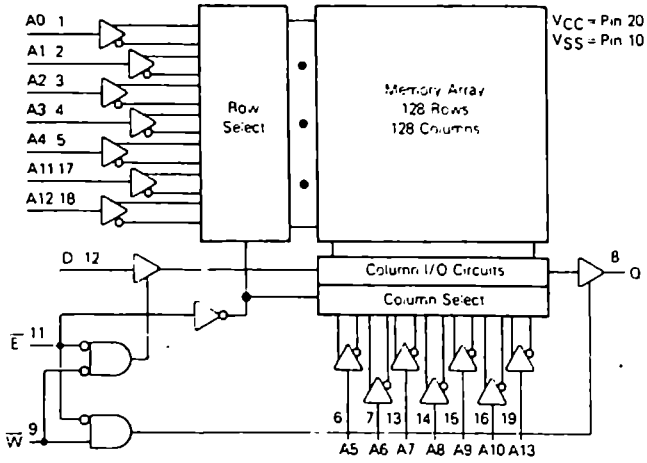
L SUFFIX
CERAMIC PACKAGE
CASE 729-02

PIN ASSIGNMENT



PIN NAMES	
A0-A13	Address Input
$\overline{W}$	Write Enable
$\overline{E}$	Chip Enable
D	Data Input
Q	Data Output
V_{CC}	Power (+5 V)
V_{SS}	Ground

BLOCK DIAGRAM



TRUTH TABLE

$\overline{E}$	$\overline{W}$	Mode	Output	Power
H	X	Not Selected	High Z	Standby
L	L	Write	High Z	Active
L	H	Read	Data Out	Active

NP326/11-80

MOTOROLA

MCM4016

Product Preview

2048 × 8-BIT STATIC RANDOM ACCESS MEMORY

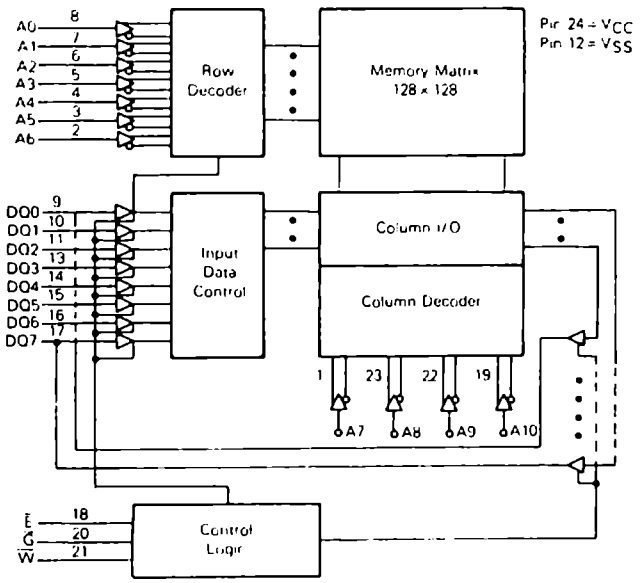
The MCM4016 is a 16,384-bit static Random Access Memory organized as 2048 words by 8-bits, fabricated using Motorola's high-performance silicon-gate metal oxide semiconductor (HMOS) technology. Its static design means that no refresh clocking circuitry is needed and timing requirements are simplified. Access time is equal to cycle time.

A chip select control is provided for controlling the flow of data in and data out, and an output enable function is provided which eliminates the need for external bus buffers.

The MCM4016 is in a 24-pin dual-in-line package with the industry standard pinout and is pinout compatible with the industry standard 16K EPROM and 16K mask programmable ROM.

- 2048 Words by 8-Bits Organization
- HMOS Technology
- Single +5 V Supply
- Fully Static: No Clock or Timing Strobe Required
- Low Power Dissipation —
  35 mW Typical (Standby)
  400 mW Typical (Active)
- Maximum Access Time: MCM4016 20 — 200 ns
- Fully TTL Compatible
- Pinout Compatible with Industry Standard 2716 16K EPROM and Mask Programmable ROM
- Output Enable ($\overline{G}$) Eliminates Need for External Bus Buffers

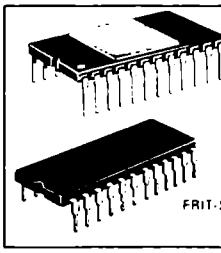
BLOCK DIAGRAM



MOS

(N-CHANNEL, SILICON-GATE)

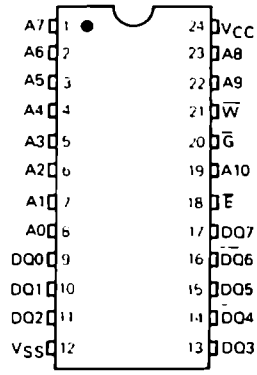
2048 × 8 BIT STATIC RANDOM ACCESS MEMORY



L SUFFIX
CERAMIC PACKAGE
CASE 716

C SUFFIX
FRIT-SEAL CERAMIC PACKAGE
CASE 623

PIN ASSIGNMENTS



PIN NAMES	
A0-A10	Address Input
DQ0-DQ7	Data Input/Output
$\overline{G}$	Output Enable
$\overline{E}$	Chip Select
$\overline{W}$	Write Enable
V_{CC}	Power (+5 V)
V_{SS}	Ground

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MOTOROLA

MCM6641
MCM66L41

Advance Information

4096-BIT STATIC RANDOM ACCESS MEMORIES

The MCM6641 series 4096 x 1-bit Random Access Memory is fabricated with high density, high reliability N-channel silicon-gate technology. For ease of use, the device operates from a single 5-volt power supply, is directly compatible with TTL and DTL, and requires no clocks or refreshing because of fully static operation. The fully static operation allows chip selects to be tied low, further simplifying system timing. Data access is particularly simple, since address setup times are not required. The output data has the same polarity as the data input.

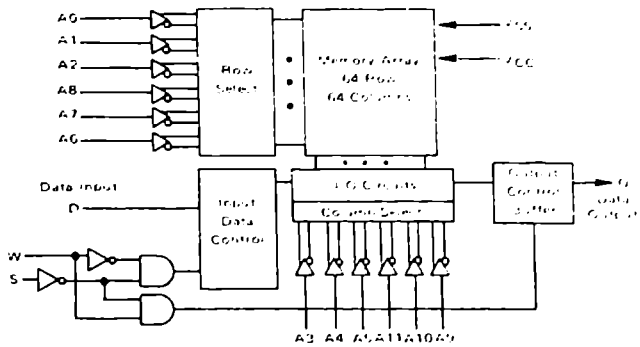
The MCM6641 is designed for memory applications where simple interfacing is the design objective, and is assembled in 18 pin dual-in-line packages with the industry standard pin-outs.

- Single ±10% +5 V Supply
- Fully Static Operation — No Clock, Timing Strobe, Pre-Charge or Refresh Required
- Industry Standard 18-Pin Configuration
- Fully TTL Compatible
- Common Data Input and Output Capability
- Three-State Outputs for OR-Tie Capability
- Power Dissipation MCM6641 Less Than 550 mW (Maximum) MCM66L41 Less Than 385 mW (Maximum)
- Standby Power Dissipation Less Than 125 mW (Typical)
- Plug In Replacement For TMS4044

MAXIMUM ACCESS TIME/MINIMUM CYCLE TIME

MCM6641-20 MCM66L41-20	200 ns	MCM6641-30 MCM66L41-30	300 ns
MCM6641-25 MCM66L41-25	250 ns	MCM6641-45 MCM66L41-45	450 ns

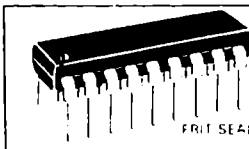
BLOCK DIAGRAM



MOS

(N-CHANNEL, SILICON-GATE)

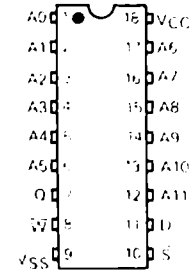
4096-BIT STATIC RANDOM ACCESS MEMORIES



C SUFFIX
FRIT SEAL CERAMIC PACKAGE
CASE 707-01

P SUFFIX
PLASTIC PACKAGE
CASE 707-02

PIN ASSIGNMENT



PIN NAMES	
A0-A11	Address Input
D	Data Input
Q	Data Output
S	Chip Select
VCC	Power Supply (+5 V)
VSS	Ground
W	Write Enable

TRUTH TABLE

S	W	D	Q	Mode
H	X	X	High Z	Not Selected
L	L	L	High Z	Write "0"
L	L	H	High Z	Write "1"
L	H	X	Output Data	Read

ADI4/5/2 /8

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Value	Unit
Temperature Under Bias	-10 to +80	°C
Voltage on Any Pin With Respect to V_{SS}	-0.5 to +7.0	Vdc
DC Output Current	20	mA
Power Dissipation	1.0	Watt
Operating Temperature Range	0 to +70	°C
Storage Temperature Range	-65 to +150	°C

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields, however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted)

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC} V_{SS}	4.5 0	5.0 0	5.5 0	V
Logic 1 Voltage, All Inputs	V_{IH}	2.0	–	6.0	V
Logic 0 Voltage, All Inputs	V_{IL}	-0.5	–	0.8	V

DC CHARACTERISTICS

Parameter	Symbol	MCM6641			MCM66L41			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Load Current (All Input Pins, V_{in} = 0 to 5.5 V)	I_{LI}	–	–	10	–	–	10	μA
Output Leakage Current (CS = 2.4 V, V_{in} = 0.4 to V_{CC})	$\|I_{LO}\|$	–	–	10	–	–	10	μA
Power Supply Current (V_{CC} = 5.5 V, I_{out} = 0 mA, T_A = 0°C)	I_{CC}		80	100	–	55	70	mA
Output Low Voltage, I_{OL} = 2.1 mA	V_{OL}	–	0.15	0.4	–	0.15	0.4	V
Output High Voltage, I_{OH} = 1.0 mA	V_{OH}	2.4	–	–	2.4	–		V
Output Short Circuit Current	I_{OS}*	–		40		–	40	mA

*Duration not to exceed 30 seconds

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, V_{CC} = 5.0 V, periodically sampled rather than 100% tested)

Characteristic	Symbol	Max	Unit
Input Capacitance (V_{in} = 0 V)	C_{in}	5.0	pF
Output Capacitance (V_{out} = 0 V)	C_{out}	10	pF

Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation $C = \Delta t / \Delta V$

STANDBY OPERATION

(Typical Supply Values)

Device	Supply	Operating	Standby	Max Standby Power
MCM6641	V_{CC}	+5 V	+2.4 V	225 mW
MCM66L41	V_{CC}	+5 V	+2.4 V	150 mW

AC OPERATING CONDITIONS AND CHARACTERISTICS

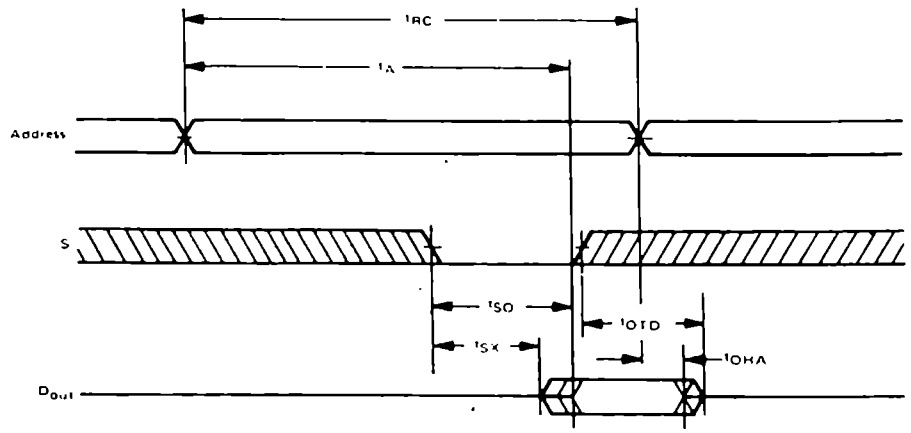
(Full operating voltage and temperature range unless otherwise noted)

Input Pulse Levels	0.8 Volt to 2.0 Volts	Input and Output Timing Levels	1.5 Volts
Input Rise and Fall Times	10 ns	Output Load	1 TTL Gate and C_L = 100 pF

READ (NOTE 1), WRITE (NOTE 2) CYCLES

Parameter	Symbol	MCM6641-20 MCM66L41-20		MCM6641-25 MCM66L41-25		MCM6641-30 MCM66L41-30		MCM6641-45 MCM66L41-45		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	200	–	250	–	300	–	450	–	ns
Access Time	t_A	–	200	–	250	–	300	–	450	ns
Chip Selection to Output Valid	t_{SO}	–	70	–	85	–	100	–	120	ns
Chip Selection to Output Active	t_{SX}	10	–	10	–	10	–	10	–	ns
Output 3-State From Deselection	t_{OTD}	–	40	–	60	–	80	–	100	ns
Output Hold From Address Change	t_{OHA}	50	–	50	–	50	–	50	–	ns
Write Cycle Time	t_{WC}	200	–	250	–	300	–	450	–	ns
Write Time	t_W	100	–	125	–	150	–	200	–	ns
Write Release Time	t_{WR}	0	–	0	–	0	–	0	–	ns
Output 3-State From Write	t_{OTW}	–	40	–	60	–	80	–	100	ns
Data to Write Time Overlap	t_{DW}	100	–	125	–	150	–	200	–	ns
Data Hold From Write Time	t_{DH}	0	–	0	–	0	–	0	–	ns

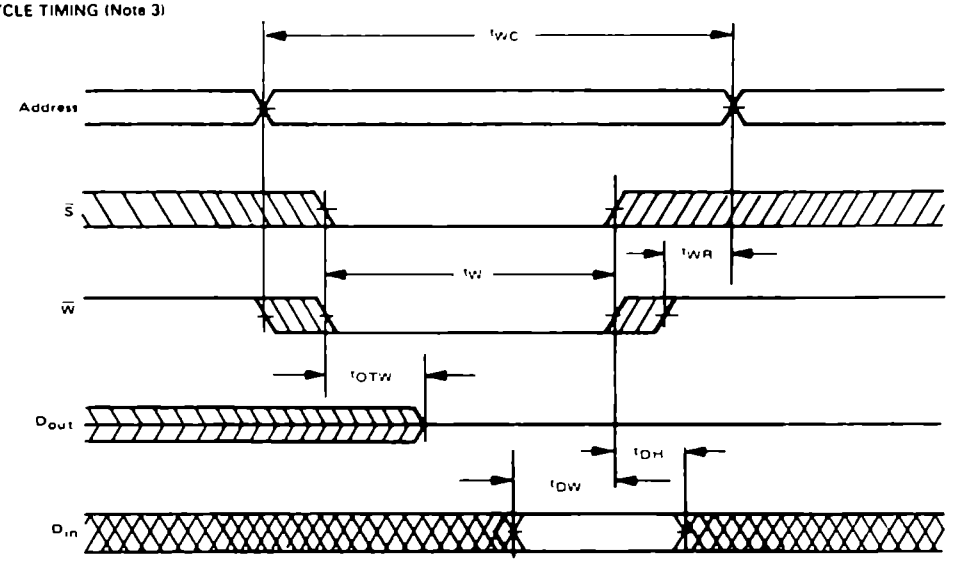
READ CYCLE TIMING
($\overline{W}$ HELD HIGH)



NOTES

1. A Read occurs during the overlap of a low $\overline{S}$ and a high $\overline{W}$.
2. A Write occurs during the overlap of a low $\overline{S}$ and a low $\overline{W}$.
3. If the $\overline{S}$ low transition occurs simultaneously with the $\overline{W}$ low transition, the output buffers remain in a high impedance state.

WRITE CYCLE TIMING (Note 3)



MOTOROLA

MCM6810
1.0 MHz
MCM68A10
1.5 MHz
MCM68B10
2.0 MHz

128 X 8-BIT STATIC RANDOM ACCESS MEMORY

The MCM6810 is a byte-organized memory designed for use in bus-organized systems. It is fabricated with N-channel silicon-gate technology. For ease of use, the device operates from a single power supply, has compatibility with TTL and DTL, and needs no clocks or refreshing because of static operation.

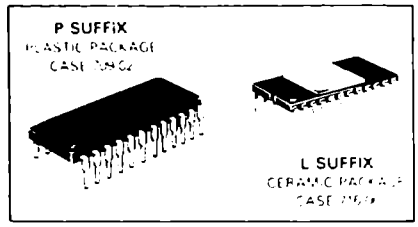
The memory is compatible with the M6800 Microcomputer Family, providing random storage in byte increments. Memory expansion is provided through multiple Chip Select inputs.

- Organized as 128 Bytes of 8 Bits
- Static Operation
- Bidirectional Three-State Data Input-Output
- Six Chip Select Inputs (Four Active Low, Two Active High)
- Single 5-Volt Power Supply
- TTL Compatible
- Maximum Access Time = 450 ns – MCM6810
  360 ns – MCM68A10
  250 ns – MCM68B10

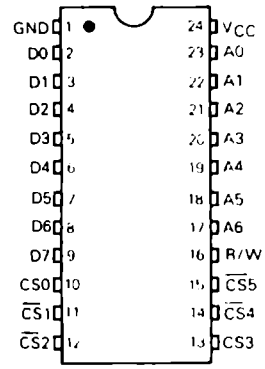
MOS

(N-CHANNEL, SILICON-GATE)

128 X 8-BIT STATIC RANDOM ACCESS MEMORY



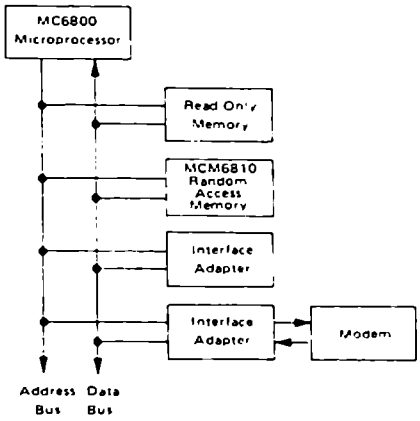
PIN ASSIGNMENT



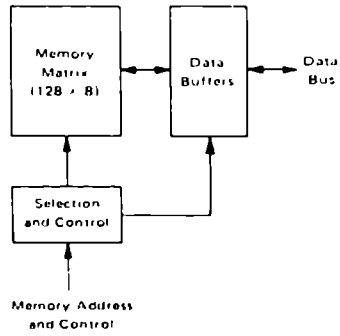
ORDERING INFORMATION

Speed	Device	Temperature Range
1.0 MHz	MC6810P, L	0 to 70°C
	MC6810CP, CL	-40 to +85°C
MIL-STD-883B	MC6810BJCS	-55 to +125°C
MIL-STD-883C	MC6810CJCS	
1.5 MHz	MC68A10P, L	0 to +70°C
	MC68A10CP, CL	-40 to +85°C
2.0 MHz	MC68B10P, L	0 to +70°C

M6800 MICROCOMPUTER FAMILY
BLOCK DIAGRAM



MCM6810 – RANDOM ACCESS MEMORY
BLOCK DIAGRAM



DS9487/7-78

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3 to +7.0	Vdc
Input Voltage	V_{in}	-0.3 to +7.0	Vdc
Operating Temperature Range	T_A	T_L to T_H 0 to 70 -40 to 85 -55 to 125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C
Thermal Resistance	θ_{JA}	82.5	°C/W

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V ±5%, V_{SS} = 0, T_A = T_L to T_H unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
Input Current (A_n, R/W, CS_n, $\overline{CS}_n$) (V_{in} = 0 to 5.25 V)		I_{in}	–	–	2.5	μAdc
Output High Voltage (I_{OH} = -205 μA)		V_{OH}	2.4	–	–	Vdc
Output Low Voltage (I_{OL} = 1.6 mA)		V_{OL}	–	–	0.4	Vdc
Output Leakage Current (Three-State) (CS = 0.8 V or $\overline{CS}$ = 2.0 V, V_{out} = 0.4 V to 2.4 V)		I_{TSI}	–	–	10	μAdc
Supply Current (V_{CC} = 5.25 V, all other pins grounded)	1.0 MHz 1.5, 2.0 MHz	I_{CC}	–	–	80 100	mAdc
Input Capacitance (A_n, R/W, CS_n, $\overline{CS}_n$) (V_{in} = 0, T_A = 25°C, f = 1.0 MHz)		C_{in}	–	–	7.5	pF
Output Capacitance (D_n) (V_{out} = 0, T_A = 25°C, f = 1.0 MHz, CSØ = 0)		C_{out}	–	–	12.5	pF

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Symbol	Min	Nom	Max	Unit
Input High Voltage	V_{IH}	2.0	–	5.25	Vdc
Input Low Voltage	V_{IL}	-0.3	–	0.8	Vdc

BLOCK DIAGRAM

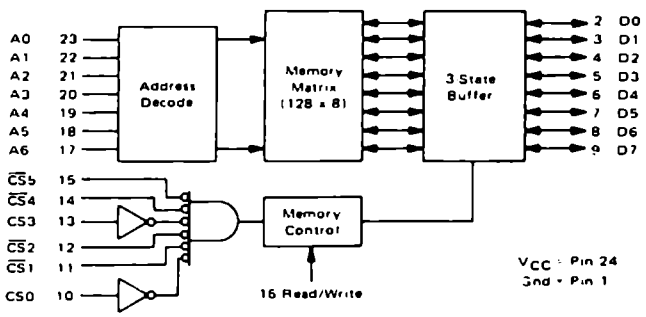
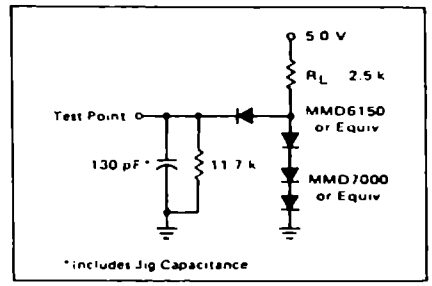


FIGURE 1 – AC TEST LOAD



AC TEST CONDITIONS

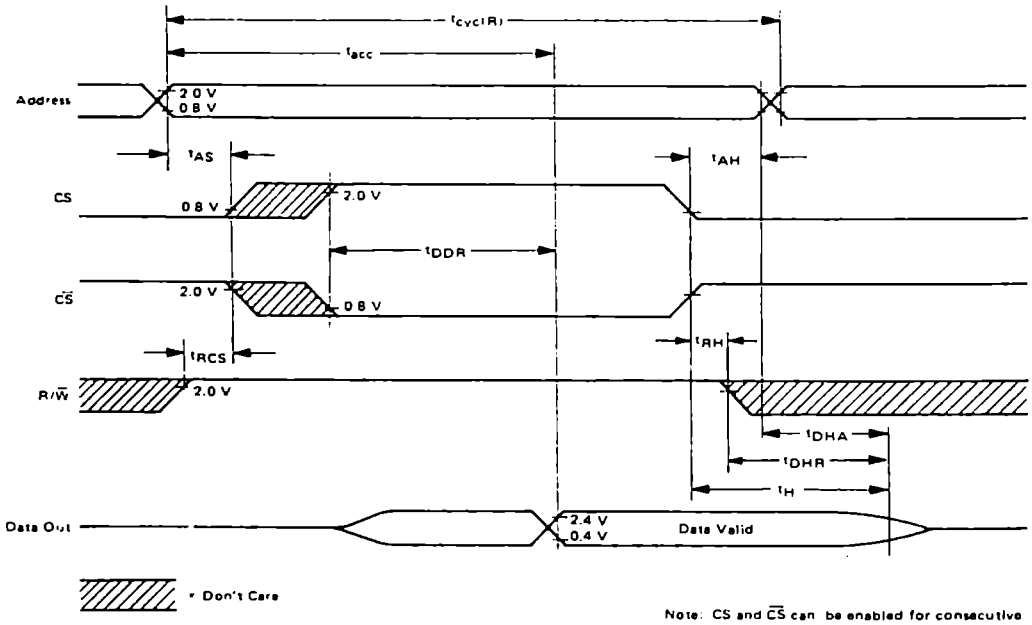
Condition	Value
Input Pulse Levels	0.8 V to 2.0 V
Input Rise and Fall Times	20 ns
Output Load	See Figure 1

AC OPERATING CONDITIONS AND CHARACTERISTICS

READ CYCLE (V_{CC} = 5.0 V ± 5%, V_{SS} = 0, T_A = T_L to T_H unless otherwise noted.)

Characteristic	Symbol	MCM6810		MCM68A10		MCM68B10		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	$t_{cyc(R)}$	450	–	360	–	250	–	ns
Access Time	t_{acc}	–	450	–	360	–	250	ns
Address Setup Time	t_{AS}	20	–	20	–	20	–	ns
Address Hold Time	t_{AH}	0	–	0	–	0	–	ns
Data Delay Time (Read)	t_{DDR}	–	230	–	220	–	180	ns
Read to Select Delay Time	t_{RCS}	0	–	0	–	0	–	ns
Data Hold from Address	t_{DHA}	10	–	10	–	10	–	ns
Output Hold Time	t_H	10	–	10	–	10	–	ns
Data Hold from Read	t_{DHR}	10	80	10	60	10	60	ns
Read Hold from Chip Select	t_{RH}	0	–	0	–	0	–	ns

READ CYCLE TIMING

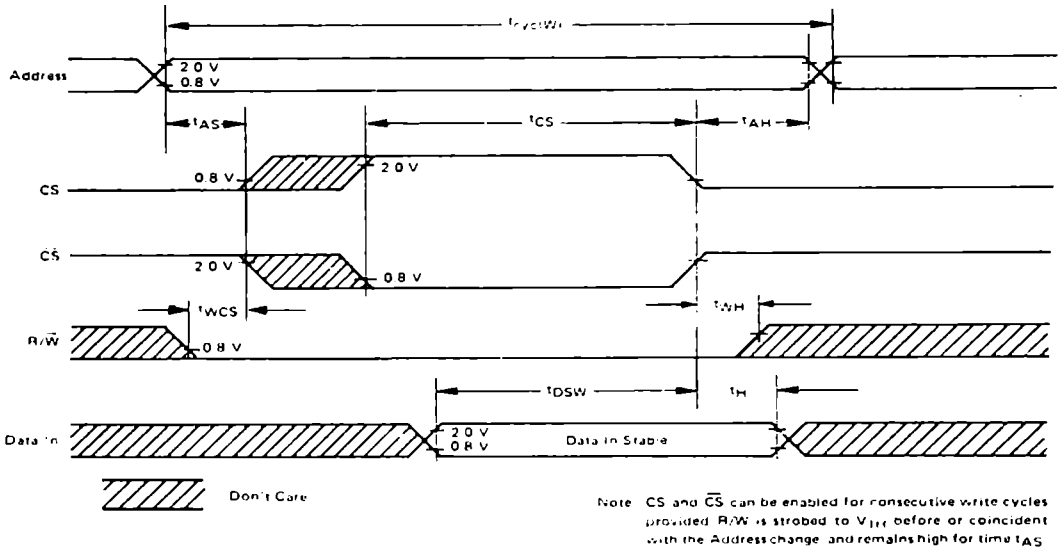


Note: CS and $\overline{CS}$ can be enabled for consecutive read cycles provided R/W remains at V_{IH}.

WRITE CYCLE (V_{CC} = 5.0 V ±5%, V_{SS} = 0, T_A = T_L to T_H unless otherwise noted.)

Characteristic	Symbol	MCM6810		MCM68A10		MCM68B10		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{cycWr}	450		360	--	250	-	ns
Address Setup Time	t_{AS}	20	–	20	--	20	--	ns
Address Hold Time	t_{AH}	0		0	--	0	–	ns
Chip Select Pulse Width	t_{CS}	300	–	250	–	210	–	ns
Write to Chip Select Delay Time	t_{WCS}	0	–	0	-	0		ns
Data Setup Time (Write)	t_{DSW}	190	-	80	--	60	–	ns
Input Hold Time	t_H	10	–	10	–	10	–	ns
Write Hold Time from Chip Select	t_{WH}	0	-					

WRITE CYCLE TIMING



Note: CS and $\overline{CS}$ can be enabled for consecutive write cycles provided R/W is strobed to V_{IH} before or coincident with the Address change and remains high for time t_{AS}.

MOTOROLA

MCM2532
MCM25L32

4096 × 8-BIT UV ERASABLE PROM

The MCM2532/25L32 is a 32,768-bit Erasable and Electrically Reprogrammable PROM designed for system debug usage and similar applications requiring nonvolatile memory that could be reprogrammed periodically. The transparent window in the package allows the memory content to be erased with ultraviolet light.

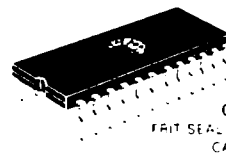
For ease of use, the device operates from a single power supply and has static power-down mode. Pin-for-pin compatible mask programmable ROMs are available for large volume production runs of systems initially using the MCM2532.

- Single +5 V Power Supply
- Organized as 4096 Bytes of 8 Bits
- Automatic Power-Down Mode (Standby)
- Fully Static Operation (No Clocks)
- TTL Compatible During Both Read and Program
- Maximum Access Time = 450 ns MCM2532
  350 ns MCM2532-35
  250 ns MCM2532-25
- Pin Compatible with MCM68A332 Mask Programmable ROMs
- Low Power Version
  MCM25L32 Active – 50 mA Max
  Standby – 10 mA Max
  MCM25L32-25 Active – 70 mA
  Standby – 15 mA

MOS

(N-CHANNEL, SILICON-GATE)

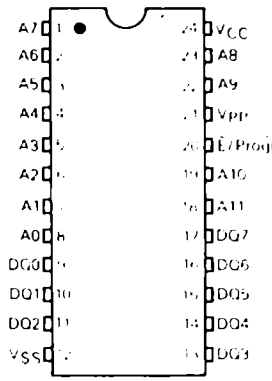
4096 × 8-BIT
UV ERASABLE PROM



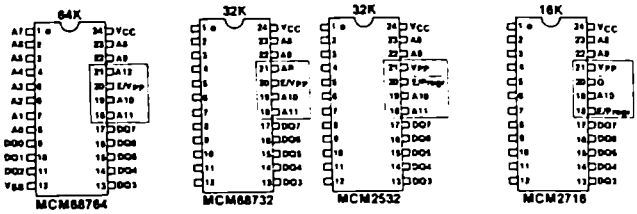
C SUFFIX
FRIT SEAL CERAMIC PACKAGE
CASE 623A-02

L SUFFIX CERAMIC PACKAGE
ALSO AVAILABLE – CASE 716

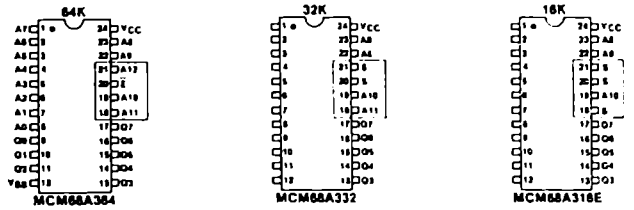
PIN ASSIGNMENT



MOTOROLA'S PIN-COMPATIBLE EPROM FAMILY



MOTOROLA'S PIN-COMPATIBLE ROM FAMILY



INDUSTRY STANDARD PINOUTS

*PIN NAMES	
A	Address
DQ	Data Input/Output
Ē/Progr	Dual Function Enable (Power Down/Program Pulse)

*New industry standard nomenclature

DS9816/4 80

ABSOLUTE MAXIMUM RATINGS

Rating	Value	Unit
Temperature Under Bias	- 10 to + 80	°C
Operating Temperature Range	0 to + 70	C
Storage Temperature	- 65 to + 125	°C
All Input/Output Voltages with Respect to V_{SS}	+ 6 to - 0.3	Vdc
Vpp Supply Voltage with Respect to V_{SS}	+ 28 to - 0.3	Vdc

NOTE Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields, however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

MODE SELECTION

Mode	Pin Number				
	9-11, 13-17 DQ	12 V_{SS}	20 $\overline{E}$/Progr	21 V_{PP}	24 V_{CC}
Read	Data Out	V_{SS}	V_{IL}	5 V	V_{CC}
Output Disable	High Z	V_{SS}	V_{IH}	5 to 25 V	V_{CC}
Standby	High Z	V_{SS}	V_{IH}	5 V	V_{CC}
Program	Data In	V_{SS}	Pulsed V_{IH} to V_{IL}	V_{PPH}	V_{CC}
Program Verify	Data Out	V_{SS}	V_{IL}	5 V	V_{CC}
Program Inhibit	High Z	V_{SS}	V_{IH}	V_{PPH}	V_{CC}

BLOCK DIAGRAM

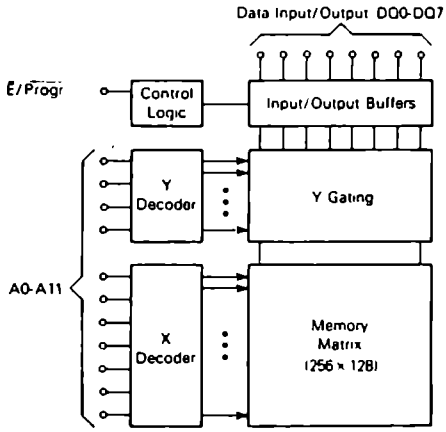
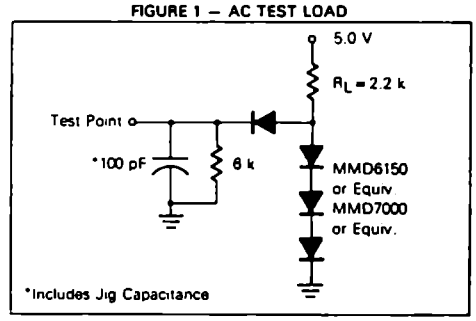


FIGURE 1 — AC TEST LOAD



CAPACITANCE (f = 1.0 MHz, T_A = 25°C, periodically sampled rather than 100% tested.)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance (V_{in} = 0 V)	C_{in}	4.0	6.0	pF
Output Capacitance (V_{out} = 0 V)	C_{out}	8.0	12	pF

Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation $C = I\Delta_t/\Delta V$.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Fully operating voltage and temperature range unless otherwise noted)

RECOMMENDED DC OPERATING CONDITIONS

Parameter		Symbol	Min	Typ	Max	Unit
Supply Voltage*	MCM25L32/MCM2532	V_{CC}	4.75	5.0	5.25	Vdc
	MCM2532-35/MCM2532-25		4.5	5.0	5.5	
	MCM25L32-35/MCM25L32-25	V_{PP}	V_{CC} – 0.6	5.0	V_{CC} + 0.6	
Input High Voltage		V_{IH}	2.2	–	V_{CC} + 1.0	Vdc
Input Low Voltage		V_{IL}	– 0.1	–	0.65	Vdc

RECOMMENDED DC OPERATING CHARACTERISTICS

Characteristic		Condition	Symbol	MCM2532		MCM25L32		Unit
				Min	Max	Min	Max	
Address and $\overline{E}$ Input Sink Current		V_{in} = 5.25 V	I_{in}	–	10	–	10	μA
Output Leakage Current		V_{out} = 5.25 V	I_{LO}	–	10	–	10	μA
V_{CC} Supply Current* (Standby)	MCM2532 MCM2532-35	$\overline{E} = V_{IH}$	I_{CC1}	–	25	–	10	mA
V_{CC} Standby Current* (Standby)	MCM2532-25	$\overline{E} = V_{IH}$	I_{CC1}	–	25	–	15	mA
V_{CC} Supply Current* (Active)	MCM2532 MCM2532-35	$\overline{E} = V_{IL}$	I_{CC2}	–	100	–	50	mA
V_{CC} Supply Current* (Active)	MCM2532-25	$\overline{E} = V_{IL}$	I_{CC2}	–	120	–	70	mA
V_{PP} Supply Current*		V_{PP} = 5.85 V	I_{PP1}	–	5.0	–	5.0	mA
Output Low Voltage		I_{OL} = 2.1 mA	V_{OL}	–	0.45	–	0.45	V
Output High Voltage		I_{OH} = – 400 μA	V_{OH}	2.4	–	2.4	–	V

*V_{CC} must be applied simultaneously or prior to V_{PP}. V_{CC} must also be switched off simultaneously with or after V_{PP}. With V_{PP} connected directly to V_{CC} during the read operation, the supply current would be the sum of I_{PP1} and I_{CC}. The additional 0.6 V tolerance on V_{PP} makes it possible to use a driver circuit for switching V_{PP} supply from V_{CC} in Read mode to +25 V for programming. Typical values are for T_A = 25°C and nominal supply voltages.

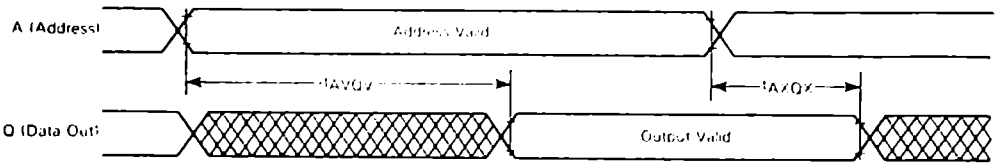
AC READ OPERATING CONDITIONS AND CHARACTERISTICS

(Full Operating Voltage and Temperature Range Unless Otherwise Noted)

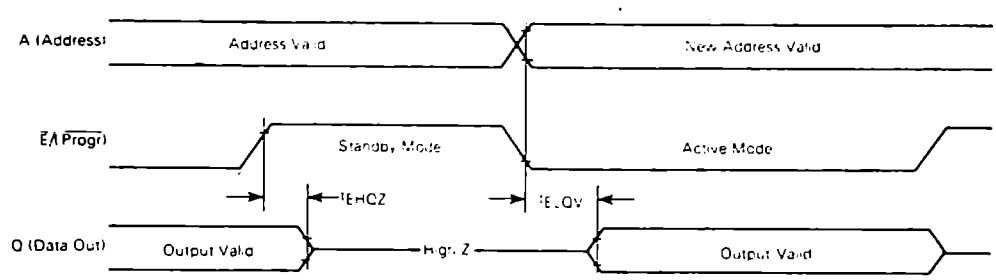
Input Pulse Levels . . . . . 0.65 Volt and 2.2 Volts
Input Rise and Fall Times . . . . . 20 ns
Input and Output Timing Levels . . . . . 0.8 and 2.0 Volts
Output Load . . . . . See Figure 1

Characteristic	Symbol	MCM2532-25		MCM2532-35		MCM2532		Unit
		Min	Max	Min	Max	Min	Max	
Address Valid to Output Valid ($\overline{E}/\overline{Progr} = V_{IL}$)	t_{AVQV}	–	250	–	350	–	450	ns
$\overline{E}$ to Output Valid	t_{ELQV}	–	250	–	350	–	450	ns
$\overline{E}$ to High Z Output	t_{EHQZ}	0	100	0	100	0	100	ns
Data Hold from Address ($\overline{E} = V_{IL}$)	t_{AXDX}	0	–	0	–	0	–	ns

READ MODE TIMING DIAGRAMS ($\overline{E}$ = V_{IL})



STANDBY MODE



DC PROGRAMMING CONDITIONS AND CHARACTERISTICS

(T_A = 25°C ± 5°C)

RECOMMENDED PROGRAMMING OPERATION CONDITIONS

Parameter	Symbol	Min	Nom	Max	Unit
Supply Voltage	V_{CC}, V_{PPL} V_{PPH}	4.75 24	5.0 25	5.25 26	Vdc
Input High Voltage for Data	V_{IH}	2.2	–	V_{CC} + 1	Vdc
Input Low Voltage for Data	V_{IL}	−0.1	–	0.65	Vdc

*V_{CC} must be applied simultaneously or prior to V_{PP}. V_{CC} must also be switched off simultaneously with or after V_{PP}. The device must not be inserted into or removed from a board with V_{PP} at + 25 V. V_{PP} must not exceed the + 26 V maximum specifications.

PROGRAMMING OPERATION DC CHARACTERISTICS

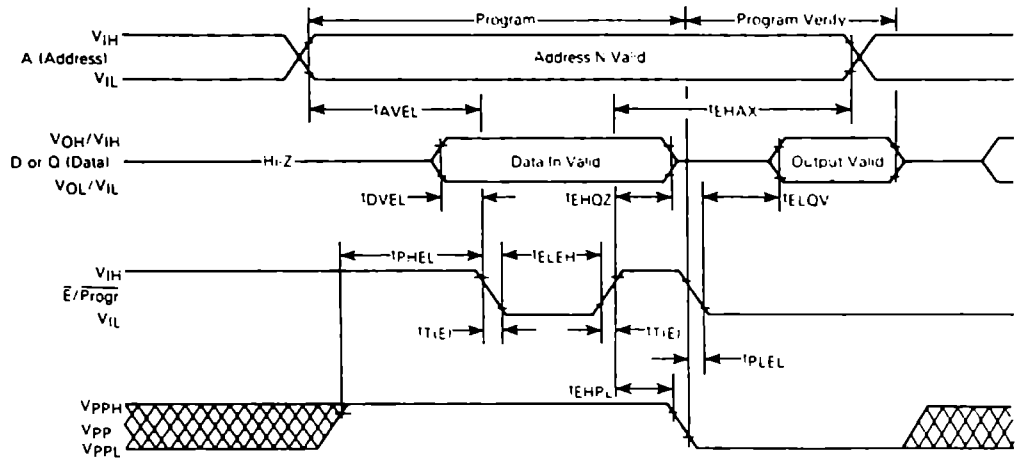
Characteristic	Condition	Symbol	Min	Typ	Max	Unit
Address and $\overline{E}/\overline{Progr}$ Input Sink Current	V_{in} = 5.25 V/0.45 V	I_{LI}	–	–	10	μAdc
V_{PP} Supply Current (V_{PP} = 25 V ± 1 V)	$\overline{E}/\overline{Progr}$ = V_{IH}	I_{PP1}	–	–	10	mAdc
V_{PP} Programming Pulse Supply Current (V_{PP} = 25 V ± 1 V)	$\overline{E}$, $\overline{Progr}$ = V_{IL}	I_{PP2}	–	–	30	mAdc
V_{CC} Supply Current – MCM2532	–	I_{CC}	–	–	160	mAdc

AC PROGRAMMING OPERATING CONDITIONS AND CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit
Address Setup Time	t_{AVEL}	2.0	–	μs
V_{PP} Setup Time	t_{PHEL}	0	–	ns
Data Setup Time	t_{DVEL}	2.0	–	μs
Address Hold Time	t_{EHAX}	2.0	–	μs
V_{PP} to Enable Low Time	t_{PLEL}	0	–	ns
Data Hold Time	t_{EHQZ}	2.0	–	μs
V_{PP} Hold Time	t_{EHPL}	0	–	ns
Enable (Program) Active Time	t_{ELEH}	1*	55	ms
Enable ($\overline{E}$/Progr) Pulse Transition Time	$t_{T(PE)}$	5	–	ns
V_{PP} Rise and Fall Time from 5 to 25 V	t_R, t_F	0.5	2	μs

*If shorter than 45 ms (min) pulses are used, the same number of pulses should be applied after the specific data has been verified.

PROGRAMMING OPERATION TIMING DIAGRAM



PROGRAMMING INSTRUCTIONS

After the completion of an ERASE operation, every bit in the device is in the "1" state (represented by Output High). Data are entered by programming zeros (Output Low) into the required bits. The words are addressed the same way as in the READ operation. A programmed "0" can only be changed to a "1" by ultraviolet light erasure.

To set the memory up for PROGRAM mode, the V_{PP} input (pin 21) should be raised to +25 V. The V_{CC} supply voltage is the same as for the READ operation. Programming data is entered in 8-bit words through the data out (DQ) terminals while $\overline{E}/\overline{Progr}$ is high. Only "0's" will be programmed when "0's" and "1's" are entered in the data word.

After address and data setup, a 50 ms program pulse (V_{IH} to V_{IL}) is applied to the $\overline{E}/\overline{Progr}$ input. A program pulse is applied to each address location to be programmed. To minimize programming time, a 2 ms pulse width is recommended. The maximum program pulse width is 55 ms, therefore, programming must not be attempted with a dc signal applied to the $\overline{E}/\overline{Progr}$ input.

Multiple MCM2532s may be programmed in parallel with the same data by connecting together like inputs and applying the program pulse to the $\overline{E}/\overline{Progr}$ inputs. Different data may be programmed into multiple MCM2532s connected in parallel by using the PROGRAM INHIBIT mode. Except for the $\overline{E}/\overline{Progr}$ pin, all like inputs may be common.

PROGRAM VERIFY for the MCM2532 is the read operation.

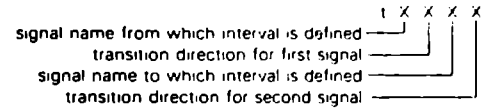
READ OPERATION

After access time, data is valid at the outputs in the READ mode.

ERASING INSTRUCTIONS

The MCM2532/25L32 can be erased by exposure to high intensity shortwave ultraviolet light, with a wave-length of 2537 angstroms. The recommended integrated dose (i.e., UV-intensity X exposure time) is 15 Ws/cm^2. As an example, using the "Model 30-000" UV-Eraser Turner Designs, Mountain View, CA94043) the ERASE-time is 36 minutes. The lamps should be used without shortwave filters and the MCM2532/25L32 should be positioned about one inch away from the UV-tubes.

TIMING PARAMETER ABBREVIATIONS


t X X X X
signal name from which interval is defined
transition direction for first signal
signal name to which interval is defined
transition direction for second signal

The transition definitions used in this data sheet are

- H = transition to high
- L = transition to low
- V = transition to valid
- X = transition to invalid or don't care
- Z = transition to off (high impedance)

TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

WAVEFORMS

Waveform Symbol	Input	Output
	Must Be Valid	Will Be Valid
	Change From H to L	Will Change From H to L
	Change From L to H	Will Change From L to H
	Don't Care Any Change Permitted	Changing State Unknown
		High Impedance

MOTOROLA

MCM2708
MCM27A08

1024 X 8 ERASABLE PROM

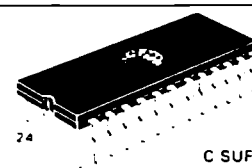
The MCM2708 27A08 is an 8192-bit Erasable and Electrically Reprogrammable PROM designed for system debug usage and similar applications requiring nonvolatile memory that could be reprogrammed periodically. The transparent window on the package allows the memory content to be erased with ultraviolet light. Pin-for-pin mask programmable ROMs are available for large volume production runs of systems initially using the MCM2708 27A08.

- Organized as 1024 Bytes of 8 Bits
- Static Operation
- Standard Power Supplies of +12 V, +5 V and -5 V
- Maximum Access Time = 300 ns – MCM27A08
  450 ns – MCM2708
- Low Power Dissipation
- Chip Select Input for Memory Expansion
- TTL Compatible
- Three-State Outputs
- Pin Equivalent to the 2708
- Pin-for-Pin Compatible to MCM65308, MCM68308 or 2308 Mask-Programmable ROMs

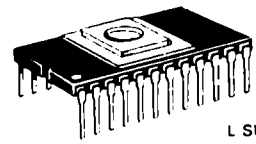
MOS

(N-CHANNEL, SILICON-GATE)

1024 X 8-BIT
UV ERASABLE PROM



C SUFFIX
FRIT SEAL CERAMIC PACKAGE
CASE 623A-02



L SUFFIX
CERAMIC PACKAGE
CASE 716-07

PIN CONNECTION DURING READ OR PROGRAM

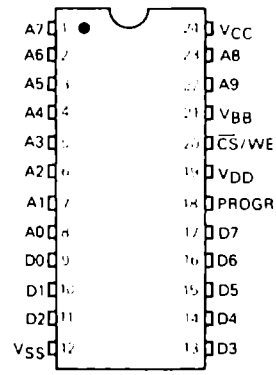
Mode	Pin Number						
	9-11, 13-17	12	18	19	20	21	24
Read	D_{out}	V_{SS}	V_{SS}	V_{DD}	V_{IL}	V_{BB}	V_{CC}
Program	Din	V_{SS}	Pulsed V_{IHP}	V_{DD}	V_{IHW}	V_{BB}	V_{CC}

ABSOLUTE MAXIMUM RATINGS (1)

Rating	Value	Unit
Operating Temperature	0 to +70	°C
Storage Temperature	-65 to +125	°C
V_{DD} with Respect to V_{BB}	+20 to -0.3	Vdc
V_{CC} and V_{SS} with Respect to V_{BB}	+15 to -0.3	Vdc
All Input or Output Voltages with Respect to V_{BB} during Read	+15 to -0.3	Vdc
$\overline{CS}/WE$ Input with Respect to V_{BB} during Programming	+20 to -0.3	Vdc
Program Input with Respect to V_{BB}	+35 to -0.3	Vdc
Power Dissipation	1.8	Watts

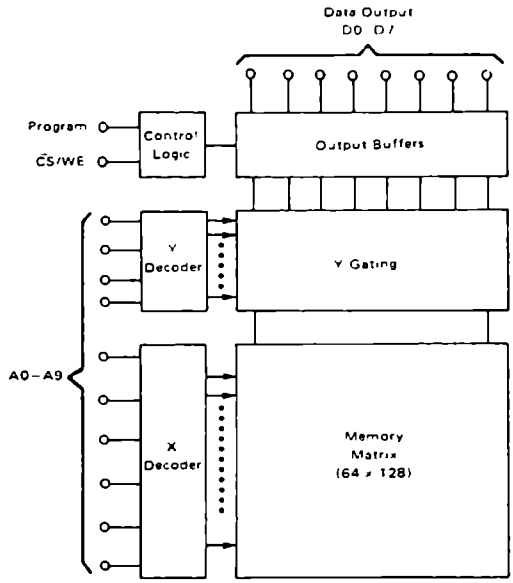
Note 1:
Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

PIN ASSIGNMENT



DS9440 R2/1-79

BLOCK DIAGRAM



DC READ OPERATING CONDITIONS AND CHARACTERISTICS
(Full operating voltage and temperature range unless otherwise noted.)

RECOMMENDED DC READ OPERATING CONDITIONS

Parameter	Symbol	Min	Nom	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	Vdc
	V_{DD}	11.4	12	12.6	Vdc
	V_{BB}	-5.25	-5.0	-4.75	Vdc
Input High Voltage	V_{IH}	3.0	–	V_{CC} + 1.0	Vdc
Input Low Voltage	V_{IL}	V_{SS}	–	0.65	Vdc

READ OPERATION DC CHARACTERISTICS

Characteristic		Condition	Symbol	Min	Typ	Max	Unit
Address and CS Input Sink Current		V_{in} = 5.25 V or V_{in} = V_{IL}	I_{in}	-	1	10	μA
Output Leakage Current		V_{out} = 5.25 V, $\overline{CS}$/WE = 5 V	I_{LO}	-	1	10	μA
V_{DD} Supply Current		Worst-Case Supply Currents	I_{DD}	-	50	65	mA
V_{CC} Supply Current	(Note 2)	All Inputs High	I_{CC}	-	6	10	mA
V_{BB} Supply Current		$\overline{CS}$/WE = 5.0 V, T_A = 0°C	I_{BB}	-	30	45	mA
Output Low Voltage		I_{OL} = 1.6 mA	V_{OL}	–	–	0.45	V
Output High Voltage		I_{OH} = -100 μA	$V_{OH}1$	3.7	–	–	V
Output High Voltage		I_{OH} = -1.0 mA	$V_{OH}2$	2.4	–	–	V
Power Dissipation	(Note 2)	T_A 70°C	P_D	-	–	800	mW

Note 2:
The total power dissipation is specified at 800 mW. It is not calculable by summing the various current (I_{DD}, I_{CC}, and I_{BB}) multiplied by their respective voltages, since current paths exist between the various power supplies and V_{SS}. The I_{DD}, I_{CC}, and I_{BB} currents should be used to determine power supply capacity only.

V_{BB} must be applied prior to V_{CC} and V_{DD}. V_{BB} must also be the last power supply switched off.

AC READ OPERATING CONDITIONS AND CHARACTERISTICS
(Full operating voltage and temperature range unless otherwise noted.)
(All timing with $t_r = t_f = 20$ ns, Load per Note 3)

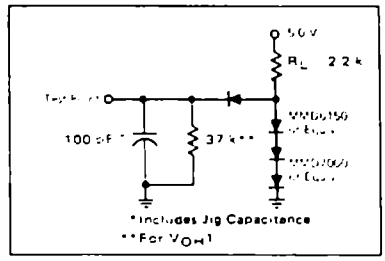
Characteristic	Symbol	MCM27A08			MCM2708			Unit
		Min	Typ	Max	Min	Typ	Max	
Address to Output Delay	t_{AO}	–	220	300	–	280	450	ns
Chip Select to Output Delay	t_{CO}	–	60	120	–	60	120	ns
Data Hold from Address	t_{DHA}	0	–	–	0	–	–	ns
Data Hold from Deselection	t_{DHD}	0	–	120	0	–	120	ns

CAPACITANCE (periodically sampled rather than 100% tested.)

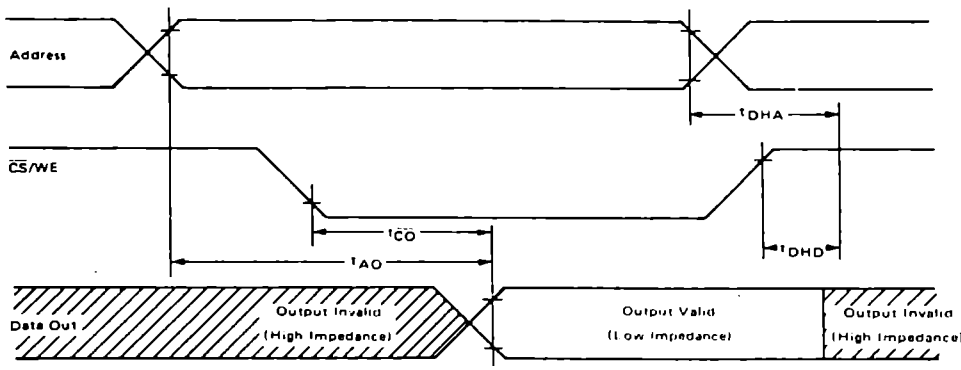
Characteristic	Condition	Symbol	Typ	Max	Unit
Input Capacitance (f = 1.0 MHz)	V_{in} = 0 V, T_A = 25°C	C_{in}	4.0	6.0	pF
Output Capacitance (f = 1.0 MHz)	V_{out} = 0 V, T_A = 25°C	C_{out}	8.0	12	pF

Note 3:
Output Load = 1 TTL Gate and C_L = 100 pF (Includes Jig Capacitance)
Timing Measurement Reference Levels Inputs 0.8 V and 2.8 V
Outputs 0.8 V and 2.4 V

AC TEST LOAD



READ OPERATION TIMING DIAGRAM



DC PROGRAMMING CONDITIONS AND CHARACTERISTICS
(Full operating voltage and temperature range unless otherwise noted.)

RECOMMENDED PROGRAMMING OPERATING CONDITIONS

Parameter	Symbol	Min	Nom	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	Vdc
	V_{DD}	11.4	12	12.6	Vdc
	V_{BB}	-5.25	-5.0	-4.75	Vdc
Input High Voltage for All Addresses and Data	V_{IH}	3.0	–	V_{CC} + 1.0	Vdc
Input Low Voltage (except Program)	V_{IL}	V_{SS}	–	0.65	Vdc
$\overline{CS}$/WE Input High Voltage (Note 4)	V_{IHW}	11.4	12	12.6	Vdc
Program Pulse Input High Voltage (Note 4)	V_{IHP}	25	–	27	Vdc
Program Pulse Input Low Voltage (Note 5)	V_{ILP}	V_{SS}	–	1.0	Vdc

Note 4: Referenced to V_{SS}.
Note 5: $V_{IHP} - V_{ILP} = 25$ V min.

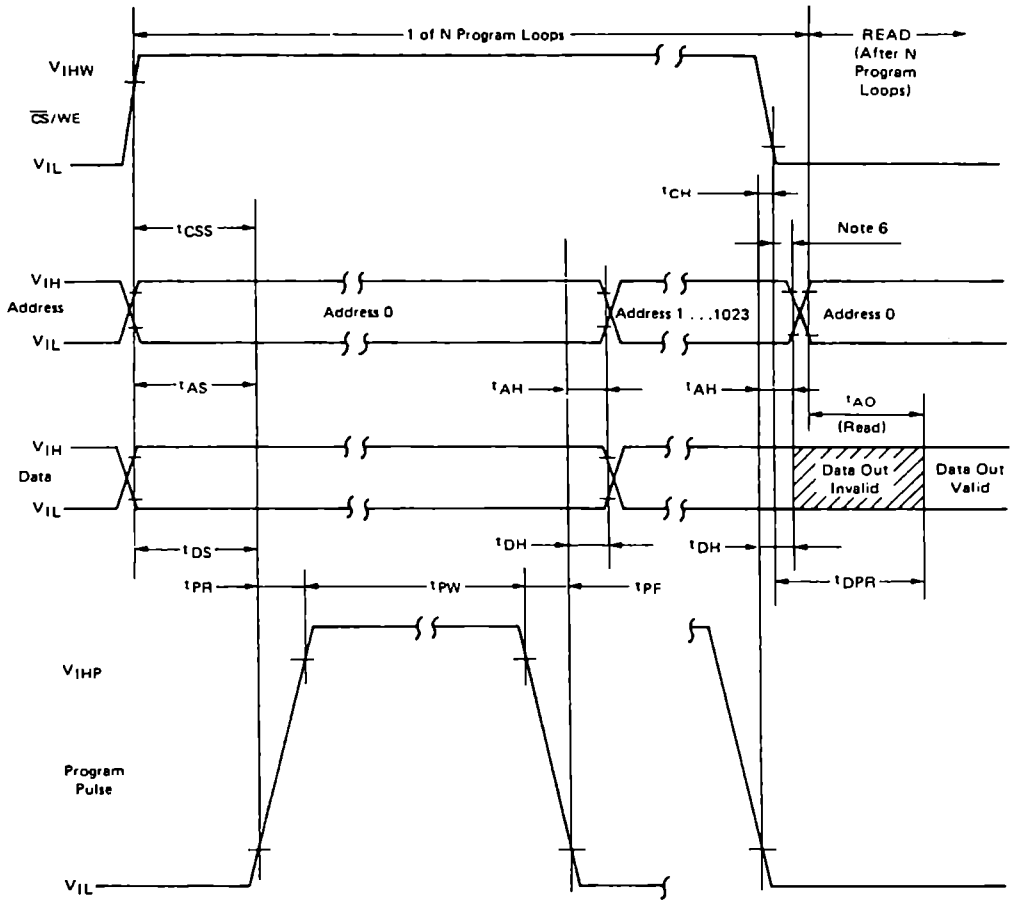
PROGRAMMING OPERATION DC CHARACTERISTICS

Characteristic	Condition	Symbol	Min	Typ	Max	Unit
Address and $\overline{CS}$/WE Input Sink Current	$V_{in} = 5.25$ V	I_{LI}	–	–	10	μAdc
Program Pulse Source Current		I_{IPL}	–	–	3.0	mAdc
Program Pulse Sink Current		I_{IPH}	–	–	20	mAdc
V_{DD} Supply Current	Worst-Case Supply Currents	I_{DD}	–	50	65	mAdc
V_{CC} Supply Current	All Inputs High	I_{CC}	–	6	10	mAdc
V_{BB} Supply current	$\overline{CS}$/WE = 5 V, $T_A = 0°C$	I_{BB}	–	30	45	mAdc

AC PROGRAMMING OPERATING CONDITIONS AND CHARACTERISTICS
(Full operating voltage and temperature unless otherwise noted.)

Characteristic	Symbol	Min	Max	Unit
Address Setup Time	t_{AS}	10	–	μs
$\overline{CS}$/WE Setup Time	t_{CSS}	10	–	μs
Data Setup Time	t_{DS}	10	–	μs
Address Hold Time	t_{AH}	1.0	–	μs
$\overline{CS}$/WE Hold Time	t_{CH}	0.5	–	μs
Data Hold Time	t_{DH}	1.0	–	μs
Chip Deselect to Output Float Delay	t_{DF}	0	120	ns
Program to Read Delay	t_{DPR}	–	10	μs
Program Pulse Width	t_{PW}	0.1	1.0	ms
Program Pulse Rise Time	t_{PR}	0.5	2.0	μs
Program Pulse Fall Time	t_{PF}	0.5	2.0	μs

PROGRAMMING OPERATION TIMING DIAGRAM



Note 6: The $\overline{CS}$/WE transition must occur after the Program Pulse transition and before the Address Transition.

PROGRAMMING INSTRUCTIONS

After the completion of an ERASE operation, every bit in the device is in the "1" state (represented by Output High). Data are entered by programming zeros (Output Low) into the required bits. The words are addressed the same way as in the READ operation. A programmed "0" can only be changed to a "1" by ultraviolet light erasure.

To set the memory up for programming mode, the $\overline{CS}$/WE input (Pin 20) should be raised to +12 V. Programming data is entered in 8-bit words through the data output terminals (D0 to D7).

Logic levels for the data lines and addresses and the supply voltages (V_{CC}, V_{DD}, V_{BB}) are the same as for the READ operation.

After address and data setup one program pulse per address is applied to the program input (Pin 18). A program loop is a full pass through all addresses. Total programming time, $T_{Ptotal} = N \times t_{PW} \geq 100$ ms. The required number of program loops (N) is a function of the program pulse width (t_{PW}), where: $0.1 \text{ ms} \leq t_{PW} \leq 1.0$ ms; correspondingly N is: $100 \leq N \leq 1000$. There must be N successive loops through all 1024 addresses. It is not permitted to apply more than one program pulse in succession to the same address (i.e., N program pulses to an address and then change to the next address to be programmed). At the end of a program sequence the $\overline{CS}$/WE falling edge transition must occur before the first address transition, when changing from a PROGRAM to a READ cycle. The program pin (Pin 18) should be pulled down to V_{ILP} with an active device, because this pin sources a small amount of current (I_{IPL}) when $\overline{CS}$/WE is at V_{IHW} (12 V) and the program pulse is at V_{ILP}.

EXAMPLES FOR PROGRAMMING

Always use the $T_{Ptotal} = N \times t_{PW} \geq 100$ ms relationship.

1. All 8192 bits should be programmed with a 0.2 ms program pulse width.

   The minimum number of program loops:

   $$N = \frac{T_{Ptotal}}{t_{PW}} = \frac{100 \text{ ms}}{0.2 \text{ ms}} = 500$$ One program loop consists of words 0 to 1023.

2. Words 0 to 200 and 300 to 700 are to be programmed. All other bits are "don't care". The program pulse width is 0.5 ms. The minimum number of program loops, $N = \frac{100}{0.5} = 200$. One program loop consists of words 0 to 1023. The data entered into the "don't care" bits should be all 1s.
3. Same requirements as example 2, but the EPROM is now to be updated to include data for words 850 to 880. The minimum number of program loops is the same as in the previous example, N = 200. One program loop consists of words 0 to 1023. The data entered into the "don't care" bits should be all 1s. Addresses 0 to 200 and 300 to 700 must be reprogrammed with their original data pattern.

ERASING INSTRUCTIONS

The MCM2708/27A08 can be erased by exposure to high intensity shortwave ultraviolet light, with a wavelength of 2537 Å. The recommended integrated dose (i.e., UV-intensity x exposure time) is 12.5 Ws/cm^2. As an example, using the "Model 30-000" UV-Eraser (Turner Designs, Mountain View, CA94043) the ERASE-time is 30 minutes. The lamps should be used without shortwave filters and the MCM2708/27A08 should be positioned about one inch away from the UV-tubes.

MOTOROLA

MCM2716
MCM27L16

2048 × 8-BIT UV ERASABLE PROM

The MCM2716/27L16 is a 16,384-bit Erasable and Electrically Reprogrammable PROM designed for system debug usage and similar applications requiring nonvolatile memory that could be reprogrammed periodically. The transparent lid on the package allows the memory content to be erased with ultraviolet light.

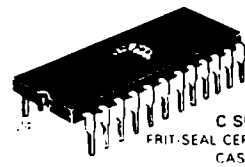
For ease of use, the device operates from a single power supply and has a static power-down mode. Pin-for-pin mask programmable ROMs are available for large volume production runs of systems initially using the MCM2716/27L16.

- Single 5 V Power Supply
- Automatic Power-down Mode (Standby)
- Organized as 2048 Bytes of 8 Bits
- Low Power Version 27L16/27L16-35 Active 50 mA Max
  Standby 10 mA Max
  27L16-25 Active 70 mA Max
  Standby 15 mA Max
- TTL Compatible During Read and Program
- Maximum Access Time = 450 ns MCM2716
  350 ns MCM2716-35
  250 ns MCM2716-25
- Pin Equivalent to Intel's 2716
- Pin Compatible to MCM68A316E
- Output Enable Active Level is User Selectable

MOS

(N-CHANNEL, SILICON-GATE)

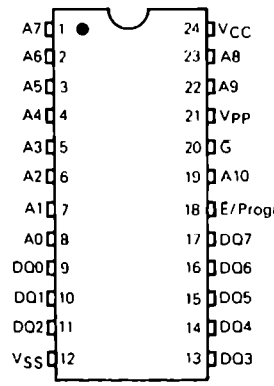
2048 × 8-BIT
UV ERASABLE PROM



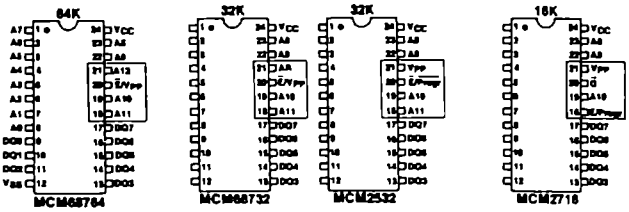
C SUFFIX
FRIT-SEAL CERAMIC PACKAGE
CASE 623A

L SUFFIX CERAMIC PACKAGE
ALSO AVAILABLE — CASE 716

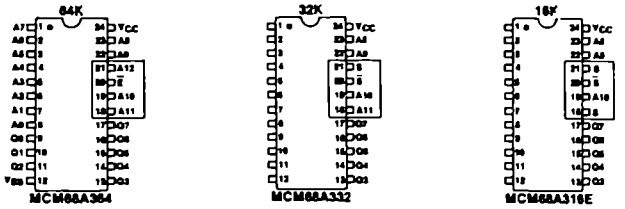
PIN ASSIGNMENT



MOTOROLA'S PIN-COMPATIBLE EPROM FAMILY



MOTOROLA'S PIN-COMPATIBLE ROM FAMILY



INDUSTRY STANDARD PINOUTS

*Pin Names	
A	Address
DQ	Data Input/Output
E/Progr	Chip Enable/Program
G	Output Enable

*New industry standard nomenclature

DS9817/4-80

ABSOLUTE MAXIMUM RATINGS

Rating	Value	Unit
Temperature Under Bias	−10 to +80	°C
Operating Temperature Range	0 to +70	°C
Storage Temperature	−65 to −125	°C
All Input or Output Voltages with Respect to V_{SS}	+6 to −0.3	Vdc
V_{PP} Supply Voltage with Respect to V_{SS}	+28 to −0.3	Vdc

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields, however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

MODE SELECTION

Mode	Pin Number					
	9-11, 13-17 DQ	12 V_{SS}	18 E/Progr	20 G*	21 V_{PP}	24 V_{CC}
Read	Data Out	V_{SS}	V_{IL}	V_{IL}	V_{CC}*	V_{CC}
Output Disable	High Z	V_{SS}	Don't Care	V_{IH}	V_{CC}*	V_{CC}
Standby	High Z	V_{SS}	V_{IH}	Don't Care	V_{CC}*	V_{CC}
Program	Data In	V_{SS}	Pulsed V_{IL} to V_{IH}	V_{IH}	V_{IHP}	V_{CC}
Program Verify	Data Out	V_{SS}	V_{IL}	V_{IL}	V_{IHP}	V_{CC}
Program Inhibit	High Z	V_{SS}	V_{IL}	V_{IH}	V_{IHP}	V_{CC}

*In the Read Mode if $V_{PP} \geq V_{IH}$, then $\overline{G}$ (active low)
$V_{PP} \leq V_{IL}$, then G (active high)

BLOCK DIAGRAM

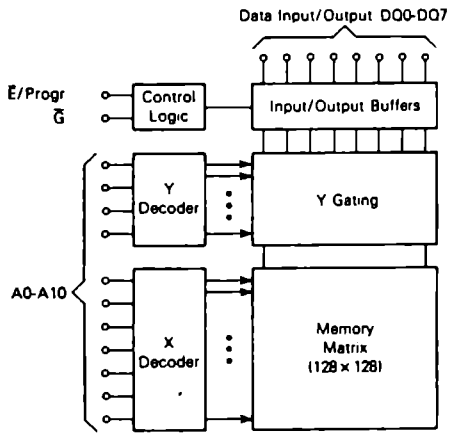
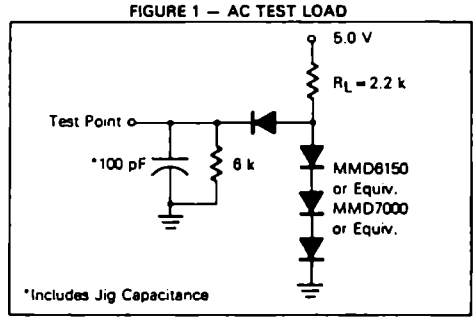


FIGURE 1 — AC TEST LOAD



CAPACITANCE (f = 1.0 MHz, T_A = 25°C, periodically sampled rather than 100% tested)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance (V_{in} = 0 V)	C_{in}	4.0	6.0	pF
Output Capacitance (V_{out} = 0 V)	C_{out}	8.0	12	pF

Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation $C = \frac{I\Delta t}{\Delta V}$

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted)

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Symbol	Min	Nom	Max	Unit
Supply Voltage* MCM27L16/MCM2716	V_{CC}	4.75	5.0	5.25	Vdc
MCM27L16-35/MCM27L16-25/MCM2716-35/MCM2716-25	V_{CC}	4.5	5.0	5.5	
	V_{PP}	V_{CC} – 0.6	5.0	V_{CC} + 0.6	
Input High Voltage	V_{IH}	2.0	–	V_{CC} + 1.0	Vdc
Input Low Voltage	V_{IL}	– 0.1	–	0.8	Vdc

RECOMMENDED DC OPERATING CHARACTERISTICS

Characteristic	Condition	Symbol	MCM2716			MCM27L16			Units
			Min	Typ	Max	Min	Typ	Max	
Address, $\overline{G}$ and $\overline{E}$/Progr Input Sink Current	V_{in} = 5.25 V	I_{in}	–	–	10	–	–	10	μA
Output Leakage Current	V_{out} = 5.25 V, $\overline{G}$ = 5.0 V	I_{LO}	–	–	10	–	–	10	μA
V_{CC} Supply Current (Standby) 2716/2716-35	$\overline{E}$/Progr = V_{IH}, $\overline{G}$ = V_{IL}	I_{CC1}	–	–	25	–	–	10	mA
V_{CC} Supply Current (Standby) 2716-25	$\overline{E}$/Progr = V_{IH}, $\overline{G}$/V_{IL}	I_{CC1}	–	–	25	–	–	15	mA
V_{CC} Supply Current (Active) 2716/2716-35 (Outputs Open)	$\overline{G}$ = $\overline{E}$/Progr = V_{IL}	I_{CC2}	–	–	100	–	–	60	mA
V_{CC} Supply Current (Active) 2716-25 (Outputs Open)	$\overline{G}$ = $\overline{E}$/Progr = V_{IL}	I_{CC2}	–	–	120	–	–	70	mA
V_{PP} Supply Current*	V_{PP} = 5.85 V	I_{PP1}	–	–	5.0	–	–	5.0	mA
Output Low Voltage	I_{OL} = 2.1 mA	V_{OL}	–	–	0.45	–	–	0.45	V
Output High Voltage	I_{OH} = – 400 μA	V_{OH}	2.4	–	–	2.4	–	–	V

*V_{CC} must be applied simultaneously or prior to V_{PP}. V_{CC} must also be switched off simultaneously with or after V_{PP}. With V_{PP} connected directly to V_{CC} during the read operation, the supply current would then be the sum of I_{PP1} and I_{CC}. The additional 0.6 V tolerance on V_{PP} makes it possible to use a driver circuit for switching the V_{PP} supply pin from V_{CC} in Read mode to ± 25 V for programming. Typical values are for T_A = 25°C and nominal supply voltages.

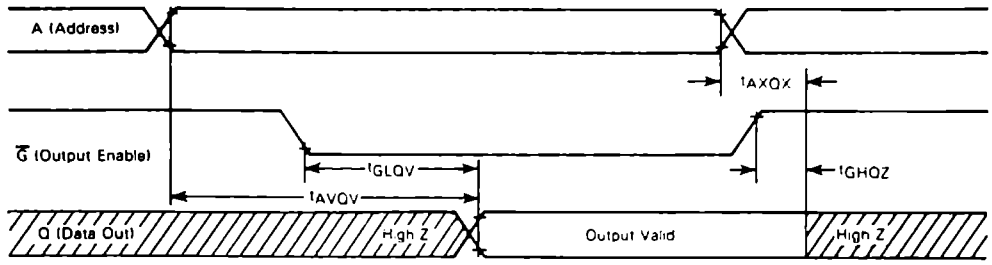
AC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted)

Input Pulse Levels ..... 0.8 Volt and 2.2 Volts
Input Rise and Fall Times ..... 20 ns
Input and Output Timing Levels ..... 2.0 and 0.8 Volts
Output Load ..... See Figure 1

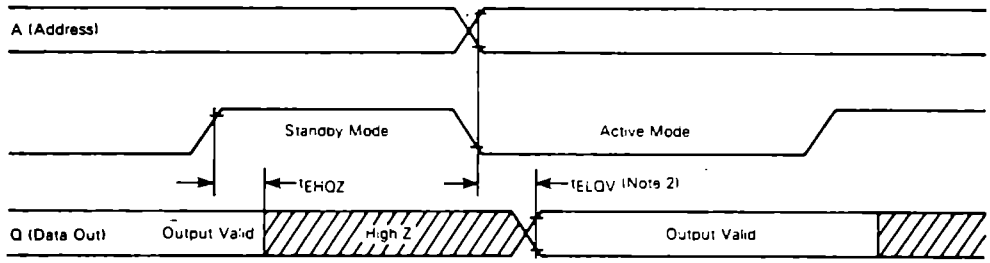
Characteristic	Condition	Symbol	MCM2716-25		MCM2716-35		MCM2716		Units
			Min	Max	Min	Max	Min	Max	
Address Valid to Output Valid	$\overline{E}$/Progr = G = V_{IL}	t_{AVQV}	–	250	–	350	–	450	ns
$\overline{E}$/Progr to Output Valid	(Note 2)	t_{ELQV}	–	250	–	350	–	450	
Output Enable to Output Valid	$\overline{E}$/Progr = V_{IL}	t_{GLQV}	–	150	–	150	–	150	
$\overline{E}$/Progr to Hi-Z Output	–	t_{EHQZ}	0	100	0	100	0	100	
Output Disable to Hi-Z Output	$\overline{E}$/Progr = V_{IL}	t_{GHQZ}	0	100	0	100	0	100	
Data Hold from Address	$\overline{E}$/Progr = G = V_{IL}	t_{AXDX}	0	–	0	–	0	–	

READ MODE TIMING DIAGRAMS ($\overline{E}$/Progr = V_{IL})



STANDBY MODE (Output Enable = V_{IL})

Standby Mode ($\overline{E}$/Progr = V_{IH})



NOTE 2 t_{ELQV} is referenced to $\overline{E}$/Progr or stable address, whichever occurs last

DC PROGRAMMING CONDITIONS AND CHARACTERISTICS

(T_A = 25°C ± 5°C)

RECOMMENDED PROGRAMMING OPERATING CONDITIONS

Parameter	Symbol	Min	Nom	Max	Unit
Supply Voltage	V_{CC} V_{PP}	4.75 24	5.0 25	5.25 26	Vdc
Input High Voltage for Data	V_{IH}	2.2	–	V_{CC} + 1	Vdc
Input Low Voltage for Data	V_{IL}	−0.1	–	0.8	Vdc

PROGRAMMING OPERATION DC CHARACTERISTICS

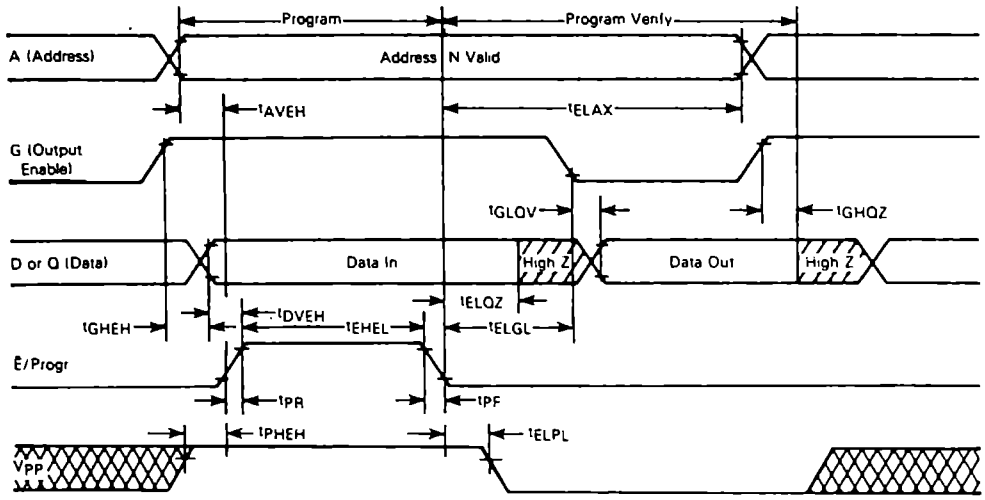
Characteristic	Condition	Symbol	Min	Typ	Max	Unit
Address, G and $\overline{E}$/Progr Input Sink Current	V_{in} = 5.25 V/0.45 V	I_{LI}	–	–	10	μAdc
V_{PP} Supply Current (V_{PP} = 25 V ± 1 V)	$\overline{E}$/Progr = V_{IL}	I_{PP1}	–	–	10	mAdc
V_{PP} Programming Pulse Supply Current (V_{PP} = 25 V ± 1 V)	$\overline{E}$/Progr = V_{IH}	I_{PP2}	–	–	30	mAdc
V_{CC} Supply Current (Outputs Open)	–	I_{CC}	–	–	160	mAdc

AC PROGRAMMING OPERATING CONDITIONS AND CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit
Address Setup Time	t_{AVEH}	2.0	–	μs
Output Enable High to Program Pulse	t_{GHEH}	2.0	–	μs
Data Setup Time	t_{DVEH}	2.0	–	μs
Address Hold Time	t_{ELAX}	2.0	–	μs
Output Enable Hold Time	t_{ELGL}	2.0	–	μs
Data Hold Time	t_{ELQZ}	2.0	–	μs
V_{PP} Setup Time	t_{PHEH}	0	–	ns
V_{PP} to Enable Low Time	t_{ELPL}	0	–	ns
Output Disable to High Z Output	t_{GHQZ}	0	150	ns
Output Enable to Valid Data ($\overline{E}$/Progr = V_{IL})	t_{GLQV}	–	150	ns
Program Pulse Width	t_{EHEL}	1*	55	ms
Program Pulse Rise Time	t_{PR}	5	–	ns
Program Pulse Fall Time	t_{PF}	5	–	ns

*If shorter than 45 ms (min) pulses are used, the same number of pulses should be applied after the specific data has been verified

PROGRAMMING OPERATION TIMING DIAGRAM



PROGRAMMING INSTRUCTIONS

After the completion of an ERASE operation, every bit in the device is in the "1" state (represented by Output High). Data are entered by programming zeros (Output Low) into the required bits. The words are addressed the same way as in the READ operation. A programmed "0" can only be changed to a "1" by ultraviolet light erasure.

To set the memory up for Program Mode, the V_{PP} input (Pin 21) should be raised to +25 V. The V_{CC} supply voltage is the same as for the Read operation and G is at V_{IH}. Programming data is entered in 8-bit words through the data out (DQ) terminals. Only "0's" will be programmed when "0's" and "1's" are entered in the 8-bit data word.

After address and data setup, a program pulse (V_{IL} to V_{IH}) is applied to the $\overline{E}$/Progr input. A program pulse is applied to each address location to be programmed. To minimize programming time, a 2 ms pulse width is recommended. The maximum program pulse width is 55 ms, therefore, programming must not be attempted with a dc signal applied to the $\overline{E}$/Progr input.

Multiple MCM2716s may be programmed in parallel by connecting together like inputs and applying the program pulse to the $\overline{E}$/Progr inputs. Different data may be programmed into multiple MCM2716s connected in parallel by using the PROGRAM INHIBIT mode. Except for the $\overline{E}$/Progr pin, all like inputs (including Output Enable) may be common.

The PROGRAM VERIFY mode with V_{PP} at 25 V is used to determine that all programmed bits were correctly programmed.

READ OPERATION

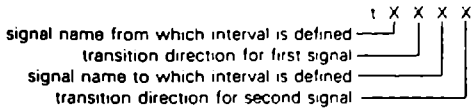
After access time, data is valid at the outputs in the READ mode. With stable system addresses, effectively faster access time can be obtained by gating the data onto the bus with Output Enable.

The Standby mode is available to reduce active power dissipation. The outputs are in the high impedance state when the $\overline{E}$/Progr input pin is high (V_{IH}) independent of the Output Enable input.

ERASING INSTRUCTIONS

The MCM2716/27L16 can be erased by exposure to high intensity shortwave ultraviolet light, with a wavelength of 2537 angstroms. The recommended integrated dose (i.e., UV-intensity X exposure time) is 15 Ws/cm^2. As an example, using the "Model 30-000" UV-Eraser (Turner Designs, Mountain View, CA 94043) the ERASE-time is 36 minutes. The lamps should be used without shortwave filters and the MCM2716/MCM27L16 should be positioned about one inch away from the UV-tubes.

TIMING PARAMETER ABBREVIATIONS


t X X X X
signal name from which interval is defined
transition direction for first signal
signal name to which interval is defined
transition direction for second signal

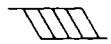
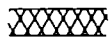
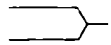
The transition definitions used in this data sheet are:

- H = transition to high
- L = transition to low
- V = transition to valid
- X = transition to invalid or don't care
- Z = transition to off (high impedance)

TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

WAVEFORMS

Waveform Symbol	Input	Output
	Must Be Valid	Will Be Valid
	Change From H to L	Will Change From H to L
	Change From L to H	Will Change From L to H
	Don't Care Any Change Permitted	Changing State Unknown
		High Impedance

MOTOROLA

TMS2716
TMS27A16

MOS

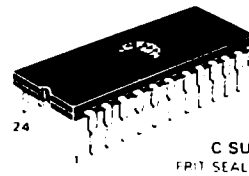
(N-CHANNEL, SILICON-GATE)

2048 × 8-BIT
UV ERASABLE PROM

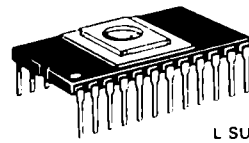
2048 × 8 ERASABLE PROM

The TMS2716 and TMS27A16 are 16,384-bit Erasable and Electrically Reprogrammable PROMs designed for system debug usage and similar applications requiring nonvolatile memory that could be reprogrammed periodically. The transparent window on the package allows the memory content to be erased with ultraviolet light. The TMS2716 is pin compatible with 2708 EPROMs, allowing easy memory size doubling.

- Organized as 2048 Bytes of 8 Bits
- Fully Static Operation (No Clocks, No Refresh)
- Standard Power Supplies of +12 V, +5 V, and −5 V
- Maximum Access Time = 300 ns – TMS27A16
  450 ns – TMS2716
- Chip-Select Input for Memory Expansion
- TTL Compatible – No Pull-up Resistors Required
- Three-State Outputs for OR-Tie Capability
- The TMS2716 is Pin Compatible to MCM2708 and MCM68708 EPROMs

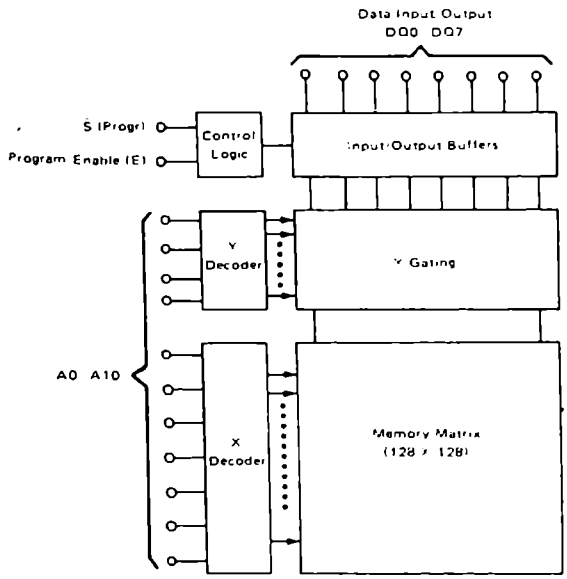


C SUFFIX
FRIT SEAL PACKAGE
CASE 623A-02

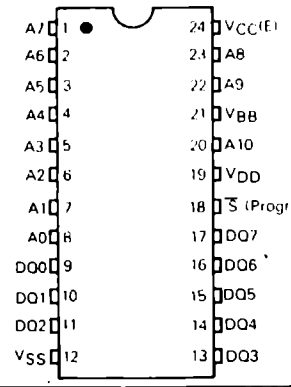


L SUFFIX
CERAMIC PACKAGE
CASE 715-07

BLOCK DIAGRAM



PIN ASSIGNMENT



PIN NAMES	
A0 A10	Address Inputs
DQ0 DQ7	Data Input (Program) or Output (Read)
(E)	Program Enable
$\overline{S}$	Chip Select
(Progr)	Program Pulse
V_{BB}	−5 V Power Supply
V_{CC}	+5 V Power Supply
V_{DD}	+12 V Power Supply
V_{SS}	Ground

DS9518 R1/1-79

ABSOLUTE MAXIMUM RATINGS (1)

Rating	Value	Unit
Operating Temperature	0 to +70	°C
Storage Temperature	−65 to +125	°C
V_{DD} with Respect to V_{BB}	+20 to −0.3	V
V_{CC} and V_{SS} with Respect to V_{BB}	+15 to −0.3	V
All Input or Output Voltage with Respect to V_{BB} During Read	+15 to −0.3	V
(E) Input with Respect to V_{BB} During Programming	+20 to −0.3	V
Program Input with Respect to V_{BB}	+35 to −0.3	V
Power Dissipation	1.8	Watts

NOTE 1: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

PIN CONNECTION DURING READ OR PROGRAM

	Pin Number		
Mode	9–11, 13–17	18	24
Read	D_{out}	V_{IL} or V_{IH}	V_{CC}
Program	D_{in}	Pulsed V_{IHP}	V_{IHW}

DC READ OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted)

RECOMMENDED DC READ OPERATING CONDITIONS

Parameter		Symbol	Min	Nom	Max	Unit
Supply Voltage	TMS2716	V_{CC}	4.75	5.0	5.25	V
		V_{DD}	11.4	12	12.6	V
		V_{BB}	−5.25	−5.0	−4.75	V
	TMS27A16	V_{CC}	4.5	5.0	5.5	V
		V_{DD}	10.8	12	13.2	V
		V_{BB}	−5.5	−5.0	−4.5	V
Input High Voltage		V_{IH}	2.2	–	V_{CC} + 1.0	V
Input Low Voltage		V_{IL}	V_{SS}	–	0.65	V

READ OPERATING DC CHARACTERISTICS

Characteristic	Condition	Symbol	Min	Typ	Max	Unit
Address Input Sink Current	V_{in} = V_{CC}max or V_{in} = V_{IL}	I_{in}	–	1	10	μA
Output Leakage Current	V_{out} = V_{CC}max and S = 5 V	I_{LO}	–	1	10	μA
V_{DD} Supply Current	Worst Case Supply Currents All Inputs High (E) 5.0 V, T_A = 0°C	I_{DD}			65	mA
V_{CC} Supply Current		I_{CC}	–	–	12	mA
V_{BB} Supply Current		I_{BB}	–	–	45	mA
Output Low Voltage	I_{OL} = 1.6 mA	V_{OL}	–	–	0.45	V
Output High Voltage	I_{OH} = −100 μA	V_{OH1}	3.7	–	–	V
Output High Voltage	I_{OH} = −1.0 mA	V_{OH2}	2.4	–	–	V

V_{BB} must be applied prior to V_{CC} and V_{DD}. V_{BB} must also be the last power supply switched off.

CAPACITANCE (periodically sampled rather than 100% tested)

Characteristic	Condition	Symbol	Typ	Max	Unit
Input Capacitance (f = 1.0 MHz)	V_{in} = 0 V, T_A = 25°C	C_{in}	4.0	6.0	pF
Output Capacitance (f = 1.0 MHz)	V_{out} = 0 V, T_A = 25°C	C_{out}	8.0	12	pF

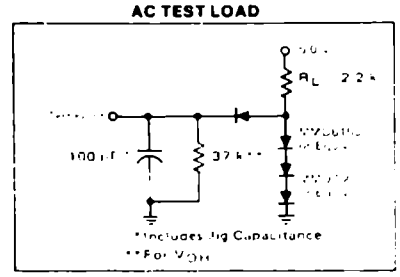
AC READ OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted)
(All timing with t_r = t_f = 20 ns, Load per Note 2)

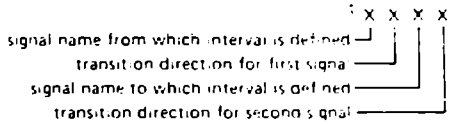
Characteristic	Symbol	TMS2716		TMS27A16		Unit
		Min	Max	Min	Max	
Address to Output Delay	t_{AVQV}		450		300	ns
Chip Select to Output Delay	t_{SLQV}		120		120	ns
Data Hold from Address	t_{AXQZ}	10		10		ns
Data Hold from Deselection	t_{SHQZ}	10	120	10	120	ns

NOTE 2 Output Load = 1 TTL Gate and C_L = 100 pF (Includes Jig Capacitance)
Timing Measurement Reference Levels Inputs 0.8 V and 2.8 V
Outputs 0.8 V and 2.4 V

AC TEST LOAD



TIMING PARAMETER ABBREVIATIONS

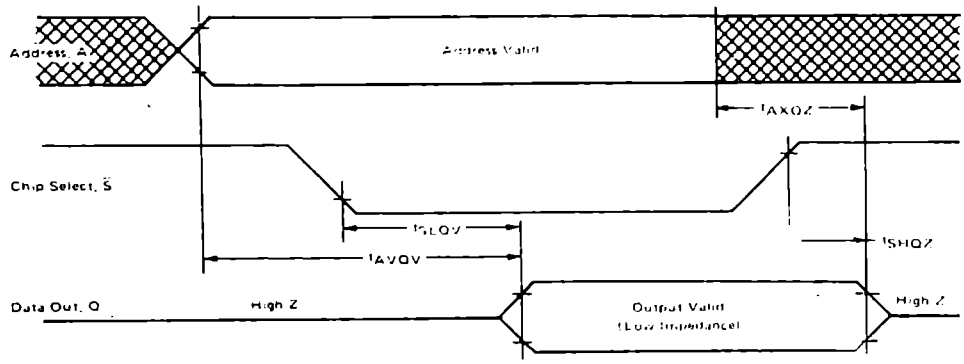

T X X X X
signal name from which interval is defined
transition direction for first signal
signal name to which interval is defined
transition direction for second signal

The transition definitions used in this data sheet are
- H = transition to high
- L = transition to low
- V = transition to valid
- X = transition to invalid or don't care
- Z = transition to off (high impedance)

TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

READ OPERATION TIMING DIAGRAM



DC PROGRAMMING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted)

RECOMMENDED PROGRAMMING OPERATING CONDITIONS

Parameter	Symbol	Min	Nom	Max	Unit
Supply Voltage – TMS2716 and TMS27A16	V_{CC}	4.75	5.0	5.25	Vdc
	V_{DD}	11.4	12	12.6	Vdc
	V_{BB}	-5.25	-5.0	-4.75	Vdc
Input High Voltage for Data	V_{IHD}	3.8	–	V_{CC} + 1	Vdc
Input Low Voltage for Data	V_{ILD}	V_{SS}	–	0.65	Vdc
Input High Voltage for Addresses	V_{IHA}	3.8	–	V_{CC} + 1	Vdc
Input Low Voltage for Addresses	V_{ILA}	V_{SS}	–	0.4	Vdc
Program Enable (E) Input High Voltage (Note 3)	V_{IHW}	11.4	12	12.6	Vdc
Program Enable (E) Input Low Voltage (Note 3)	V_{ILW}	4.75	5.0	5.25	Vdc
Program Pulse Input High Voltage (Note 3)	V_{IHP}	25	–	27	Vdc
Program Pulse Input Low Voltage (Note 4)	V_{ILP}	V_{SS}	–	1.0	Vdc

NOTE 3: Referenced to V_{SS}.
NOTE 4: $V_{IHP} - V_{ILP} = 25$ V min

PROGRAMMING OPERATION DC CHARACTERISTICS

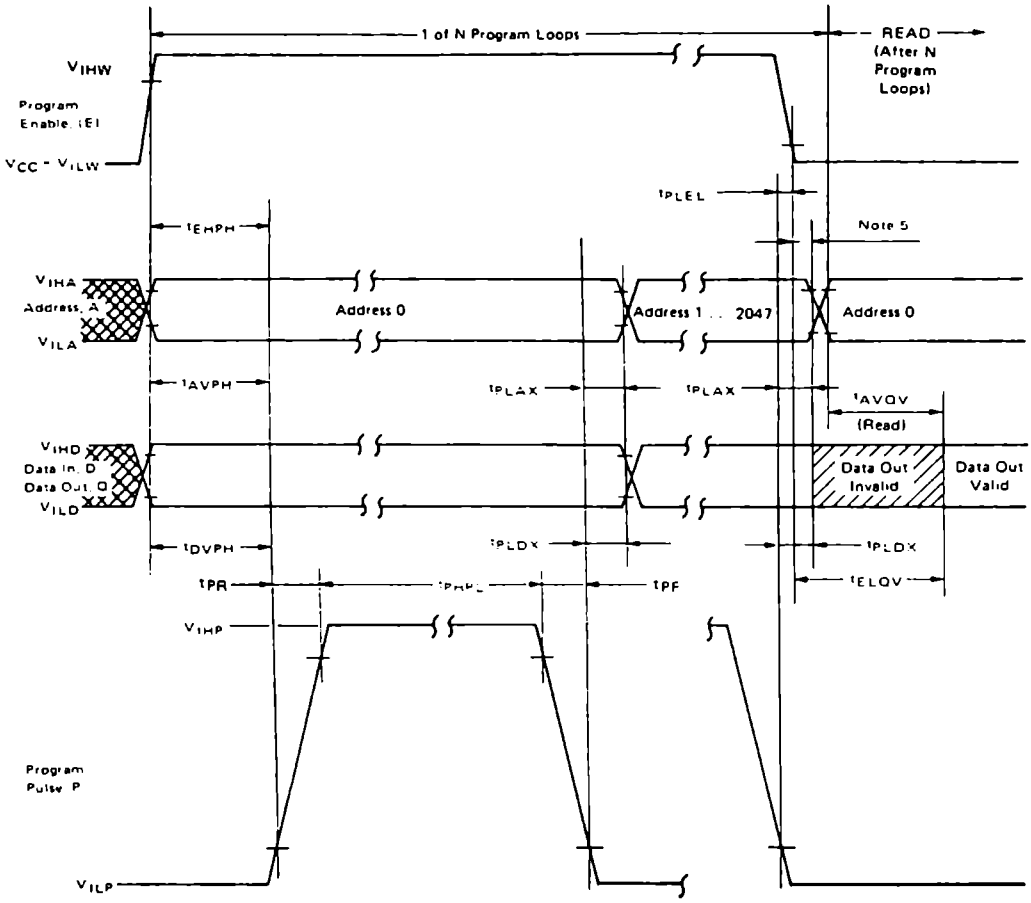
Characteristic	Condition	Symbol	Min	Typ	Max	Unit
Address Input Sink Current	$V_{in} = 5.25$ V	I_{LI}	–	–	10	μAdc
Program Pulse Source Current		I_{IPL}	–	–	3.0	mAdc
Program Pulse Sink Current		I_{IPH}	–	–	20	mAdc
V_{DD} Supply Current	Worst-Case Supply Currents All Inputs High (E) = 5 V, $T_A = 0°C$	I_{DD}	–	–	65	mAdc
V_{CC} Supply Current		I_{CC}	–	–	15	mAdc
V_{BB} Supply current		I_{BB}	–	–	45	mAdc

AC PROGRAMMING OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
Address Setup Time	t_{AVPH}	10	–	μs
(E) Setup Time	t_{EHPH}	10	–	μs
Data Setup Time	t_{DVPH}	10	–	μs
Address Hold Time	t_{PLAX}	1.0	–	μs
(E) Hold Time	t_{PLEL}	0.5	–	μs
Data Hold Time	t_{PLDX}	1.0	–	μs
Program to Read Delay	t_{ELQV}	–	10	μs
Program Pulse Width	t_{PHPL}	0.1	1.0	ms
Program Pulse Rise Time	t_{PR}	0.5	2.0	μs
Program Pulse Fall Time	t_{PF}	0.5	2.0	μs

PROGRAMMING OPERATION TIMING DIAGRAM



NOTE 5: This Program Enable transition must occur after the Program Pulse transition and before the Address Transition.

WAVEFORM DEFINITIONS

Waveform Symbol	Input	Output
———	MUST BE VALID	WILL BE VALID
——— / ———	CHANGE FROM H TO L	WILL CHANGE FROM H TO L
——— / ———	CHANGE FROM L TO H	WILL CHANGE FROM L TO H

Waveform Symbol	Input	Output
//////	DON'T CARE Any CHANGE PERMITTED	CHANGING STATE UNKNOWN
><><		HIGH IMPEDANCE

PROGRAMMING INSTRUCTIONS

After the completion of an ERASE operation, every bit in the device is in the "1" state (represented by Output High). Data are entered by programming zeros (Output Low) into the required bits. The words are addressed the same way as in the READ operation. A programmed "0" can only be changed to a "1" by ultraviolet light erasure.

To set the memory up for programming mode, the V_{CC}(E) input (Pin 24) should be raised to +12 V. Programming data is entered in 8-bit words through the data output terminals (DQ0 to DQ7).

The V_{DD} and V_{BB} supply voltages are the same as for the READ operation.

After address and data setup, one program pulse per address is applied to the program input. A program loop is a full pass through all addresses. Total programming time/address, $T_{Ptotal} = N \times t_{PHPL} \geq 100$ ms. The required number of program loops (N) is a function of the program pulse width (t_{PHPL}) where: $0.1 \text{ ms} \leq t_{PHPL} \leq 1.0 \text{ ms}$, correspondingly, N is $100 \leq N \leq 1000$. There must be N successive loops through all 2048 addresses. It is not permitted to apply more than one program pulse in succession to the same address (i.e., N program pulses to an address and then change to the next address to be programmed). At the end of a program sequence the Program Enable (E) falling edge transition must occur before the first address transition, when changing from a PROGRAM to a READ cycle. The program pin should be pulled down to V_{ILP} with an active device, because this pin sources a small amount of current (I_{IPL}) when (E) is at V_{IHW} (12 V) and the program pulse is at V_{ILP}.

EXAMPLE FOR PROGRAMMING

Always use the $T_{Ptotal} = N \times t_{PHPL} \geq 100$ ms relationship.

1. All 16,384 bits should be programmed with a 0.2 ms program pulse width.

The minimum number of program loops:

$$N = \frac{T_{Ptotal}}{t_{PHPL}} = \frac{100 \text{ ms}}{0.2 \text{ ms}} = 500.$$

One program loop consists of words 0 to 2047.

2. Words 0 to 200 and 300 to 700 are to be programmed. All other bits are "don't care". The program pulse width is 0.5 ms. The minimum number of program loops, $N = 100/0.5 = 200$. One program loop consists of words 0 to 2047. The data entered into the "don't care" bits should be all 1s.

3. Same requirements as example 2, but the EPROM is now to be updated to include data for words 850 to 880. The minimum number of program loops is the same as in the previous example, $N = 200$. One program loop consists of words 0 to 2047. The data entered into the "don't care" bits should be all 1s. Addresses 0 to 200 and 300 to 700 must be reprogrammed with their original data pattern.

ERASING INSTRUCTIONS

The TMS2716/27A16 can be erased by exposure to high intensity shortwave ultraviolet light, with a wavelength of 2537 Å. The recommended integrated dose (i.e., UV-intensity × exposure time) is 12.5 Ws/cm^2. As an example, using the "Model 30-000" UV-Eraser (Turner Designs, Mountain View, CA 94043) the ERASE time is 30 minutes. The lamps should be used without shortwave filters and the TMS2716/27A16 should be positioned about one inch away from the UV-tubes.

MOTOROLA

MCM68708
MCM68A708

MOS

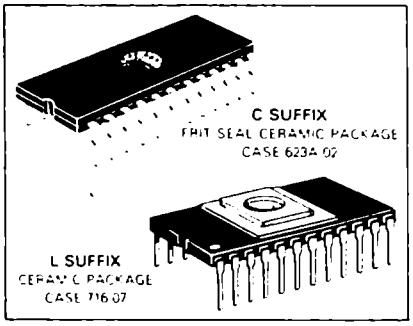
(N CHANNEL, SILICON-GATE)

1024 X 8-BIT
UV ERASABLE PROM

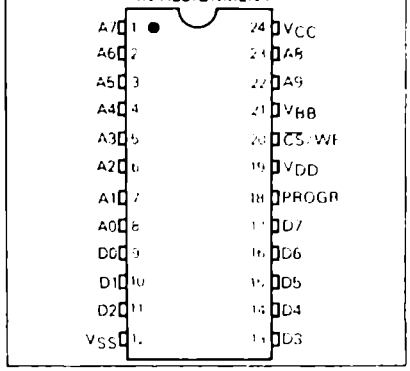
1024 X 8 ERASABLE PROM

The MCM68708/68A708 is a 8192-bit Erasable and Electrically Reprogrammable PROM designed for system debug usage and similar applications requiring nonvolatile memory that could be reprogrammed periodically. The transparent window on the package allows the memory content to be erased with ultraviolet light. Pin-for-pin mask-programmable ROMs are available for large volume production runs of systems initially using the MCM68708 68A708.

- Organized as 1024 Bytes of 8 Bits
- Fully Static Operation
- Standard Power Supplies of +12 V, +5 V and -5 V
- Maximum Access Time = 300 ns – MCM68A708
  450 ns – MCM68708
- Low Power Dissipation
- Chip-Select Input for Memory Expansion
- TTL Compatible
- Three-State Outputs
- Pin Equivalent to the 2708
- Pin-for-Pin Compatible to MCM65308, MCM68308 or 2308 Mask-Programmable ROMs
- Bus Compatible to the M6800 Family



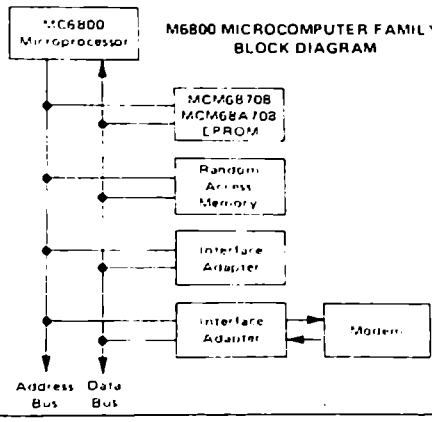
PIN ASSIGNMENT



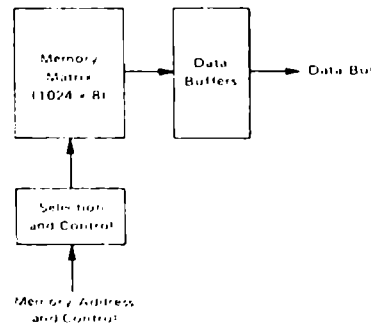
PIN CONNECTION DURING READ OR PROGRAM

Mode	Pin Number						
	9-11, 13-17	12	18	19	20	21	24
Read	D_{out}	V_{SS}	V_{SS}	V_{DD}	V_{IL}	V_{BB}	V_{CC}
Program	D_{in}	V_{SS}	Pulsed V_{IHP}	V_{DD}	$V_{IH/W}$	V_{BB}	V_{CC}

M6800 MICROCOMPUTER FAMILY
BLOCK DIAGRAM

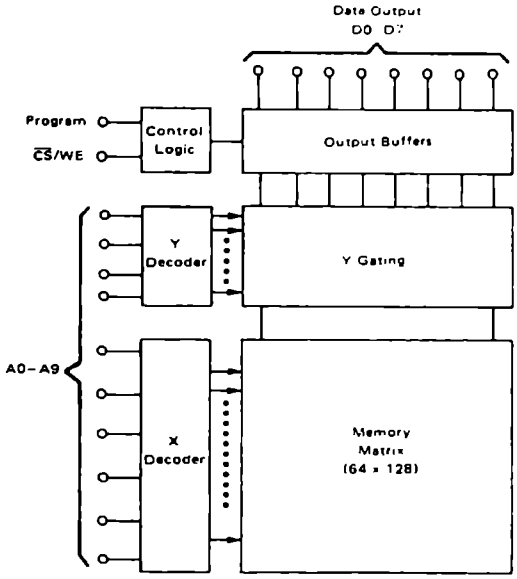


MCM68708/68A708 READ ONLY
MEMORY BLOCK DIAGRAM



DS9439 R1/1 /9

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1]

Rating	Value	Unit
Operating Temperature	0 to +70	°C
Storage Temperature	-65 to +125	°C
V_{DD} with Respect to V_{BB}	+20 to -0.3	Vdc
V_{CC} and V_{SS} with Respect to V_{BB}	+15 to -0.3	Vdc
All Input or Output Voltages with Respect to V_{BB} during Read	+15 to -0.3	Vdc
$\overline{CS}$/WE Input with Respect to V_{BB} during Programming	+20 to -0.3	Vdc
Program Input with Respect to V_{BB}	+35 to -0.3	Vdc
Power Dissipation	1.8	Watts

Note 1:
Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

DC READ OPERATING CONDITIONS AND CHARACTERISTICS
(Full operating voltage and temperature range unless otherwise noted.)

RECOMMENDED DC READ OPERATING CONDITIONS

Parameter	Symbol	Min	Nom	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	Vdc
	V_{DD}	11.4	12	12.6	Vdc
	V_{BB}	-5.25	-5.0	-4.75	Vdc
Input High Voltage	V_{IH}	V_{SS} +2.0	–	V_{CC}	Vdc
Input Low Voltage	V_{IL}	V_{SS} -0.3	–	V_{SS} +0.8	Vdc

READ OPERATION DC CHARACTERISTICS

Characteristic		Condition	Symbol	Min	Typ	Max	Unit
Address and CS Input Sink Current		V_{in} = 5.25 V or V_{in} = V_{IL}	I_{in}	–	1	10	μA
Output Leakage Current		V_{out} = 5.25 V, $\overline{CS}$/WE = 5 V	I_{LO}	–	1	10	μA
V_{DD} Supply Current	(Note 2)	Worst-Case Supply Currents	I_{DD}		50	65	mA
V_{CC} Supply Current		All Inputs High	I_{CC}	–	6	10	mA
V_{BB} Supply Current		$\overline{CS}$/WE = 5.0 V, T_A = 0°C	I_{BB}	–	30	45	mA
Output Low Voltage		I_{OL} = 1.6 mA	V_{OL}	–	–	V_{SS} +0.4	V
Output High Voltage		I_{OH} = -100 μA	V_{OH}	V_{SS} +2.4	–	–	V
Power Dissipation	(Note 2)	T_A = 70°C	P_D	–	–	800	mW

Note 2:
The total power dissipation is specified at 800 mW. It is not calculable by summing the various currents (I_{DD}, I_{CC}, and I_{BB}) multiplied by their respective voltages, since current paths exist between the various power supplies and V_{SS}. The I_{DD}, I_{CC}, and I_{BB} currents should be used to determine power supply capacity only.

V_{BB} must be applied prior to V_{CC} and V_{DD}. V_{BB} must also be the last power supply switched off.

AC READ OPERATING CONDITIONS AND CHARACTERISTICS
(Full operating voltage and temperature range unless otherwise noted.)
(All timing with $t_r = t_f = 20$ ns, Load per Note 3)

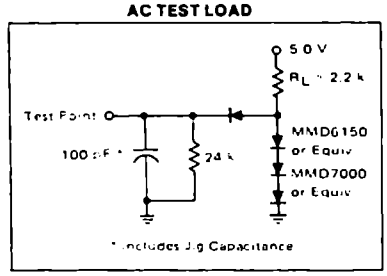
Characteristic	Symbol	MCM68A708			MCM68708			Unit
		Min	Typ	Max	Min	Typ	Max	
Address to Output Delay	t_{AO}	–	220	300	–	280	450	ns
Chip Select to Output Delay	t_{CO}	–	60	120	–	60	120	ns
Data Hold from Address	t_{DHA}	10	–	–	10	–	–	ns
Data Hold from Deselection	t_{DHD}	10	–	120	10	–	120	ns

CAPACITANCE (periodically sampled rather than 100% tested.)

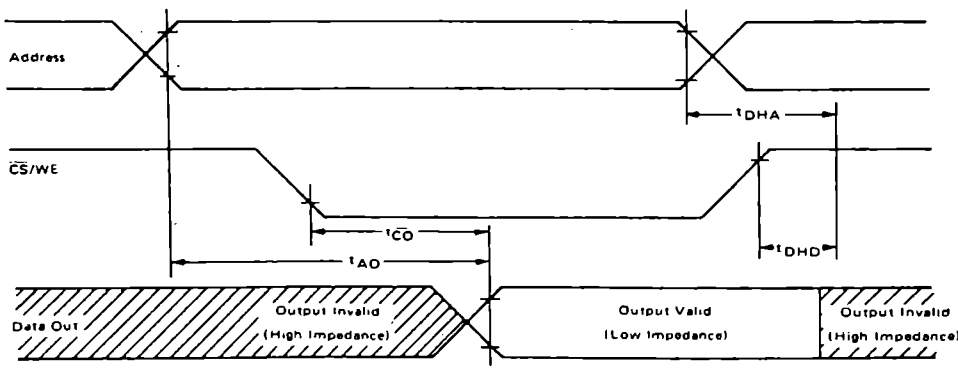
Characteristic	Condition	Symbol	Typ	Max	Unit
Input Capacitance (f = 1.0 MHz)	V_{in} = 0 V, T_A = 25°C	C_{in}	4.0	6.0	pF
Output Capacitance (f = 1.0 MHz)	V_{out} = 0 V, T_A = 25°C	C_{out}	8.0	12	pF

Note 3:
Output Load = 1 TTL Gate and C_L = 100 pF (Includes Jig Capacitance)
Timing Measurement Reference Levels — Inputs 0.8 V and 2.8 V
Outputs 0.8 V and 2.4 V

AC TEST LOAD



READ OPERATION TIMING DIAGRAM



DC PROGRAMMING CONDITIONS AND CHARACTERISTICS
(Full operating voltage and temperature range unless otherwise noted.)

RECOMMENDED PROGRAMMING OPERATING CONDITIONS

Parameter	Symbol	Min	Nom	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	Vdc
	V_{DD}	11.4	12	12.6	Vdc
	V_{BB}	-5.25	-5.0	-4.75	Vdc
Input High Voltage for All Addresses and Data	V_{IH}	3.0	–	V_{CC} + 1.0	Vdc
Input Low Voltage (except Program)	V_{IL}	V_{SS}	–	0.65	Vdc
$\overline{CS}$/WE Input High Voltage (Note 4)	V_{IHW}	11.4	12	12.6	Vdc
Program Pulse Input High Voltage (Note 4)	V_{IHP}	25	–	27	Vdc
Program Pulse Input Low Voltage (Note 5)	V_{ILP}	V_{SS}	–	1.0	Vdc

Note 4: Referenced to V_{SS}.
Note 5: $V_{IHP} - V_{ILP}$ = 25 V min.

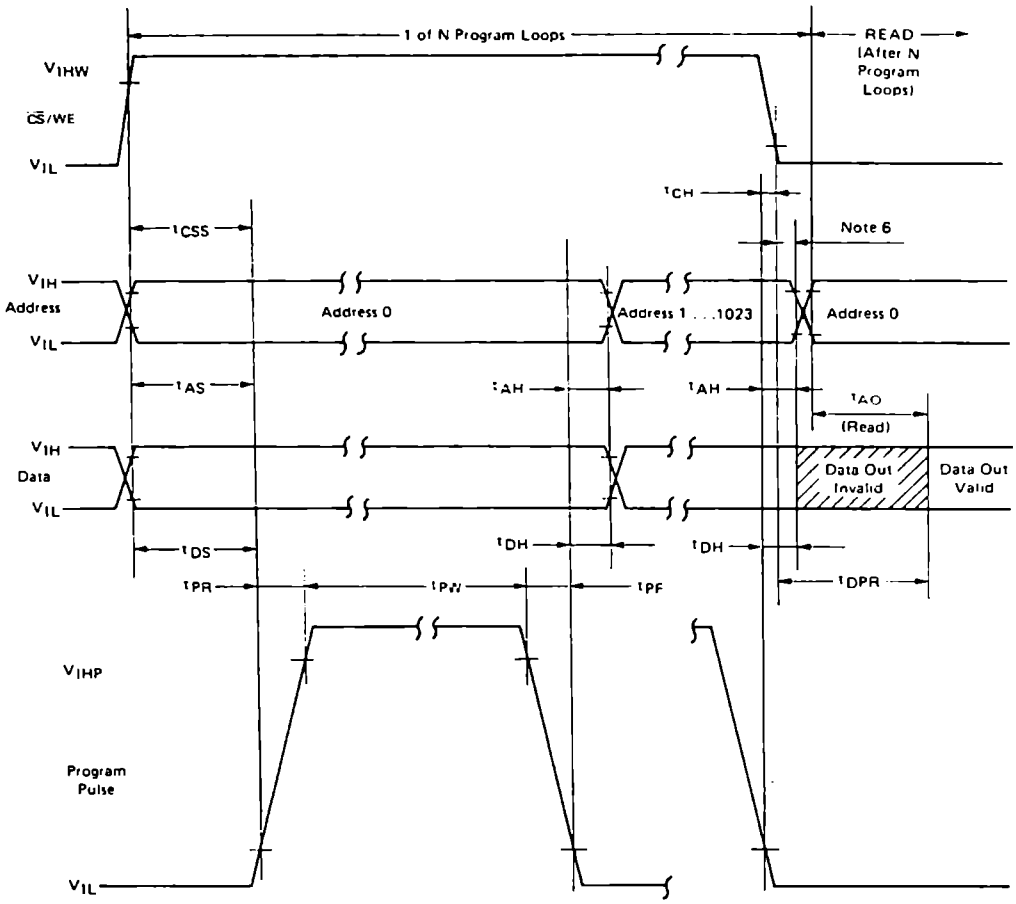
PROGRAMMING OPERATION DC CHARACTERISTICS

Characteristic	Condition	Symbol	Min	Typ	Max	Unit
Address and $\overline{CS}$/WE Input Sink Current	V_{in} = 5.25 V	I_{LI}	–	–	10	μAdc
Program Pulse Source Current		I_{IPL}	–	–	3.0	mAdc
Program Pulse Sink Current		I_{IPH}	–	–	20	mAdc
V_{DD} Supply Current	Worst-Case Supply Currents	I_{DD}	–	50	65	mAdc
V_{CC} Supply Current	All Inputs High	I_{CC}	–	6	10	mAdc
V_{BB} Supply current	$\overline{CS}$/WE = 5 V, T_A = 0°C	I_{BB}	–	30	45	mAdc

AC PROGRAMMING OPERATING CONDITIONS AND CHARACTERISTICS
(Full operating voltage and temperature unless otherwise noted.)

Characteristic	Symbol	Min	Max	Unit
Address Setup Time	t_{AS}	10	–	μs
$\overline{CS}$/WE Setup Time	t_{CSS}	10	–	μs
Data Setup Time	t_{DS}	10	–	μs
Address Hold Time	t_{AH}	1.0	–	μs
$\overline{CS}$/WE Hold Time	t_{CH}	0.5	–	μs
Data Hold Time	t_{DH}	1.0	–	μs
Chip Deselect to Ouptut Float Delay	t_{DF}	0	120	ns
Program to Read Delay	t_{DPR}	–	10	μs
Program Pulse Width	t_{PW}	0.1	1.0	ms
Program Pulse Rise Time	t_{PR}	0.5	2.0	μs
Program Pulse Fall Time	t_{PF}	0.5	2.0	μs

PROGRAMMING OPERATION TIMING DIAGRAM



Note 6: The $\overline{CS}$/WE transition must occur after the Program Pulse transition and before the Address Transition

PROGRAMMING INSTRUCTIONS

After the completion of an ERASE operation, every bit in the device is in the "1" state (represented by Output High). Data are entered by programming zeros (Output Low) into the required bits. The words are addressed the same way as in the READ operation. A programmed "0" can only be changed to a "1" by ultraviolet light erasure.

To set the memory up for programming mode, the $\overline{CS}$/WE input (Pin 20) should be raised to +12 V. Programming data is entered in 8-bit words through the data output terminals (D0 to D7).

Logic levels for the data lines and addresses and the supply voltages (V_{CC}, V_{DD}, V_{BB}) are the same as for the READ operation.

After address and data setup one program pulse per address is applied to the program input (Pin 18). A program loop is a full pass through all addresses. Total programming time, $T_{Ptotal} = N \times t_{PW} \geq 100$ ms. The required number of program loops (N) is a function of the program pulse width (t_{PW}), where: $0.1 \text{ ms} \leq t_{PW} \leq 1.0$ ms; correspondingly N is: $100 \leq N \leq 1000$. There must be N successive loops through all 1024 addresses. It is not permitted to apply more than one program pulse in succession to the same address (i.e., N program pulses to an address and then change to the next address to be programmed). At the end of a program sequence the $\overline{CS}$/WE falling edge transition must occur before the first address transition, when changing from a PROGRAM to a READ cycle. The program pin (Pin 18) should be pulled down to V_{ILP} with an active device, because this pin sources a small amount of current (I_{IPL}) when $\overline{CS}$/WE is at V_{IHW} (12 V) and the program pulse is at V_{ILP}.

EXAMPLES FOR PROGRAMMING

Always use the $T_{Ptotal} = N \times t_{PW} \geq 100$ ms relationship.

1. All 8092 bits should be programmed with a 0.2 ms program pulse width.

   The minimum number of program loops:

   $$N = \frac{T_{Ptotal}}{t_{PW}} = \frac{100 \text{ ms}}{0.2 \text{ ms}} = 500$$ One program loop consists of words 0 to 1023.

2. Words 0 to 200 and 300 to 700 are to be programmed. All other bits are "don't care". The program pulse width is 0.5 ms. The minimum number of program loops, $N = \frac{100}{0.5} = 200$ One program loop consists of words 0 to 1023. The data entered into the "don't care" bits should be all 1s.

3. Same requirements as example 2, but the EPROM is now to be updated to include data for words 850 to 880. The minimum number of program loops is the same as in the previous example, N = 200. One program loop consists of words 0 to 1023. The data entered into the "don't care" bits should be all 1s. Addresses 0 to 200 and 300 to 700 must be reprogrammed with their original data pattern.

ERASING INSTRUCTIONS

The MCM68708/68A708 can be erased by exposure to high intensity shortwave ultraviolet light, with a wavelength of 2537 Å. The recommended integrated dose (i.e., UV intensity x exposure time) is 12.5 Ws/cm^2. As an example, using the "Model 30-000" UV Eraser (Turner Designs, Mountain View, CA 94043) the ERASE-time is 30 minutes. The lamps should be used without shortwave filters and the MCM68708/68A708 should be positioned about one inch away from the UV-tubes.

MOTOROLA

MCM68732
MCM68L732

4096 × 8-BIT UV ERASABLE PROM

The MCM68732/68L732 is a 32,768-bit Erasable and Electrically Reprogrammable PROM designed for system debug usage and similar applications requiring nonvolatile memory that could be reprogrammed periodically, or for replacing 32K ROMs for fast turnaround time. The transparent window on the package allows the memory content to be erased with ultraviolet light.

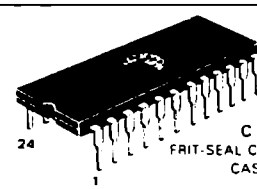
For ease of use, the device operates from a single power supply and has a static power-down mode. Pin-for-pin compatible mask programmable ROMs are available for large volume production runs of systems initially using the MCM68732/68L732.

- Single +5 V Power Supply
- Automatic Power-down Mode (Standby) with Chip Enable
- Organized as 4096 Bytes of 8 Bits
- Low Power Dissipation
- Fully TTL Compatible
- Maximum Access Time = 450 ns MCM68732
  350 ns MCM68732-35
- Standard 24-Pin DIP for EPROM Upgradability
- Pin Compatible to MCM68A332 Mask Programmable ROM
- AR Selects the Operational 32K Portion of the Die
  MCM68732-1 AR = 1 = HIGH
  MCM68732-0 AR = 0 = LOW
- Pin Compatible With the MCM2532 32K EPROM in the Read Mode
- Low Power Version
  MCM68L732 Active 60 mA Maximum
  Standby 15 mA Maximum
  MCM68L732-35 Active 100 mA Maximum
  Standby 25 mA Maximum

MOS

(N-CHANNEL, SILICON GATE)

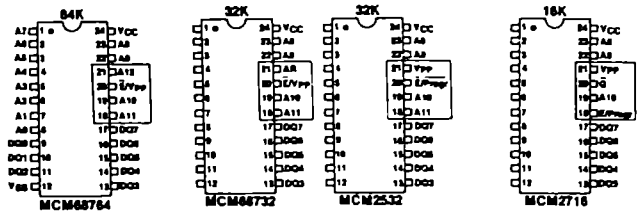
4096 × 8-BIT
UV ERASABLE PROGRAMMABLE
READ ONLY MEMORY



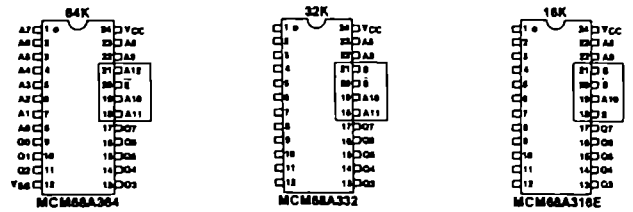
C SUFFIX
FRIT-SEAL CERAMIC PACKAGE
CASE 623A-02

L SUFFIX SIDEBRAZE CERAMIC PACKAGE
ALSO AVAILABLE — CASE 716

MOTOROLA'S PIN-COMPATIBLE EPROM FAMILY

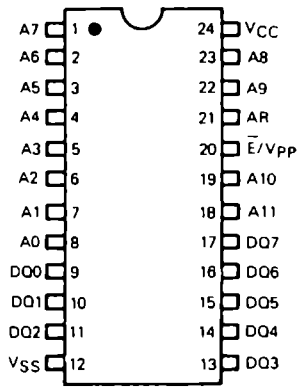


MOTOROLA'S PIN-COMPATIBLE ROM FAMILY



INDUSTRY STANDARD PINOUTS

PIN ASSIGNMENT



*Pin Names	
A	Address
AR	Address Reference
DQ	Data Input/Output
Ē/Vpp	Chip Enable/Program

*New industry standard nomenclature

DS9814 R1/10-80

ABSOLUTE MAXIMUM RATINGS (1)

Rating	Value	Unit
Temperature Under Bias	− 10 to + 80	°C
Operating Temperature Range	0 to + 70	°C
Storage Temperature	− 65 to + 125	°C
All Input or Output Voltages with Respect to V_{SS}	+ 6 to − 0.3	Vdc
V_{PP} Supply Voltage with Respect to V_{SS}	+ 28 to − 0.3	Vdc

NOTE Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

MODE SELECTION

Mode	Pin Number			
	9-11, 13-17, DQ	12 V_{SS}	20 $\overline{E}/V_{PP}$	24 V_{CC}
Read	Data out	V_{SS}	V_{IL}	V_{CC}
Output Disable	High Z	V_{SS}	V_{IH}	V_{CC}
Standby	High Z	V_{SS}	V_{IH}	V_{CC}
Program	Data in	V_{SS}	Pulsed V_{ILP} to V_{IHP}	V_{CC}

BLOCK DIAGRAM

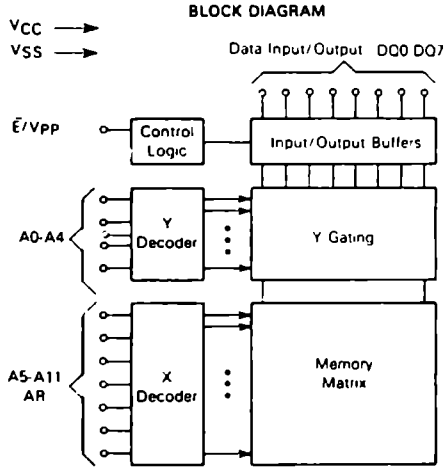
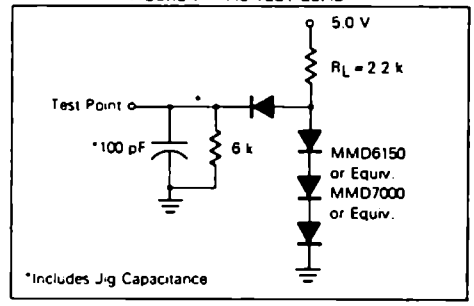


FIGURE 1 — AC TEST LOAD



CAPACITANCE (f = 1.0 MHz, T_A = 25°C, periodically sampled rather than 100% tested.)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance (V_{in} = 0 V) Except Ē/V_{PP}	C_{in}	4.0	6.0	pF
Input Capacitance Ē/V_{PP}	C_{in}	60	100	pF
Output Capacitance (V_{out} = 0 V)	C_{out}	8.0	12	pF

Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: $C = I\Delta t/\Delta V$

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted)

RECOMMENDED DC OPERATING CONDITIONS

Parameter		Symbol	Min	Nom	Max	Unit
Supply Voltage	MCM68L732/MCM68732 MCM68L732-35/MCM68732-35	V_{CC}	4.75 4.5	5.0 5.0	5.25 5.5	V
Input High Voltage		V_{IH}	2.0	–	V_{CC} + 1.0	V
Input Low Voltage		V_{IL}	−0.1	–	0.8	V

RECOMMENDED DC OPERATING CHARACTERISTICS

Characteristic	Condition	Symbol	MCM68732			MCM68L732			Units
			Min	Typ	Max	Min	Typ	Max	
Address Input Sink Current	V_{in} = 5.25 V	I_{in}	–	–	10	–	–	10	μA
Output Leakage Current	V_{out} = 5.25 V	I_{LO}	–	–	10	–	–	10	μA
$\overline{E}$/Vpp Input Sink Current	$\overline{E}$/Vpp = 0.4	I_{EL}	–	–	100	–	–	100	μA
	$\overline{E}$/Vpp = 2.4	I_{EH} = I_{PL}	–	–	400	–	–	400	μA
V_{CC} Supply Current (Standby) MCM68732	$\overline{E}$/Vpp = V_{IH}	I_{CC1}	–	–	25		–	15	mA
V_{CC} Supply Current (Standby) MCM68732-35	$\overline{E}$/Vpp = V_{IH}	I_{CC1}	–	–	25	–	–	25	mA
V_{CC} Supply Current (Active) MCM68732 (Outputs Open)	$\overline{E}$/Vpp = V_{IL}	I_{CC2}	–	–	120	–	–	60	mA
V_{CC} Supply Current (Active) MCM68732-35 (Outputs Open)	$\overline{E}$/Vpp = V_{IL}	I_{CC2}	–	–	160	–	–	100	mA
Output Low Voltage	I_{OL} = 2.1 mA	V_{OL}	–	–	0.45		–	0.45	V
Output High Voltage	I_{OH} = −400 μA	V_{OH}	2.4	–	–	2.4	–		V

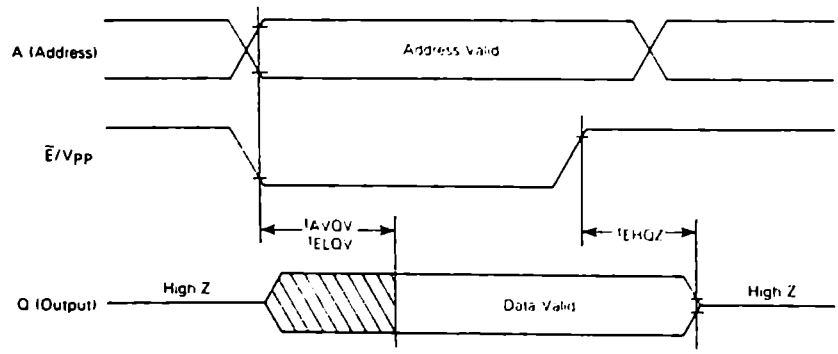
AC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted)

Input Pulse Levels	0.8 Volt and 2.2 Volts	Output Timing Levels	0.8 Volt and 2 Volts
Input Rise and Fall Times	20 ns	Output Load	See Figure 1
Input Timing Levels	1.0 Volt and 2 Volts		

Characteristic	Condition	Symbol	MCM68732-35		MCM68732		Units
			Min	Max	Min	Max	
Address Valid to Output Valid	$\overline{E}$ = V_{IL}	t_{AVQV}	–	350	–	450	ns
$\overline{E}$ to Output Valid	–	t_{ELQV}	–	350	–	450	ns
$\overline{E}$ to Hi-Z Output	–	t_{EHQZ}	0	100	0	100	ns
Data Hold from Address	$\overline{E}$ = V_{IL}	t_{AXDX}	0	–	0	–	ns

READ MODE TIMING DIAGRAM



DC PROGRAMMING CONDITIONS AND CHARACTERISTICS

(T_A = 25 ± 5°C)

RECOMMENDED PROGRAMMING OPERATING CONDITIONS

Parameter	Symbol	Min	Nom	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
Input High Voltage for All Addresses and Data	V_{IH}	2.2	–	V_{CC} + 1	V
Input Low Voltage for All Addresses and Data	V_{IL}	–0.1	–	0.8	V
Program Pulse Input High Voltage	V_{IHP}	24	25	26	V
Program Pulse Input Low Voltage	V_{ILP}	2.0	V_{CC}	6.0	V

PROGRAMMING OPERATION DC CHARACTERISTICS

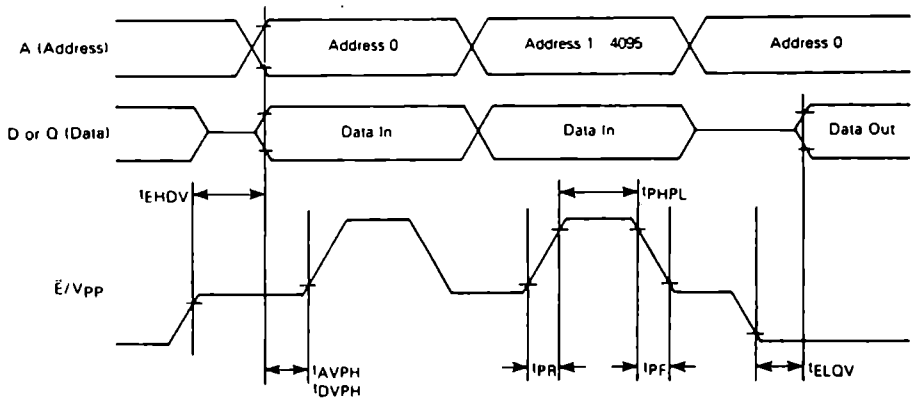
Characteristic	Condition	Symbol	Min	Typ	Max	Unit
Address Input Sink Current	V_{in} = 5.25 V	I_{LI}	–	–	10	µA
Vpp Program Pulse Supply Current (Vpp = 25 V ± 1 V)	–	I_{PH}	–	–	30	mA
Vpp Supply Current (Vpp = 2.4 V)	–	I_{PL} = I_{EH}	–	–	400	µA
V_{CC} Supply Current (Vpp = 5.0 V)	–	I_{CC}	–	–	160	mA

AC PROGRAMMING OPERATING CONDITIONS AND CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit
Address Setup Time	t_{AVPH}	2.0	–	µs
Data Setup Time	t_{DVPH}	2.0	–	µs
Chip Enable to Valid Data	t_{ELQV}	450	–	ns
Chip Disable to Data In	t_{EHDV}	2.0	–	µs
Program Pulse Width	t_{PHPL}	1.9	2.1	ms
Program Pulse Rise Time	t_{PR}	0.5	2.0	µs
Program Pulse Fall Time	t_{PF}	0.5	2.0	µs
Cumulative Programming Time Per Word*	t_{CP}	12	50	ms

*Block mode programming must be used. Block mode programming is defined as one program pulse applied to each of the 4096 address locations in sequence. Multiple blocks are used to accumulate programming time (t_{CP}).

PROGRAMMING OPERATION TIMING DIAGRAM



PROGRAMMING INSTRUCTIONS

After the completion of an ERASE operation, every bit in the device is in the "1" state (represented by Output High). Data are entered by programming zeros (Output Low) into the required bits. The words are addressed the same way as in the READ operation. A programmed "0" can only be changed to a "1" by ultraviolet light erasure.

To set the memory up for Program Mode, the $\overline{E}$/Vpp input (Pin 20) should be between +2.0 and +6.0 V, which will three-state the outputs and allow data to be setup on the DQ terminals. The V_{CC} voltage is the same as for the Read operation. Only "0's" will be programmed when "0's" and "1's" are entered in the 8-bit data word.

After address and data setup, 25-volt programming pulse (V_{IH} to V_{IHP}) is applied to the E/Vpp input. A program pulse is applied to each address location to be programmed. The maximum program pulse width is 2 ms and the maximum program pulse amplitude is 26 V.

Multiple MCM68732s may be programmed in parallel by connecting like inputs and applying the program pulse to the $\overline{E}$/Vpp inputs. Different data may be programmed into multiple MCM68732s connected in parallel by selectively applying the programming pulse only to the MCM68732s to be programmed.

READ OPERATION

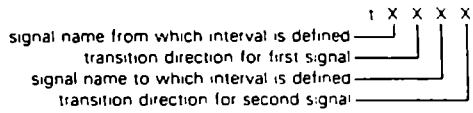
After access time, data is valid at the outputs in the Read mode. A single input ($\overline{E}$/Vpp) enables the outputs and puts the chip in active or standby mode. With $\overline{E}$/Vpp = "0" the outputs are enabled and the chip is in active mode; with $\overline{E}$/Vpp = "1" the outputs are three-stated and the chip is in standby mode. During standby mode, the power dissipation is reduced.

Multiple MCM68732s may share a common data bus with like outputs OR-tied together. In this configuration the E/Vpp input should be high on all unselected MCM68732s to prevent data contention.

ERASING INSTRUCTIONS

The MCM68732 can be erased by exposure to high intensity shortwave ultraviolet light, with a wavelength of 2537 angstroms. The recommended integrated dose (i.e., UV-intensity X exposure time) is 15 Ws/cm^2. As an example, using the "Model 30-000" UV-Eraser (Turner Designs, Mountain View, CA 94043) the ERASE-time is 36 minutes. The lamps should be used without shortwave filters and the MCM68732 should be positioned about one inch away from the UV-tubes.

TIMING PARAMETER ABBREVIATIONS


t X X X X
signal name from which interval is defined
transition direction for first signal
signal name to which interval is defined
transition direction for second signal

The transition definitions used in this data sheet are:

- H = transition to high
- L = transition to low
- V = transition to valid
- X = transition to invalid or don't care
- Z = transition to off (high impedance)

TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

WAVEFORMS

Waveform Symbol	Input	Output
———	Must Be Valid	Will Be Valid
▨	Change From H to L	Will Change From H to L
▨	Change From L to H	Will Change From L to H
▨	Don't Care Any Change Permitted	Changing State Unknown
———		High Impedance

MOTOROLA

MCM68764
MCM68L764

8192 × 8-BIT UV ERASABLE PROM

The MCM68764/68L764 is a 65,536-bit Erasable and Electrically Reprogrammable PROM designed for system debug usage and similar applications requiring nonvolatile memory that could be reprogrammed periodically, or for replacing 64K ROMs for fast turnaround time. The transparent window on the package allows the memory content to be erased with ultraviolet light.

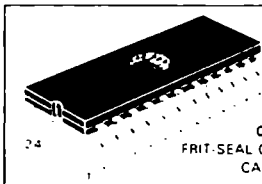
For ease of use, the device operates from a single power supply and has a static power-down mode. Pin-for-pin mask programmable ROMs are available for large volume production runs of systems initially using the MCM68764/68L764.

- Single +5 V Power Supply
- Automatic Power-down Mode (Standby) with Chip Enable
- Organized as 8192 Bytes of 8 Bits
- Low Power Dissipation
- Fully TTL Compatible
- Maximum Access Time = 450 ns MCM68764
  350 ns MCM68764-35
- Standard 24-Pin DIP for EPROM Upgradability
- Pin Compatible to MCM68A364 Mask Programmable ROM
- Low Power Version
  MCM68L764 Active 60 mA Maximum
  Standby 15 mA Maximum
  MCM68L764-35 Active 100 mA Maximum
  Standby 25 mA Maximum

MOS

(N-CHANNEL, SILICON-GATE)

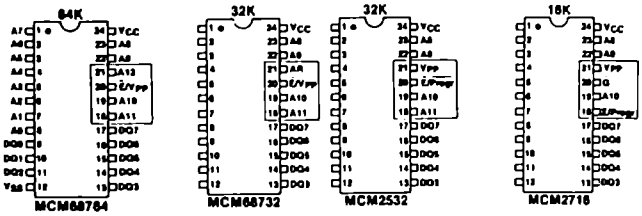
8192 × 8-BIT
UV ERASABLE
PROGRAMMABLE READ
ONLY MEMORY



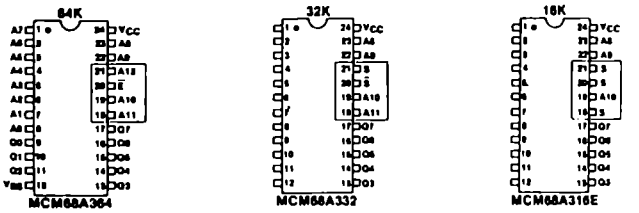
C SUFFIX
FRIT-SEAL CERAMIC PACKAGE
CASE 623A-02

L SUFFIX CERAMIC PACKAGE
ALSO AVAILABLE — CASE 716-07

MOTOROLA'S PIN-COMPATIBLE EPROM FAMILY

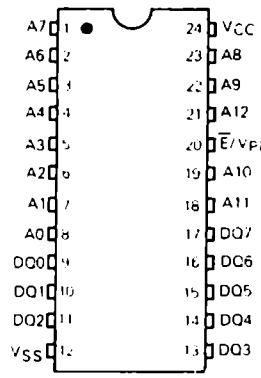


MOTOROLA'S PIN-COMPATIBLE ROM FAMILY



INDUSTRY STANDARD PINOUTS

PIN ASSIGNMENT



*Pin Names	
A	Address
DQ	Data Input/Output
$\overline{E}$/Vpp	Chip Enable/Program

*New industry standard nomenclature

DS9815 R1/9-80

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Value	Unit
Temperature Under Bias	− 10 to + 80	°C
Operating Temperature Range	0 to + 70	°C
Storage Temperature	− 65 to + 125	°C
All Input or Output Voltages with Respect to V_{SS}	+ 6 to − 0.3	Vdc
V_{PP} Supply Voltage with Respect to V_{SS}	+ 28 to − 0.3	Vdc

NOTE Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields, however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

MODE SELECTION

Mode	Pin Number			
	9-11, 13-17, DQ	12 V_{SS}	20 $\overline{E}/V_{PP}$	24 V_{CC}
Read	Data out	V_{SS}	V_{IL}	V_{CC}
Output Disable	High-Z	V_{SS}	V_{IH}	V_{CC}
Standby	High-Z	V_{SS}	V_{IH}	V_{CC}
Program	Data in	V_{SS}	Pulsed V_{ILP} to V_{IHP}	V_{CC}

BLOCK DIAGRAM

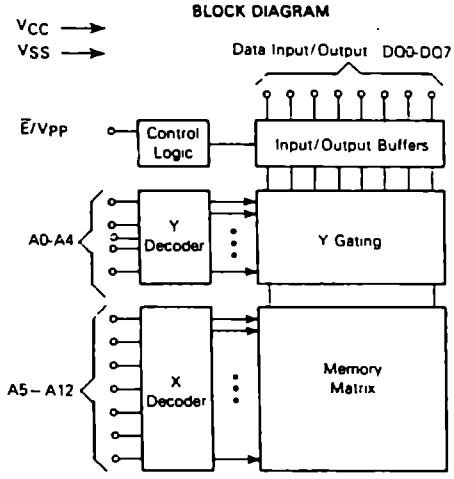
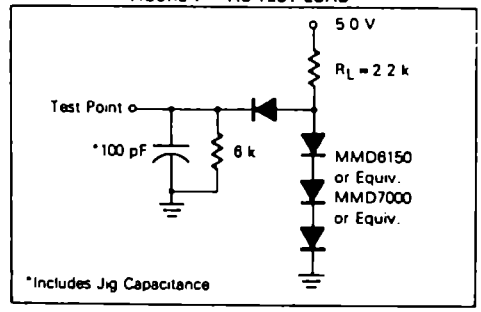


FIGURE 1 — AC TEST LOAD



DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted)

RECOMMENDED DC OPERATING CONDITIONS

Parameter		Symbol	Min	Nom	Max	Unit
Supply Voltage	MCM68L764/MCM68764 MCM68764-35/MCM68L764-35	V_{CC}	4.75 4.5	5.0 5.0	5.25 5.5	Vdc
Input High Voltage		V_{IH}	2.0	–	V_{CC} + 1.0	Vdc
Input Low Voltage		V_{IL}	−0.1	–	0.8	Vdc

RECOMMENDED DC OPERATING CHARACTERISTICS

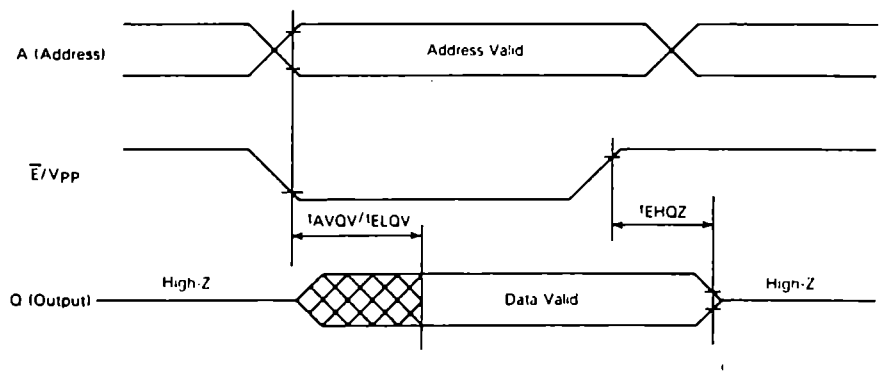
Characteristic	Condition	Symbol	MCM68764			MCM68L764			Units
			Min	Typ	Max	Min	Typ	Max	
Address Input Sink Current	V_{in} = 5.25 V	I_{in}	–	–	10	–	–	10	μA
Output Leakage Current	V_{out} = 5.25 V	I_{LO}	–	–	10	–	–	10	μA
$\overline{E}$/Vpp Input Sink Current	$\overline{E}$/Vpp = 0.4	I_{EL}	–	–	100	–	–	100	μA
	$\overline{E}$/Vpp = 2.4	$I_{EH} = I_{PL}$	–	–	400	–	–	400	μA
V_{CC} Supply Current (Standby) MCM68764	$\overline{E}$/Vpp = V_{IH}	I_{CC1}	–	–	25	–	–	15	mA
V_{CC} Supply Current (Standby) MCM68764-35	$\overline{E}$/Vpp = V_{IH}	I_{CC1}	–	–	25	–	–	25	mA
V_{CC} Supply Current (Active) MCM68764 (Outputs Open)	$\overline{E}$/Vpp = V_{IL}	I_{CC2}	–	–	120	–	–	60	mA
V_{CC} Supply Current (Active) MCM68764-35 (Outputs Open)	$\overline{E}$/Vpp = V_{IL}	I_{CC2}	–	–	160	–	–	100	mA
Output Low Voltage	I_{OL} = 2.1 mA	V_{OL}	–	–	0.45	–	–	0.45	V
Output High Voltage	I_{OH} = −400 μA	V_{OH}	2.4	–	–	2.4	–	–	V

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, periodically sampled rather than 100% tested.)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance (V_{in} = 0 V) Except $\overline{E}$/Vpp	C_{in}	4.0	6.0	pF
Input Capacitance $\overline{E}$/Vpp	C_{in}	60	100	pF
Output Capacitance (V_{out} = 0 V)	C_{out}	8.0	12	pF

Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation $C = \frac{I\Delta_t}{\Delta V}$

READ MODE TIMING DIAGRAM



AC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted)

Input Pulse Levels ..... 0.8 Volt and 2.2 Volts
Input Rise and Fall Times ..... 20 ns
Input Timing Levels ..... 1.0 and 2 Volts
Output Timing Levels ..... 0.8 Volt and 2 Volts
Output Load ..... See Figure 1

Characteristic	Condition	Symbol	MCM68764-35		MCM68764		Units
			Min	Max	Min	Max	
Address Valid to Output Valid	$\overline{E}$ = V_{IL}	t_{AVQV}	–	350	–	450	ns
$\overline{E}$ to Output Valid	–	t_{ELQV}	–	350	–	450	ns
$\overline{E}$ to Hi-Z Output	–	t_{EHQZ}	0	100	0	100	ns
Data Hold from Address	$\overline{E}$ = V_{IL}	t_{AXDX}	0	–	0	–	ns

DC PROGRAMMING CONDITIONS AND CHARACTERISTICS

(T_A = 25 ± 5°C)

RECOMMENDED PROGRAMMING OPERATING CONDITIONS

Parameter	Symbol	Min	Nom	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
Input High Voltage for All Addresses and Data	V_{IH}	2.2	–	V_{CC} + 1	V
Input Low Voltage for All Addresses and Data	V_{IL}	-0.1	–	0.8	V
Program Pulse Input High Voltage	V_{IHP}	24	25	26	V
Program Pulse Input Low Voltage	V_{ILP}	2.0	V_{CC}	6.0	V

PROGRAMMING OPERATION DC CHARACTERISTICS

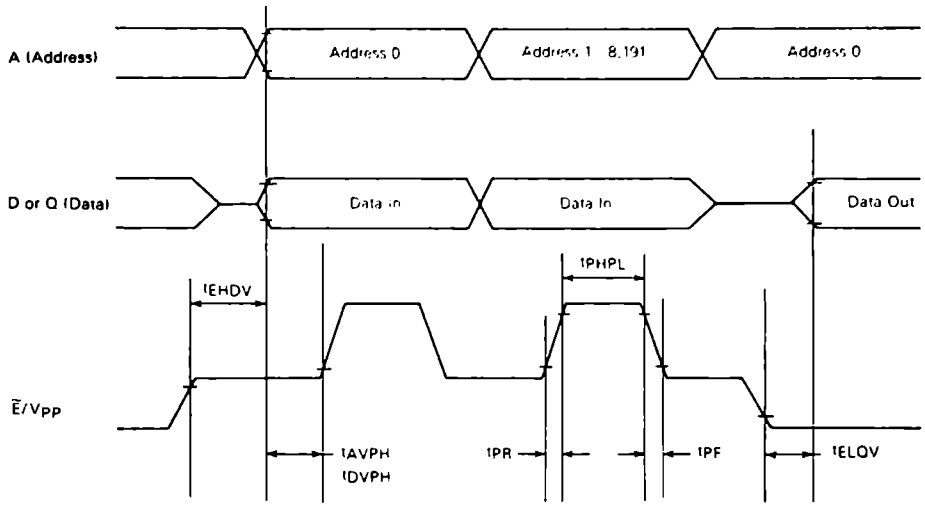
Characteristic	Condition	Symbol	Min	Typ	Max	Unit
Address Input Sink Current	V_{in} = 5.25 V	I_{LI}	–	–	10	μA
V_{PP} Program Pulse Supply Current (V_{PP} = 25 V ± 1 V)	–	I_{PH}	–	–	30	mA
V_{PP} Supply Current (V_{PP} = 2.4 V)	–	I_{PL} = I_{EH}	–	–	400	μA
V_{CC} Supply Current (V_{PP} = 6.0 V)	–	I_{CC}	–	–	160	mA

AC PROGRAMMING OPERATING CONDITIONS AND CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit
Address Setup Time	t_{AVPH}	2.0	–	μs
Data Setup Time	t_{DVPH}	2.0	–	μs
Chip Enable to Valid Data	t_{ELQV}	450		ns
Chip Disable to Data In	t_{EHDV}	2.0	–	μs
Program Pulse Width	t_{PHPL}	1.9	2.1	ms
Program Pulse Rise Time	t_{PR}	0.5	2.0	μs
Program Pulse Fall Time	t_{PF}	0.5	2.0	μs
Cumulative Programming Time Per Word*	t_{CP}	12	60	ms

*Block mode programming must be used. Block mode programming is defined as one program pulse applied to each of the 8,192 address locations in sequence. Multiple blocks are used to accumulate programming time (t_{CP}).

PROGRAMMING OPERATION TIMING DIAGRAM



PROGRAMMING INSTRUCTIONS

After the completion of an ERASE operation, every bit in the device is in the "1" state (represented by Output High). Data are entered by programming zeros (Output Low) into the required bits. The words are addressed the same way as in the READ operation. A programmed "0" can only be changed to a "1" by ultraviolet light erasure.

To set the memory up for Program Mode, the Ē/Vpp input (Pin 20) should be between +2.0 and +6.0 V, which will three-state the outputs and allow data to be setup on the DQ terminals. The V_{CC} voltage is the same as for the Read operation. Only "0's" will be programmed when "0's" and "1's" are entered in the 8-bit data word.

After address and data setup, 25-volt programming pulse (V_{IH} to V_{IHP}) is applied to the Ē/Vpp input. The program pulse width is 2 ms and the maximum program pulse amplitude is 26 V.

Multiple MCM68764s may be programmed in parallel by connecting like inputs and applying the program pulse to the Ē/Vpp inputs. Different data may be programmed into multiple MCM68764s connected in parallel by selectively applying the programming pulse only to the MCM68764s to be programmed.

READ OPERATION

After access time, data is valid at the outputs in the Read mode. A single input (Ē/Vpp) enables the outputs and puts the chip in active or standby mode. With Ē/Vpp = "0" the outputs are enabled and the chip is in active mode; with Ē/Vpp = "1" the outputs are three-stated and the chip is in standby mode. During standby mode, the power dissipation is reduced.

Multiple MCM68764s may share a common data bus with like outputs OR-tied together. In this configuration, only one Ē/Vpp input should be low and no other device outputs should be active on the same bus. This will prevent data contention on the bus.

ERASING INSTRUCTIONS

The MCM68764 can be erased by exposure to high intensity shortwave ultraviolet light, with a wavelength of 2537 angstroms. The recommended integrated dose (i.e., UV-intensity X exposure time) is 15 Ws/cm^2. As an example, using the "Model 30-000" UV-Eraser (Turner Designs, Mountain View, CA 94043) the ERASE-time is 36 minutes. The lamps should be used without shortwave filters and the MCM68764 should be positioned about one inch away from the UV-tubes.

MOTOROLA

MCM68766

Advance Information

8192 × 8-BIT UV ERASABLE PROM

The MC68766 is a 65,536-bit Erasable and Electrically Reprogrammable PROM designed for system debug usage and similar applications requiring nonvolatile memory that could be reprogrammed periodically, or for replacing 64K ROMs for fast turnaround time. The transparent window on the package allows the memory content to be erased with ultraviolet light.

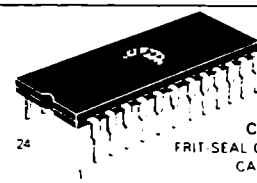
For ease of use, the device operates from a single power supply that has an output enable control and is pin-for-pin compatible with the MCM68366 mask programmable ROMs, which are available for large volume production runs of systems initially using the MCM68766.

- Single +5 V Power Supply
- Organized as 8192 Bytes of 8 Bits
- Fully TTL Compatible
- Maximum Access Time = 450 ns MCM68766
  350 ns MCM68766-35
- Standard 24-Pin DIP for EPROM Upgradability
- Pin Compatible to MCM68366 Mask Programmable ROM
- Power Dissipation — 160 mA Maximum

MOS

(N-CHANNEL, SILICON-GATE)

8192 × 8-BIT UV ERASABLE PROGRAMMABLE READ ONLY MEMORY

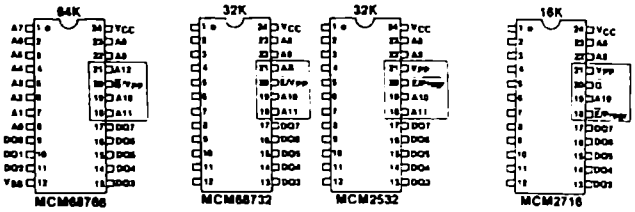


24 1

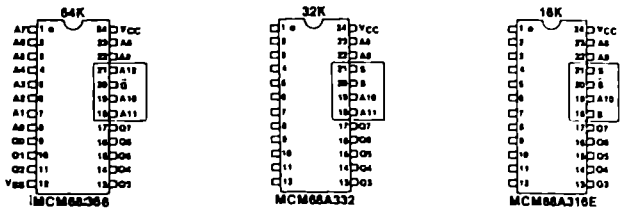
C SUFFIX
FRIT-SEAL CERAMIC PACKAGE
CASE 623A-02

L SUFFIX CERAMIC PACKAGE
ALSO AVAILABLE — CASE 716-07

MOTOROLA'S PIN-COMPATIBLE EPROM FAMILY

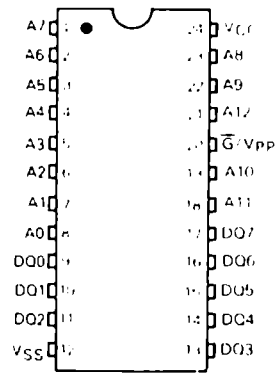


MOTOROLA'S PIN-COMPATIBLE ROM FAMILY



INDUSTRY STANDARD PINOUTS

PIN ASSIGNMENT



*Pin Names	
A	Address
DQ	Data Input/Output
$\overline{G}$/Vpp	Output Enable/ Program

*New industry standard nomenclature

ADI843/9-80

ABSOLUTE MAXIMUM RATINGS

Rating	Value	Unit
Temperature Under Bias	−10 to +80	°C
Operating Temperature Range	0 to +70	°C
Storage Temperature	−65 to +125	°C
All Input or Output Voltages with Respect to V_{SS}	+6 to −0.3	Vdc
V_{PP} Supply Voltage with Respect to V_{SS}	+28 to −0.3	Vdc

NOTE Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

MODE SELECTION

Mode	Pin Number			
	9-11, 13-17, DQ	12 V_{SS}	20 $\overline{G}/V_{PP}$	24 V_{CC}
Read	Data Out	V_{SS}	V_{IL}	V_{CC}
Output Disable	High-Z	V_{SS}	V_{IH}	V_{CC}
Program	Data In	V_{SS}	Pulsed V_{ILP} to V_{IHP}	V_{CC}

BLOCK DIAGRAM

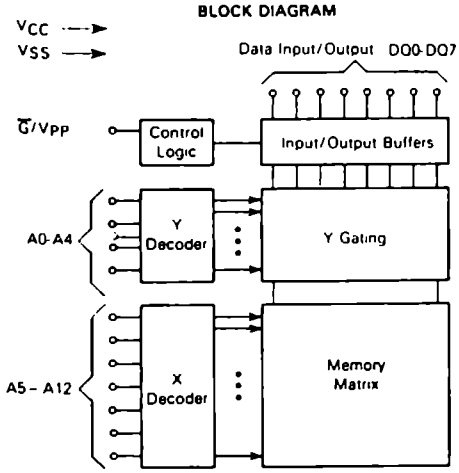
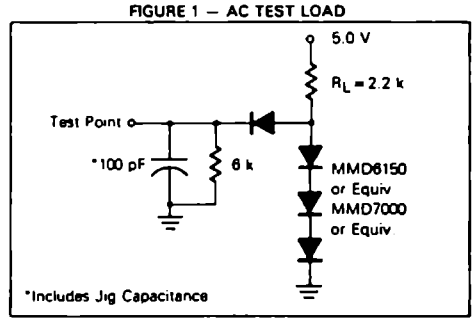


FIGURE 1 — AC TEST LOAD



CAPACITANCE (f = 1.0 MHz, T_A = 25°C, V_{CC} = 5 V periodically sampled rather than 100% tested)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance (V_{in} = 0 V) Except $\overline{G}$/Vpp	C_{in}	4.0	6.0	pF
Input Capacitance ($\overline{G}$/Vpp)	C_{in}	60	100	pF
Output Capacitance (V_{out} = 0 V)	C_{out}	8.0	12	pF

Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: $C = I\Delta_t/\Delta V$.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted)

RECOMMENDED DC OPERATING CONDITIONS

Parameter		Symbol	Min	Nom	Max	Unit
Supply Voltage	MCM68766 MCM68766-35	V_{CC}	4.75 4.5	5.0 5.0	5.25 5.5	Vdc
Input High Voltage		V_{IH}	2.0	–	V_{CC} + 1.0	Vdc
Input Low Voltage		V_{IL}	−0.1	–	0.8	Vdc

DC OPERATING CHARACTERISTICS

Characteristic	Condition	Symbol	Min	Typ	Max	Units
Address Input Sink Current	V_{in} = 5.25 V	I_{in}	–	–	10	μA
Output Leakage Current	V_{out} = 5.25 V	I_{LO}	–	–	10	μA
$\overline{G}$/Vpp Input Sink Current	$\overline{G}$/Vpp = 0.4 V	I_{GL}	–	–	100	μA
	$\overline{G}$/Vpp = 2.4 V	$I_{GH} = I_{PL}$	–	–	400	μA
V_{CC} Supply Current (Outputs Open)	$\overline{G}$/Vpp = V_{IL}	I_{CC}	–	–	160	mA
Output Low Voltage	I_{OL} = 2.1 mA	V_{OL}	–	–	0.45	V
Output High Voltage	I_{OH} = −400 μA	V_{OH}	2.4	–	–	V

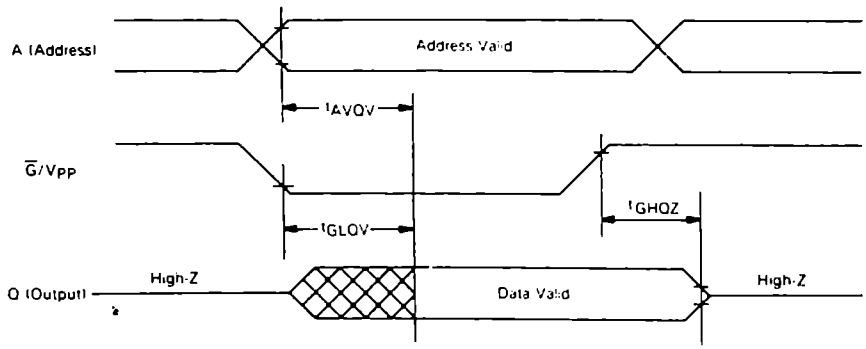
AC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted)

Input Pulse Levels ..... 0.8 Volt and 2.2 Volts
Input Rise and Fall Times ..... 20 ns
Input Timing Levels ..... 1.0 Volt and 2 Volts
Output Timing Levels ..... 0.8 Volt and 2 Volts
Output Load ..... See Figure 1

Characteristic	Condition	Symbol	MCM68766-35		MCM68766		Units
			Min	Max	Min	Max	
Address Valid to Output Valid	$\overline{G} = V_{IL}$	t_{AVQV}	–	350	–	450	ns
$\overline{G}$ to Output Valid	–	t_{GLQV}	–	150	–	150	ns
$\overline{G}$ to Hi-Z Output	–	t_{GHQZ}	0	100	0	100	ns
Data Hold from Address	$\overline{G} = V_{IL}$	t_{AXDX}	0	–	0	–	ns

READ MODE TIMING DIAGRAM



DC PROGRAMMING CONDITIONS AND CHARACTERISTICS

(T_A = 25 ± 5°C)

RECOMMENDED PROGRAMMING OPERATING CONDITIONS

Parameter	Symbol	Min	Nom	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	Vdc
Input High Voltage for All Addresses and Data	V_{IH}	2.2	–	V_{CC} + 1	Vdc
Input Low Voltage for All Addresses and Data	V_{IL}	-0.1	–	0.8	Vdc
Program Pulse Input High Voltage	V_{IHP}	24	25	26	Vdc
Program Pulse Input Low Voltage	V_{ILP}	2.0	V_{CC}	6.0	Vdc

PROGRAMMING OPERATION DC CHARACTERISTICS

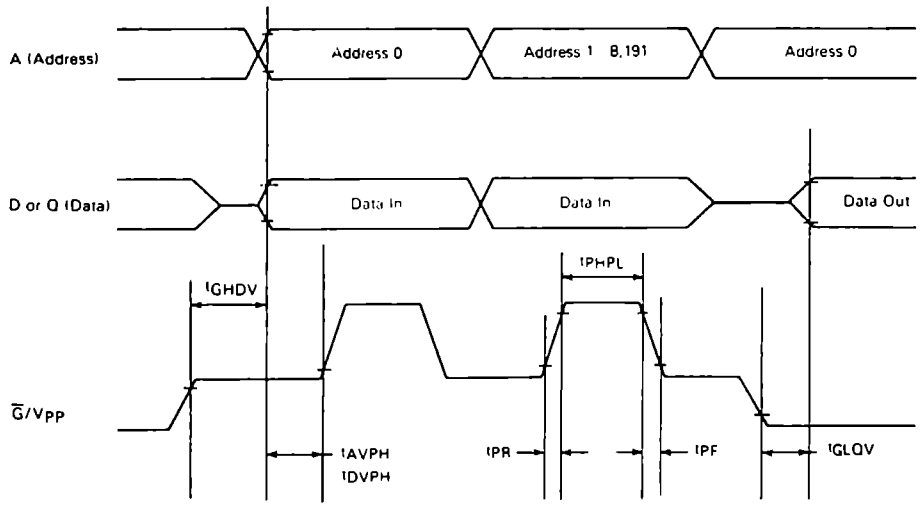
Characteristic	Condition	Symbol	Min	Typ	Max	Unit
Address Input Sink Current	V_{in} = 5.25 V	I_{LI}	–	–	10	μAdc
Vpp Program Pulse Supply Current (Vpp = 25 V ± 1 V)	–	I_{PH}	–	–	30	mAdc
Vpp Supply Current (Vpp = 2.4 V)	–	I_{PL} = I_{GH}	–	–	400	μA
V_{CC} Supply Current (Vpp = 5 V)	–	I_{CC}	–	–	160	mAdc

AC PROGRAMMING OPERATING CONDITIONS AND CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit
Address Setup Time	t_{AVPH}	2.0	–	μs
Data Setup Time	t_{DVPH}	2.0	–	μs
Output Enable to Valid Data	t_{GLQV}	150	–	ns
Output Disable to Data In	t_{GHDV}	2.0	–	μs
Program Pulse Width	t_{PHPL}	1.9	2.1	ms
Program Pulse Rise Time	t_{PR}	0.5	2.0	μs
Program Pulse Fall Time	t_{PF}	0.5	2.0	μs
Cumulative Programming Time Per Word*	t_{CP}	12	50	ms

*Block mode programming must be used. Block mode programming is defined as one program pulse applied to each of the 8,192 address locations in sequence. Multiple blocks are used to accumulate programming time (t_{CP}).

PROGRAMMING OPERATION TIMING DIAGRAM



PROGRAMMING INSTRUCTIONS

After the completion of an ERASE operation, every bit in the device is in the "1" state (represented by Output High). Data are entered by programming zeros (Output Low) into the required bits. The words are addressed the same way as in the READ operation. A programmed "0" can only be changed to a "1" by ultraviolet light erasure.

To set the memory up for Program Mode, the $\overline{G}$/Vpp input (Pin 20) should be between +2.0 and +6.0 V, which will three-state the outputs and allow data to be set up on the DQ terminals. The V_{CC} voltage is the same as for the Read operation. Only "0's" will be programmed when "0's" and "1's" are entered in the 8-bit data word.

After address and data setup, 25-volt programming pulse (V_{IH} to V_{IHP}) is applied to the G/Vpp input. The program pulse width is 2 ms and the maximum program pulse amplitude is 26 V.

Multiple MCM68766s may be programmed in parallel by connecting like inputs and applying the program pulse to the $\overline{G}$/Vpp inputs. Different data may be programmed into multiple MCM68766s connected in parallel by selectively applying the programming pulse only to the MCM68766s to be programmed.

READ OPERATION

After access time, data is valid at the outputs in the Read mode. With $\overline{G}$/Vpp = "0" the outputs are enabled, with $\overline{G}$/Vpp = "1" the outputs are three-stated.

Multiple MCM68766s may share a common data bus with like outputs OR-tied together. In this configuration only one $\overline{G}$/Vpp input should be low and no other device outputs should be active on the same bus. This will prevent data contention on the bus.

ERASING INSRUCTIONS

The MCM68766 can be erased by exposure to high intensity shortwave ultraviolet light, with a wavelength of 2537 angstroms. The recommended integrated dose (i.e., UV intensity X exposure time) is 15 Ws/cm^2. As an example, using the "Model 30-000" UV Eraser (Turner Designs, Mountain View, CA 94043) the ERASE-time is 36 minutes. The lamps should be used without shortwave filters and the MCM68766 should be positioned about one inch away from the UV-tubes.

MOTOROLA
SEMICONDUCTORS
3501 ED BLUESTEIN BLVD., AUSTIN, TEXAS 78721

MCM2801

Advance Information

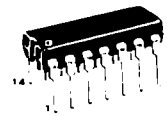
16 × 16-BIT SERIAL ELECTRICALLY ERASABLE PROM

The MCM2801 is a 256-bit serial Electrically Erasable PROM designed for handling small amounts of data in applications requiring both non-volatile memory and in-system information updates.

The MCM2801 offers in-system erase and reprogram capability. It has external control of timing functions and serial format for data and address. The MCM2801 is fabricated in floating gate technology for high reliability and producibility.

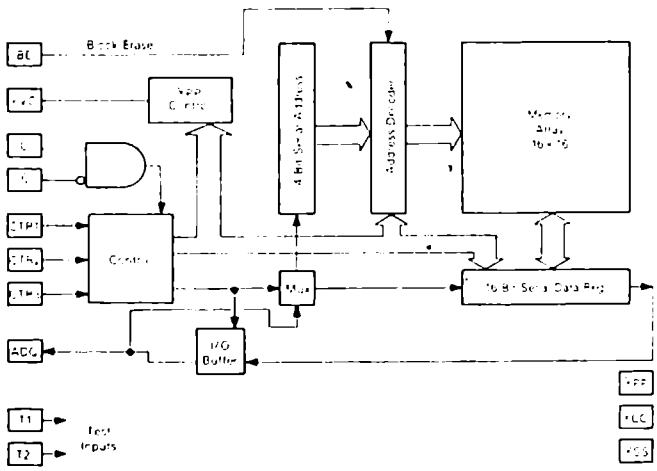
- Single +5 V Power Supply
- Organized as 16 Words of 16 Bits
- MPU Bus Compatible
- Single +25 V Power Supply for Erase and Program
- In-System Program/Erase Capability
- Both Word and Whole Array Erasable

MOS
(N-CHANNEL, SILICON GATE)
16 × 16 BIT
ELECTRICALLY ERASABLE
PROGRAMMABLE READ
ONLY MEMORY

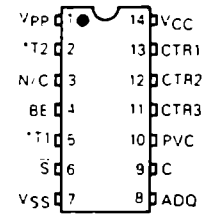


PLASTIC PACKAGE
CASE 646-06

BLOCK DIAGRAM



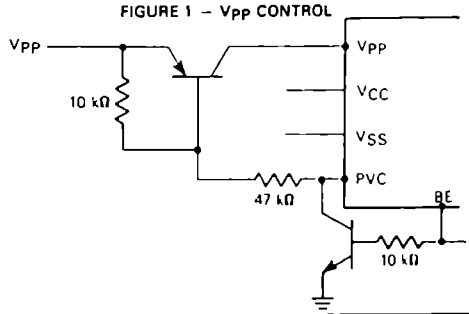
PIN ASSIGNMENT



*For normal operation, these inputs should be hardwired to V_{SS}.

PIN NAMES	
ADO	Multiplexed Address/ Data-In/Data-Out
C	Clock
PVC	Program Voltage Control
CTR1, 2, 3	Control
$\overline{BE}$	Block Erase
$\overline{S}$	Chip Select
T1, T2	Test Pins

FIGURE 1 – Vpp CONTROL



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

This is advance information and specifications are subject to change without notice.
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ADI 841 R1

MODE SELECTION

Mode	Pin Number						
	1 V_{PP}	6 $\overline{S}$	7 V_{SS}	11 CTR3	12 CTR2	13 CTR1	14 V_{CC}
Standby	V_{SS} or V_{CC}	V_{IH}	V_{SS}	V_{IH}	V_{IH}	V_{IH}	V_{CC}
Word Erase	V_{PP}	V_{IL}	V_{SS}	V_{IH}	V_{IL}	V_{IL}	V_{CC}
Write	V_{PP}	V_{IL}	V_{SS}	V_{IL}	V_{IH}	V_{IL}	V_{CC}
Serial Data Out	V_{SS} or V_{CC}	V_{IL}	V_{SS}	V_{IH}	V_{IH}	V_{IL}	V_{CC}
Serial Address In	V_{SS} or V_{CC}	V_{IL}	V_{SS}	V_{IL}	V_{IL}	V_{IH}	V_{CC}
Serial Data In	V_{SS} or V_{CC}	V_{IL}	V_{SS}	V_{IH}	V_{IL}	V_{IH}	V_{CC}
Read	V_{SS} or V_{CC}	V_{IL}	V_{SS}	V_{IL}	V_{IH}	V_{IH}	V_{CC}
Standby	V_{SS} or V_{CC}	V_{IH}	V_{SS}	V_{IL}	V_{IL}	V_{IL}	V_{CC}

ABSOLUTE MAXIMUM RATINGS (1)

Rating	Value	Unit
Temperature Under Bias	− 40 to + 85	°C
Operating Temperature Range	0 to + 70	°C
Storage Temperature	− 55 to + 150	°C
All Input or Output Voltages with Respect to V_{SS} (Except PVC)	+ 8 to − 0.5	V
V_{PP} Supply Voltage with Respect to V_{SS}	+ 28 to − 0.5	V
PVC Voltage with Respect to V_{SS}	+ 28 to − 0.5	V

NOTE 1 Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS (Full operating voltage and temperature range unless otherwise noted.)

Parameter	Symbol	Min	Nom	Max	Unit
Supply Voltage	V_{CC} V_{PP}	4.5 24.0	5.0 25	5.5 26.0	V
Input High Voltage	V_{IH}	2.4	–	V_{CC} + 1.0	V
Input Low Voltage	V_{IL}	− 0.1	–	0.8	V

OPERATING DC CHARACTERISTICS

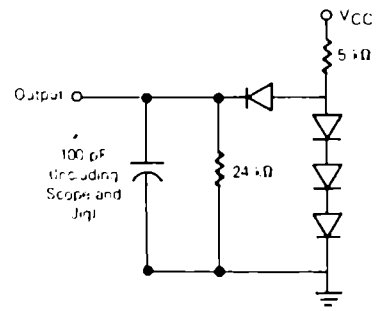
Characteristic	Condition	Symbol	Min	Typ	Max	Units
Input Sink Current	$0 < V_{in} < V_{CC}$	I_{in}	–	–	10	μA
V_{CC} Supply Current	V_{CC} = 5.5 V	I_{CC}	–	–	30	mA
V_{PP} Supply Current	V_{PP} = 26.0 V	I_{PP}	–	–	4.0	mA
Output Low Voltage	I_{OL} = 1.0 mA	V_{OL}	–	–	0.5	V
Output High Voltage	I_{OH} = − 0.1 mA	V_{OH}	2.4	–	–	V
PVC Current (Write or Word Erase)	PVCL = 1 V	PVC_{ON}	200	–	–	μA
PVC Leakage	PVCH = 26 V	PVC_{OFF}	–	–	5	μA

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, V_{CC} = +5 V, periodically sampled rather than 100% tested.)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance (V_{in} = 0 V)	C_{in}		6.0	pF
Output Capacitance (V_{out} = 0 V)	C_{out}		12	pF

Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: $C = I\Delta t/\Delta V$

FIGURE 2 — OUTPUT LOAD



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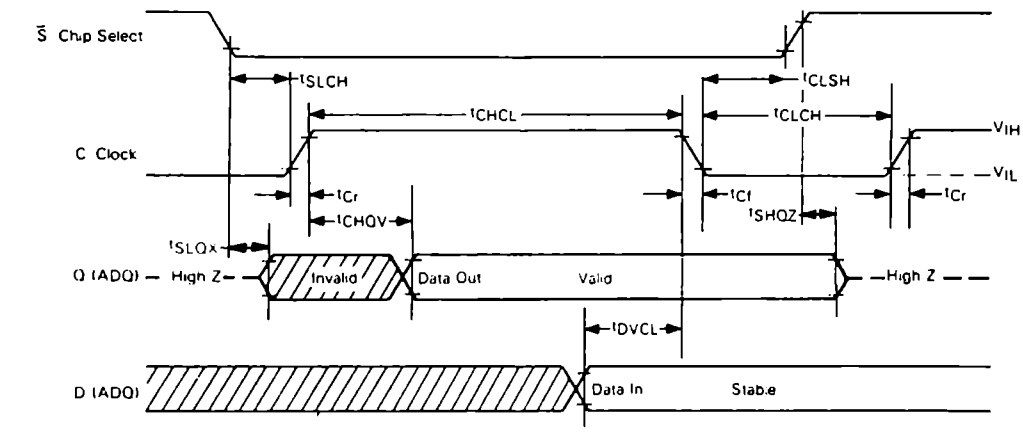
AC OPERATING CONDITIONS AND CHARACTERISTICS

Input Pulse Levels	0.65 Volts and 2.6 Volts	Output Timing Levels	1.0 Volt and 2 Volts
Input Rise and Fall Times	20 ns	Output Load	See Figure 2
Input Timing Levels	1.0 Volt and 3.8 Volts		

Characteristic	Symbol	Min	Max	Unit
Erase Time	t_{ERASE}	100	-	ms
Write Time	t_{WRITE}	10	-	ms
Clock High Level Hold Time	t_{CHCL}	4	10	µs
Clock Low Level Hold Time	t_{CLCH}	4	-	µs
Clock Rise Time	t_{Cr}	5	1000	ns
Clock Fall Time	t_{Cf}	5	1000	ns
Chip Select Setup	t_{SLCH}	1	-	µs
Chip Select Hold	t_{CLSH}	1	-	µs
Data Out Delay	t_{CHQV}	-	1	µs
Address In Setup	t_{AVCL}	1	-	µs
Data In Setup	t_{DVCL}	1	-	µs
Control Setup Time	t_{CtrVCH}	1	-	µs
Control Hold Time	t_{CtrX}	50	-	ns
Data Off Time (from the Clock)	t_{CHQZ}	-	30	µs
Chip Select Low to Output Active Time	t_{SLQX}	-	20	µs
Data Off Time (from Chip Select)	t_{SHQZ}	-	20	µs

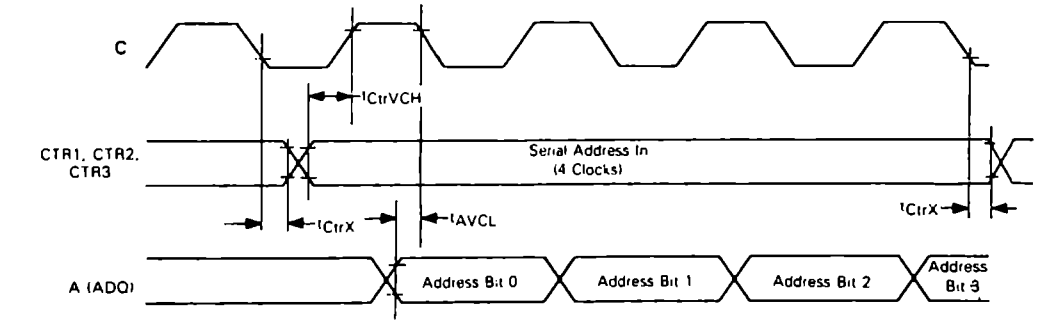
TIMING DIAGRAMS

Clock Cycle Detail

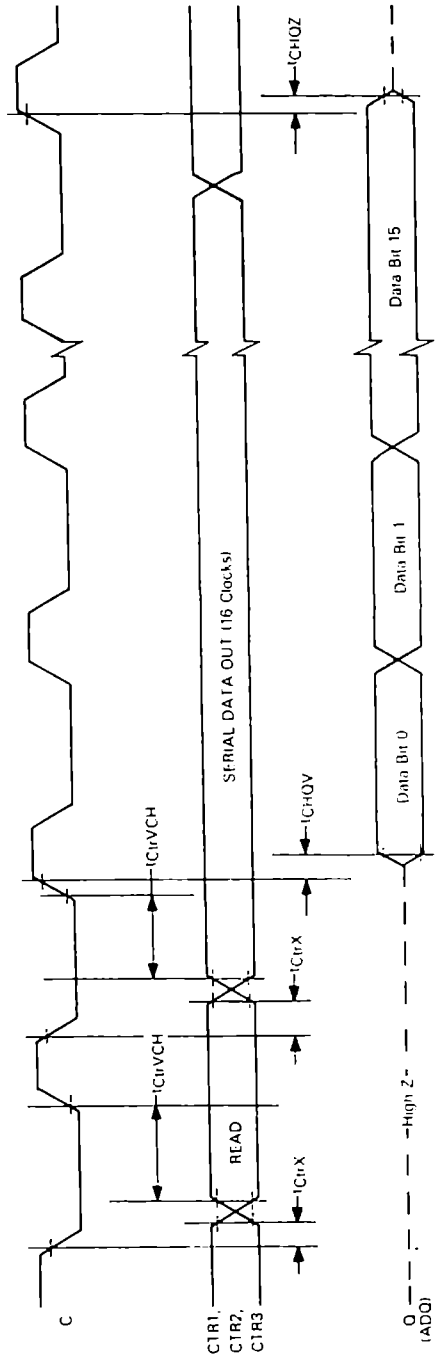


All times defined at 10% or 90% points

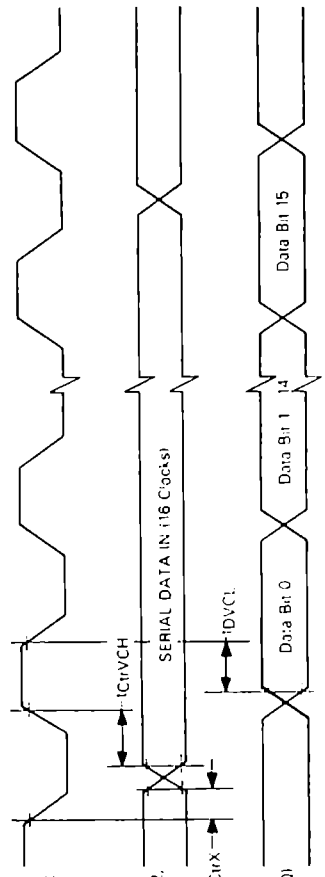
Serial Address In



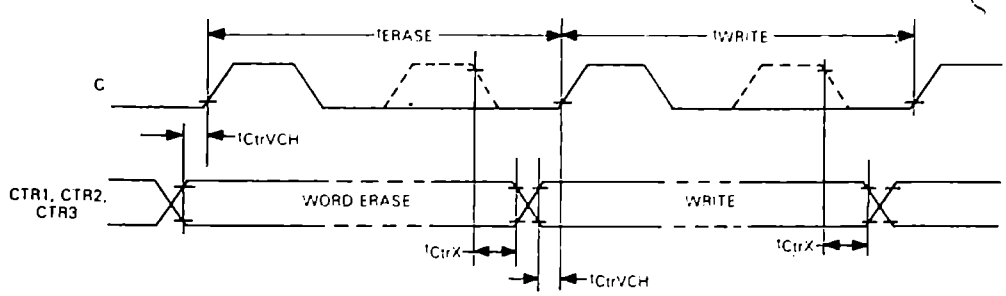
READ AND SERIAL DATA OUT



SERIAL DATA IN



ERASE-WRITE SEQUENCE



NOTE: One clock pulse is sufficient to load a new control code

FUNCTIONAL DESCRIPTION

The memory stores sixteen words, each of sixteen bits. All functions are selected by a 3-bit parallel control code. The clock line is used to strobe these codes and to serially shift data and addresses.

Read-Out

1. The 4-bit serial address is shifted on the ADQ line while the SERIAL ADDRESS-IN code is applied on the three control pins.
2. The READ instruction is strobed with one clock pulse. This reads the word from the new address in the memory array and parallel loads it into the data register.
3. While the SERIAL DATA-OUT code is being applied, data is shifted out on the ADQ pin with 16 clock pulses. In this mode, the ADQ pin output buffer is active.

Writing

1. The address is changed, if necessary, in the same manner as in the readout.
2. While the SERIAL DATA-IN code is being applied, data is shifted in on the ADQ pin with 16 clock pulses. If the data to be written has already been shifted into the data register, it is not necessary to re-enter the 16 bits, so this step may be omitted.
3. The WORD ERASE code is strobed in with one clock pulse. After the specified ERASE time, the addressed word is erased.
4. The WRITE code is strobed in with one clock pulse. After the specified WRITE time, a STANDBY code can be strobed in to stop writing. Data will be programmed at the specified address.

   It is also possible to change the sequence by erasing a memory location before starting a write sequence.

Standby

Either of the two STANDBY codes, when strobed in with a clock pulse, puts the memory in a quiescent state. The output is then in the high-impedance state and the absence or presence of the clock will not affect the device.

Pin Description

The active high clock signal (C) is used for shifting addresses and data into or out of the chip. It is also used for strobing control codes.

The I/O pin (ADQ) is used for entering addresses and data in. It is in the output state only for shifting output data.

The active low Chip Select pin ($\overline{S}$) is only used to block the clock and put the ADQ buffer into the high-impedance mode. It has no influence on the operating status of the device and does not force a standby condition.

The programming voltage control pin (PVC) is an open-drain output that is active when a WORD ERASE or WRITE control code is strobed in. As shown in Figure 1, it can be used to control the V_{PP} supply applied to the circuit. The BLOCK ERASE (BE) pin can be used to clear the whole array. As the PVC output is not active in this state, the programming voltage should be directly applied to the V_{PP} pin for the specified erase time.

The Test inputs (TEST1 and TEST2) are provided for testing purpose only and should be connected to V_{SS} in any application.

Data Protection

When V_{PP} is turned off, data stored in the array is protected. The programming voltage should not be applied to the V_{PP} pin if V_{CC} is not present. Therefore, use of the PVC control output, which is controlled by the V_{CC} supply is recommended. Using this feature, V_{PP} and V_{CC} can be turned on or off in any sequence without disturbing data in the array. However, to avoid spurious control codes being strobed into the device, all inputs should be stable when V_{PP} is on.

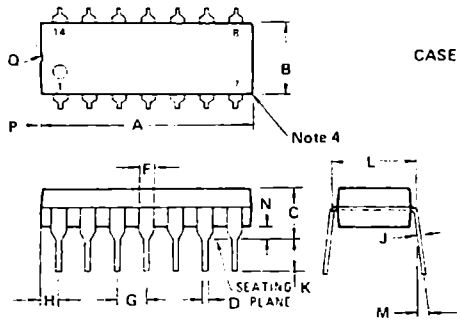
General Comments

The erased state corresponds to a logical zero at the ADQ output.

WRITE (for any address) must be preceded by an ERASE at the same address.

V_{PP} is necessary for WRITE, WORD ERASE or BLOCK ERASE. In all other cases, it can be switched to high impedance, V_{CC} or V_{SS}.

OUTLINE DIMENSIONS



CASE 646-05

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	18.16	19.56	0.715	0.770
B	6.10	6.60	0.240	0.260
C	4.06	5.08	0.160	0.200
D	0.38	0.53	0.015	0.021
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	1.32	2.41	0.052	0.095
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	10°	0°	10°
N	0.51	1.07	0.020	0.040

NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
4. ROUNDED CORNERS OPTIONAL.

MOTOROLA

MCM2816

Product Preview

2048 × 8-BIT ELECTRICALLY ERASABLE PROM

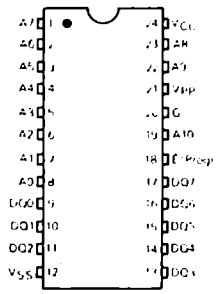
The MCM2816 is a 16,384-bit Electrically Erasable Programmable Read Only Memory designed for handling data in applications requiring both nonvolatile memory and in-system reprogramming. The industry standard pinout in a 24-pin dual-in-line package makes the MCM2816 EEPROM compatible with the popular MCM2716 EPROM.

The MCM2816 saves time and money because of the in-system erase and reprogram capability. While V_{PP} is at 25 V and $\overline{G}$ is at V_{IL}, a 100 ms active high TTL erase pulse applied to the $\overline{E}$/Progr pin allows the entire memory to be erased to the "1" state. In addition to in-system programmability, this new-generation PROM is programmable on the standard EPROM programmer.

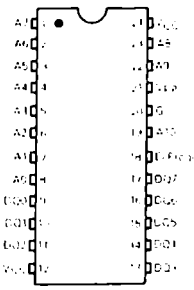
For ease of use, the device operates in the read mode from a single power supply and has a static power-down mode. The MCM2816 is fabricated in floating gate technology for high reliability and producibility.

- Single +5 V Power Supply
- Automatic Power-Down Mode (Standby)
- Single +25 V Power Supply for Erase and Program
- Organized as 2048 Bytes of 8 Bits
- TTL Compatible During Read and Program (No High Voltage Pulses)
- Maximum Access Time = 450 ns MCM2816
  350 ns MCM2816-35
- Pin Compatible to MCM68316E and MCM2716
- In-System Program/Erase Capability

PINOUT COMPARISON 2816 AND 2716



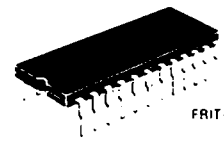
MCM2816



MCM2716

MOS
(N-CHANNEL, SILICON GATE)

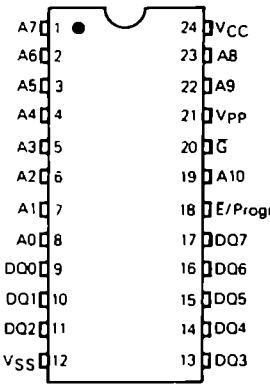
2048 × 8-BIT ELECTRICALLY ERASABLE PROGRAMMABLE READ ONLY MEMORY



C SUFFIX
FRIT-SEAL CERAMIC PACKAGE
CASE 623-04

L SUFFIX CERAMIC PACKAGE
ALSO AVAILABLE — CASE 716-07

PIN ASSIGNMENT



*Pin Names	
A	Address
DO	Data Input/Output
$\overline{E}$/Progr	Chip Enable/Program-Erase
$\overline{G}$	Output Enable

*New industry standard nomenclature

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NP332/11-80

MOTOROLA

MCM6670
MCM6674

MOS

(N-CHANNEL, SILICON GATE)

128c x 7 x 5 HORIZONTAL-SCAN CHARACTER GENERATOR

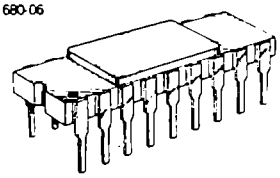
128c X 7 X 5 CHARACTER GENERATOR

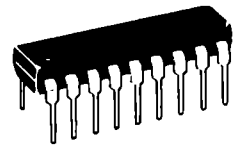
The MCM6670 is a mask-programmable horizontal-scan (row select) character generator containing 128 characters in a 5 X 7 matrix. A 7-bit address code is used to select one of the 128 available characters, and a 3-bit row select code chooses the appropriate row to appear at the outputs. The rows are sequentially displayed, providing a 7-word sequence of 5 parallel bits per word for each character selected by the address inputs.

The MCM6674 is a preprogrammed version of the MCM6670. The complete pattern of this device is contained in this data sheet.

- Fully Static Operation
- TTL Compatibility
- Single ±10% +5 Volt Power Supply
- 18-Pin Package
- Diagonal Corner Power Supply Pins
- Fast Access Time, 350 ns (max)

L SUFFIX
CERAMIC PACKAGE
CASE 680-06





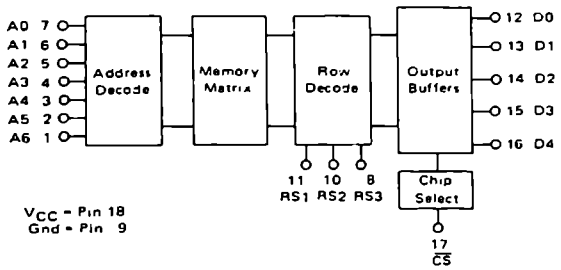
P SUFFIX
PLASTIC PACKAGE
CASE 707-02

ABSOLUTE MAXIMUM RATINGS (See Note 1)

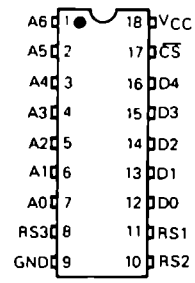
Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3 to +7.0	Vdc
Input Voltage	V_{in}	-0.3 to +7.0	Vdc
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

NOTE 1 Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

BLOCK DIAGRAM



PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

DS9459/12-77

DC OPERATING CONDITIONS AND CHARACTERISITCS

(Full operating voltage and temperature range unless otherwise noted.)

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Symbol	Min	Nom	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	Vdc
Input High Voltage	V_{IH}	2.0		5.5	Vdc
Input Low Voltage	V_{IL}	-0.3		0.8	Vdc

DC CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
Input Current (V_{in} = 0 to 5.5 V)	I_{in}			2.5	μAdc
Output High Voltage (I_{OH} = -205 μA)	V_{OH}	2.4	–	V_{CC}	Vdc
Output Low Voltage (I_{OL} = 1.6 mA)	V_{OL}		–	0.4	Vdc
Output Leakage Current (Three-State) ($\overline{CS}$ = 2.0 V or $\overline{CS}$ = 0.8 V, V_{out} = 0.4 V to 2.4 V)	I_{LO}	–	–	10	μAdc
Supply Current (V_{CC} = 5.5 V, T_A = 0°C)	I_{CC}	–	–	130	mAdc

CAPACITANCE (T_A = 25°C, f = 1.0 MHz)

Characteristic	Symbol	Typ	Unit
Input Capacitance	C_{in}	5.0	pF
Output Capacitance	C_{out}	5.0	pF

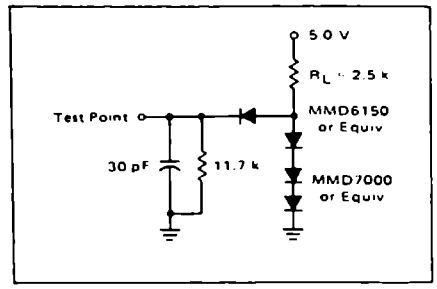
AC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted.)

AC TEST CONDITIONS

Condition	Value
Input Pulse Levels	0.8 V to 2.0 V
Input Rise and Fall Times	20 ns
Output Load	1 TTL Gate and C_L = 30 pF

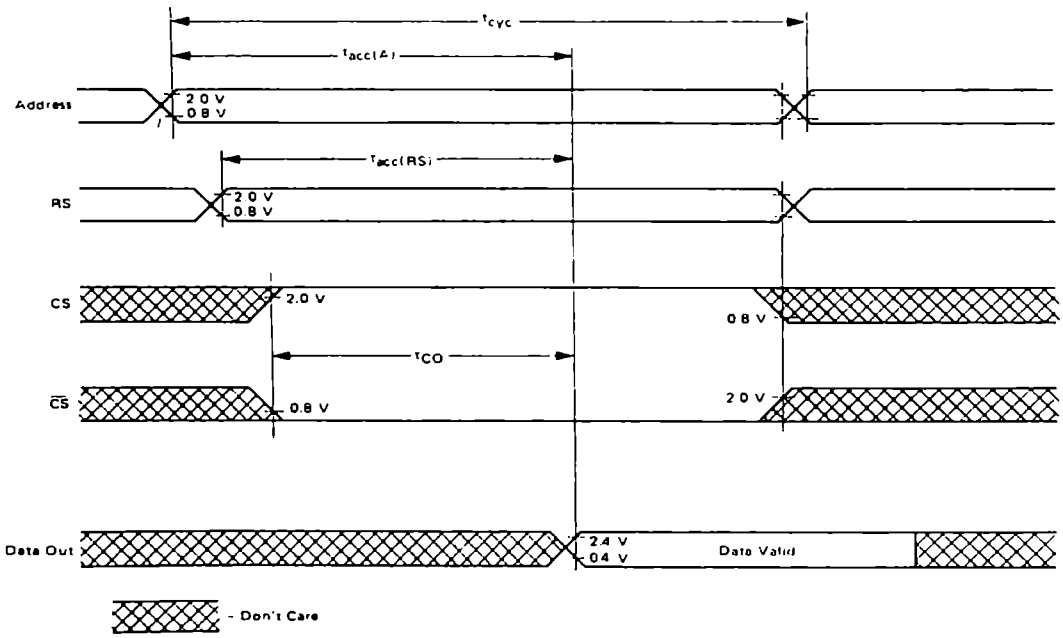
AC TEST LOAD



AC CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit
Cycle Time	t_{cyc}	350	–	ns
Address Access Time	$t_{acc(A)}$	–	350	ns
Row Select Access Time	$t_{acc(RS)}$	–	350	ns
Chip Select to Output Delay	t_{CO}	–	150	ns

TIMING DIAGRAM



CUSTOM PROGRAMMING FOR MCM6670

By the programming of a single photomask, the customer may specify the content of the MCM6670. Encoding of the photomask is done with the aid of a computer to provide quick, efficient implementation of the custom bit pattern while reducing the cost of implementation.

Information for the custom memory content may be sent to Motorola in the following forms, in order of preference:

1. Hexadecimal coding using IBM Punch Cards (Figures 3 and 4).
2. Hexadecimal coding using ASCII Paper Tape Punch (Figure 5).

Programming of the MCM6670 can be achieved by using the following sequence.

1. Create the 128 characters in a 5 x 7 font using the format shown in Figure 1. Note that information at output D4 appears in column one, D3 in column two, thru D0 information in column five. The dots filled in and programmed as a logic "1" will appear at the outputs as V_{OH}, the dots left blank will be at V_{OL}. R0 is always programmed to be blank (V_{OL}). (Blank formats appear at the end of this data sheet for your convenience, they are not to be submitted to Motorola, however.)

2. Convert the characters to hexadecimal coding treating dots as ones and blanks as zeros, and enter this information in the blocks to the right of the character font format. The information for D4 must be a hex one or zero, and is entered in the left block. The information for D3 thru D0 is entered in the right block, with D3 the most significant bit for the hex coding, and D0 the least significant.

3. Transfer the hexadecimal figures either to punched cards (Figure 3) or to paper tape (Figure 5).

4. Transmit this data to Motorola, along with the customer name, customer part number and revision, and an indication that the source device is the MCM6670.

5. Information should be submitted on an organizational data form such as that shown in Figure 2.

FIGURE 1 – CHARACTER FORMAT

ROW SELECT TRUTH TABLE

RS3	RS2	RS1	OUTPUT
0	0	0	R0
0	0	1	R1
0	1	0	R2
0	1	1	R3
1	0	0	R4
1	0	1	R5
1	1	0	R6
1	1	1	R7

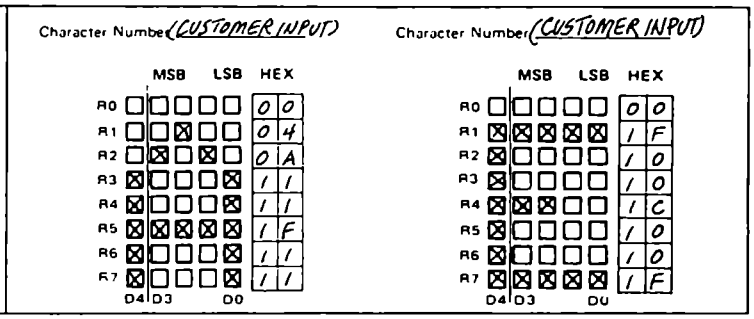


FIGURE 2 – FORMAT FOR PROGRAMMING GENERAL OPTIONS

ORGANIZATIONAL DATA
MCM6670 MOS READ ONLY MEMORY

Customer:

Company _____

Part No. _____

Originator _____

Phone No. _____

Motorola Use Only.

Quote _____

Part No. _____

Specif. No. _____

Chip-Select Options.

	Active High 1	Active Low 0	No-Connect
CS	☐	☐	☐

FIGURE 3 – CARD PUNCH FORMAT

Columns	
1-9	Blank
10-25	Hex coding for first character
26	Slash (/)
27-42	Hex coding for second character
43	Slash (/)
44-59	Hex coding for third character
60	Slash (/)
61-76	Hex coding for fourth character
77-78	Blank
79-80	Card number (starting 01, thru 32)

Column 10 on the first card contains either a zero or a one to program D4 of row R0 for the first character. Column 11 contains the hex character for D3 thru D0. Columns 12 and 13 contain the information to program R1. The entire first character is coded in columns 10 thru 25. Each card contains the coding for four characters; 32 cards are required to program the entire 128 characters. The characters must be programmed in sequence from the first character to the last in order to establish proper addressing for the part. Figure 3 provides an illustration of the correct format

FIGURE 4 – EXAMPLE OF CARD PUNCH FORMAT
(First 12 Characters of MCM6670P4)

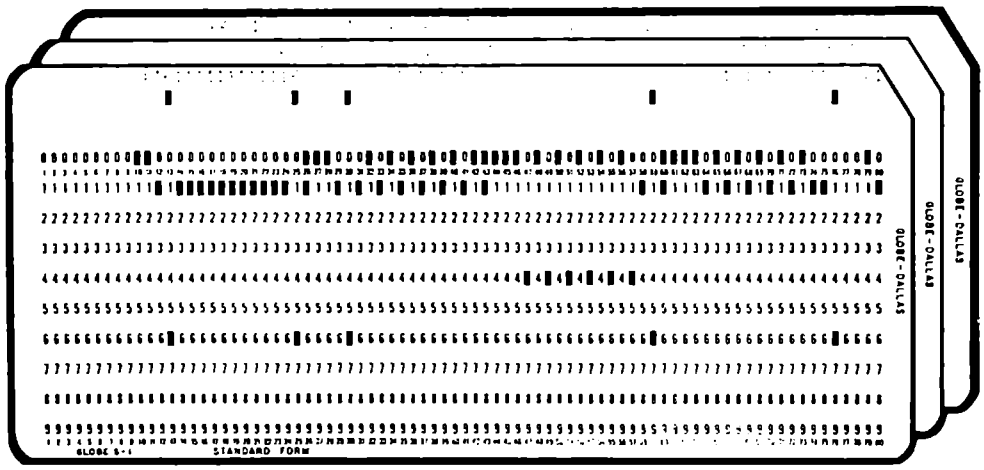


FIGURE 5 – PAPER TAPE FORMAT

Frames	
Leader	Blank Tape
1 to M	Allowed for customer use (M ⩽ 64)
M + 1, M + 2	CR; LF (Carriage Return, Line Feed)
M + 3 to M + 66	First line of pattern information (64 hex figures per line)
M + 67, M + 68	CR; LF
M + 69 to M + 2114	Remaining 31 lines of hex figures, each line followed by a Carriage Return and Line Feed

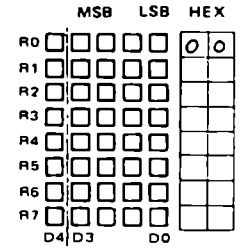
Blank Tape

Frames 1 to M are left to the customer for internal identification, where M ⩽ 64. Any combination of alphanumerics may be used. This information is terminated with a Carriage Return and Line Feed, delineating the start of data entry. (Note that the tape cannot begin with a CR and/or LF, or the customer identification will be assumed to be programming data.)

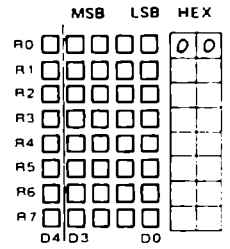
Frame M + 3 contains a zero or a one to program D4 of row R0 for the first character. Frame M + 4 contains the hex character for D3 thru D0, completing the programming information for R0. Frames M + 5 and M + 6 contain the information to program R1. The entire first character is coded in Frames M + 3 thru M + 18. Four complete characters are programmed with each line. A total of 32 lines program all 128 characters (32 x 4). The characters must be programmed in sequence from the first character to the last in order to establish proper addressing for the part.

The formats below are given for your convenience in preparing character information for MCM6670 programming. THESE FORMATS ARE NOT TO BE USED TO TRANSMIT THE INFORMATION TO MOTOROLA. Refer to the Custom Programming Instructions for detailed procedures.

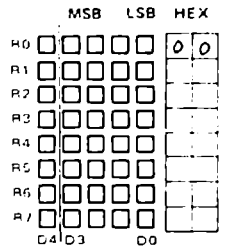
Character Number _____



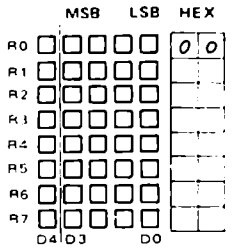
Character Number _____



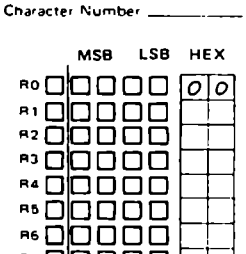
Character Number _____



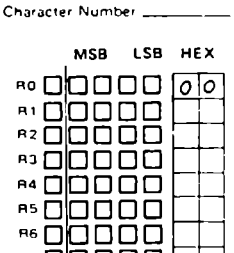
Character Number _____



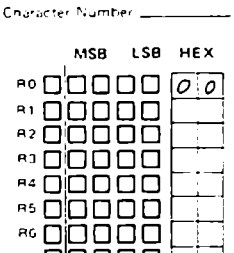
Character Number _____



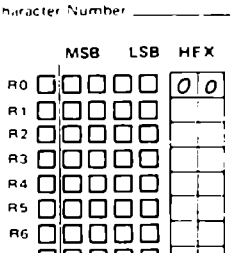
Character Number _____



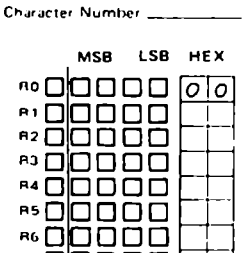
Character Number _____



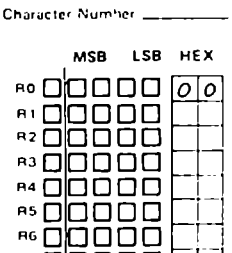
Character Number _____



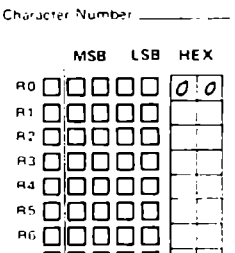
Character Number _____



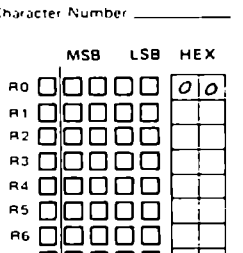
Character Number _____



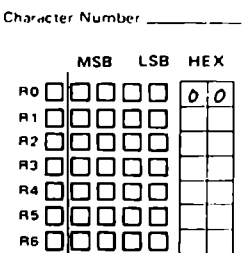
Character Number _____



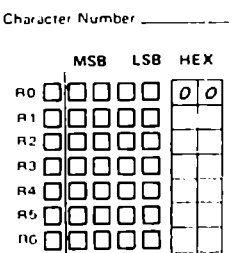
Character Number _____



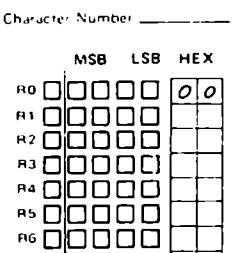
Character Number _____



Character Number _____



Character Number _____



Character Number _____

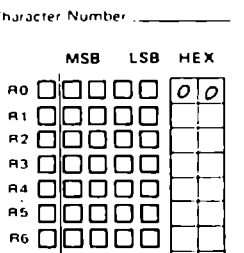
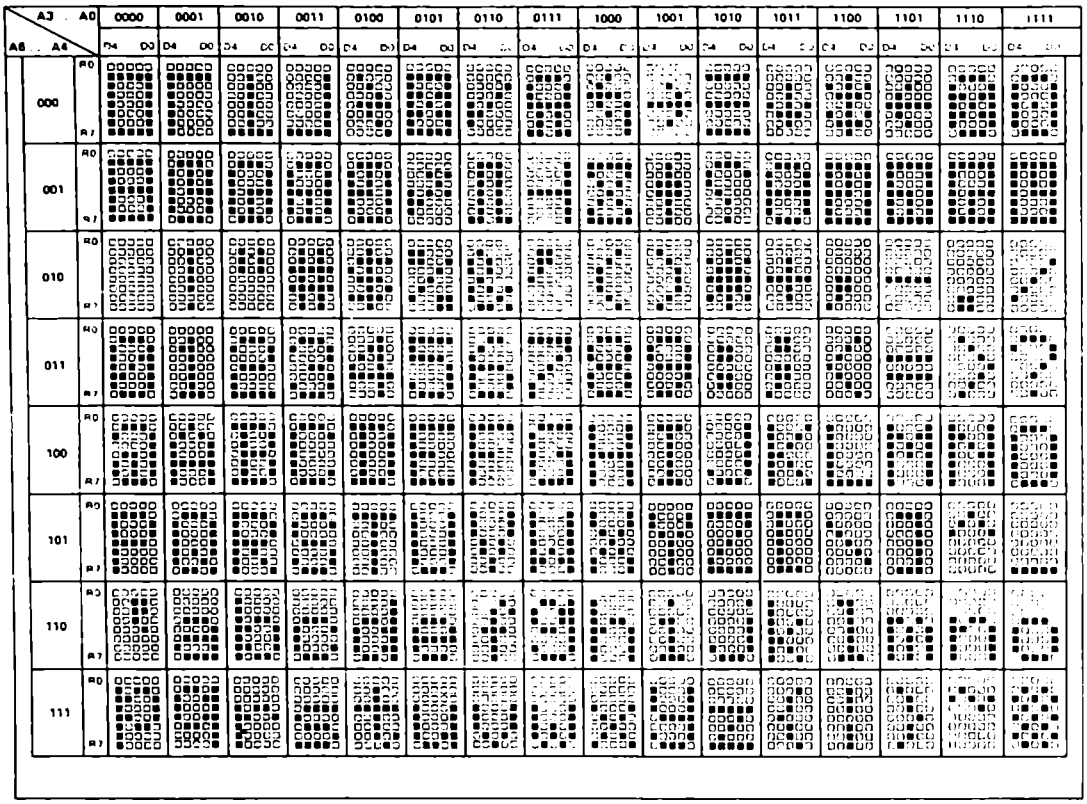


FIGURE 6 – MCM6674 PATTERN



MOTOROLA

MCM66700 MCM66710 MCM66714 MCM66720 MCM66730 MCM66734 MCM66740 MCM66750 MCM66751 MCM66760 MCM66770 MCM66780 MCM66790

8192-BIT READ ONLY MEMORIES
ROW SELECT CHARACTER GENERATORS

The MCM66700 is a mask-programmable 8192-bit horizontal scan (row select) character generator. It contains 128 characters in a 7 X 9 matrix, and has the capability of shifting certain characters that normally extend below the baseline such as j, y, g, p, and q. Circuitry is supplied internally to effectively lower the whole matrix for this type of character—a feature previously requiring external circuitry.

A seven-bit address code is used to select one of the 128 available characters. Each character is defined as a specific combination of logic 1s and 0s stored in a 7 X 9 matrix. When a specific four-bit binary row select code is applied, a word of seven parallel bits appears at the output. The rows can be sequentially selected, providing a nine-word sequence of seven parallel bits per word for each character selected by the address inputs. As the row select inputs are sequentially addressed, the devices will automatically place the 7 X 9 character in one of two preprogrammed positions on the 16-row matrix, with the positions defined by the four row select inputs. Rows that are not part of the character are automatically blanked.

The devices listed are preprogrammed versions of the MCM66700. They contain various sets of characters to meet the requirements of diverse applications. The complete patterns of these devices are contained in this data sheet.

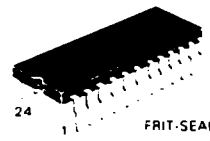
- Fully Static Operation
- Fully TTL Compatible with Three-State Outputs
- CMOS and MPU Compatible, Single ± 10% 5 Volt Supply
- Shifted Character Capability
  (Except MCM66720, MCM66730, and MCM66734)
- Maximum Access Time = 350 ns
- 4 Programmable Chip Selects (0, 1, or X)
- Pin-for-Pin Replacement for the MCM6570, Including All Standard Patterns

MOS

(N-CHANNEL, SILICON-GATE)

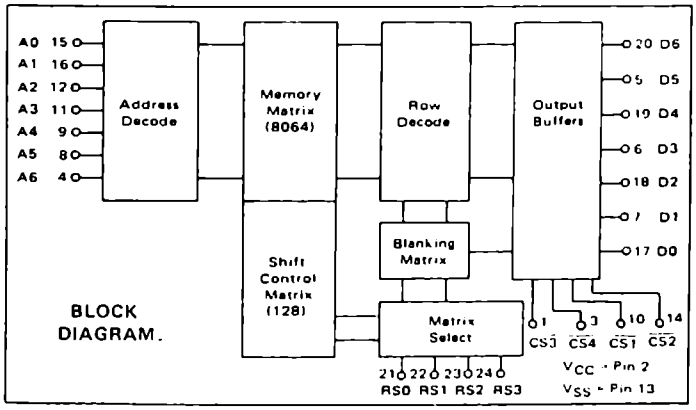
8K READ ONLY MEMORIES

HORIZONTAL-SCAN CHARACTER GENERATORS WITH SHIFTED CHARACTERS



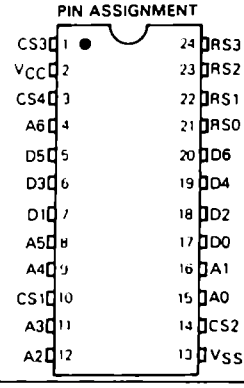
C SUFFIX
FRIT-SEAL CERAMIC PACKAGE
CASE 623-04

P SUFFIX
PLASTIC PACKAGE
CASE 709-02



BLOCK DIAGRAM.

PIN ASSIGNMENT



DS9516/8-78

ABSOLUTE MAXIMUM RATINGS (See Note 1, Voltages Referenced to V_{SS})

Rating	Symbol	Value	Unit
Supply Voltages	V_{CC}	-0.3 to 7.0	Vdc
Input Voltage	V_{in}	-0.3 to 7.0	Vdc
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-55 to +125	°C

NOTE 1: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher-than-recommended voltages for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted)

RECOMMENDED DC OPERATING CONDITIONS (Referenced to V_{SS})

Parameter	Symbol	Min	Nom	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	Vdc
Input Logic "1" Voltage	V_{IH}	2.0	–	V_{CC}	Vdc
Input Logic "0" Voltage	V_{IL}	-0.3	–	0.8	Vdc

DC CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
Input Leakage Current (V_{IH} = 5.5 Vdc, V_{CC} = 4.5 Vdc)	I_{IH}	–	–	2.5	μAdc
Output Low Voltage (Blank) (I_{OL} = 1.6 mAdc)	V_{OL}	0	–	0.4	Vdc
Output High Voltage (Dot) (I_{OH} = -205 μAdc)	V_{OH}	2.4	–	–	Vdc
Power Supply Current	I_{CC}	–	–	80	mAdc
Power Dissipation	P_D	–	200	440	mW

CAPACITANCE (Periodically sampled rather than 100% tested)

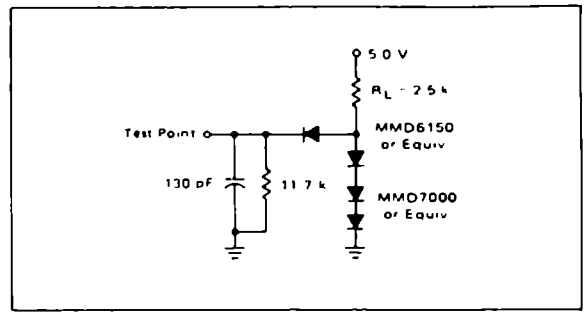
Input Capacitance (f = 1.0 MHz)	C_{in}	–	4.0	7.0	pF
Output Capacitance (f = 1.0 MHz)	C_{out}	–	4.0	7.0	pF

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

AC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted)

AC TEST LOAD



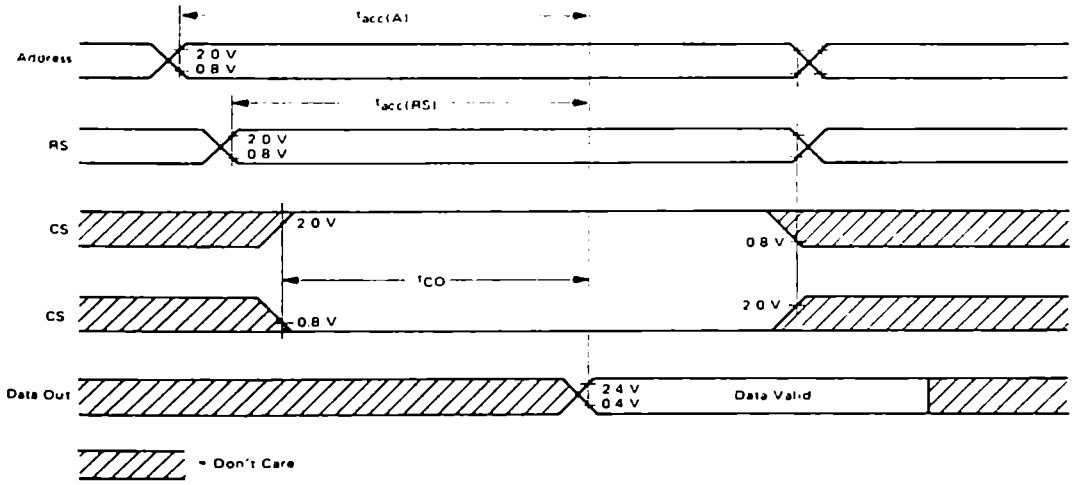
AC TEST CONDITIONS

Condition	Value
Input Pulse Levels	0.8 V to 2.0 V
Input Rise and Fall Times	20 ns
Output Load	1 TTL Gate and C_L = 130 pF

AC CHARACTERISTICS

Characteristic	Symbol	Typ	Max	Unit
Address Access Time	$t_{acc(A)}$	250	350	ns
Row Select Access Time	$t_{acc(RS)}$	250	350	ns
Chip Select to Output Delay	t_{CO}	100	150	ns

TIMING DIAGRAM



MEMORY OPERATION (Using Positive Logic)

Most positive level = 1, most negative level = 0.

Address

To select one of the 128 characters, apply the appropriate binary code to the Address inputs (A0 through A6).

Row Select

To select one of the rows of the addressed character to appear at the seven output lines, apply the appropriate binary code to the Row Select inputs (RS0 through RS3).

Shifted Characters

These devices have the capability of displaying characters that descend below the bottom line (such as lowercase letters j, y, g, p, and q). Internal circuitry effectively drops the whole matrix for this type of character. Any character can be programmed to occupy either of the two positions in a 7 X 16 matrix. (Shifted characters are not available on MCM66720, MCM66730, or MCM66734.)

Output

For these devices, an output dot is defined as a logic 1 level, and an output blank is defined as a logic 0 level.

Programmable Chip Select

The MCM66700 has four Chip Select inputs that can be programmed with a 1, 0, or don't care (not connected). A don't care must always be the highest chip select pin or pins. All standard patterns have Don't Care Chip Select—except MCM66751.

DISPLAY FORMAT

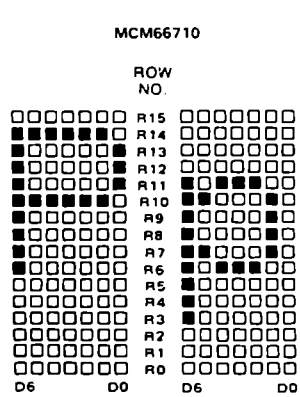
Figure 1 shows the relationship between the logic levels at the row select inputs and the character row at the outputs. The MCM66700 allows the user to locate the basic 7 X 9 font anywhere in the 7 X 16 array. In addition, a shifted font can be placed anywhere in the same 7 X 16 array. For example, the basic MCM66710 font is established in rows R14 through R6. All other rows are automatically blanked. The shifted font is established in rows R11 through R3, with all other rows blanked. Thus, while any one character is contained in a 7 X 9 array, the MCM66710 requires a 7 X 12 array on the CRT screen to contain both normal and descending characters. Other uses of the shift option may require as much as the full 7 X 16 array, or as little as the basic 7 X 9 array (when no shifting occurs, as in the MCM66720).

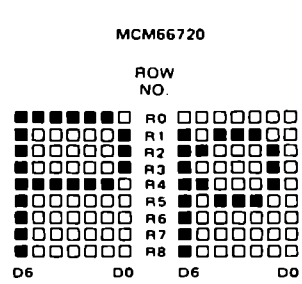
The MCM66700 can be programmed to be scanned either from bottom to top or from top to bottom. This is achieved through the option of assigning row numbers in ascending or descending count, as long as both the basic font and the shifted font are the same. For example, an up counter will scan the MCM66710 from bottom to top, whereas an up counter will scan the MCM66714 from top to bottom (see Figures 7 and 8 for row designation).

FIGURE 1 – ROW SELECT INPUT CODE AND SAMPLE CHARACTERS FOR MCM66710 AND MCM66720

ROW SELECT TRUTH TABLE

RS3	RS2	RS1	RS0	OUTPUT
0	0	0	0	R0
0	0	0	1	R1
0	0	1	0	R2
0	0	1	1	R3
0	1	0	0	R4
0	1	0	1	R5
0	1	1	0	R6
0	1	1	1	R7
1	0	0	0	R8
1	0	0	1	R9
1	0	1	0	R10
1	0	1	1	R11
1	1	0	0	R12
1	1	0	1	R13
1	1	1	0	R14
1	1	1	1	R15





CUSTOM PROGRAMMING FOR MCM66700

By the programming of a single photomask, the customer may specify the content of the MCM66700. Encoding of the photomask is done with the aid of a computer to provide quick, efficient implementation of the custom bit pattern while reducing the cost of implementation.

Information for the custom memory content may be sent to Motorola in the following forms, in order of preference:*

1. Hexadecimal coding using IBM Punch Cards (Figures 3 and 4)
2. Hexadecimal coding using ASCII Paper Tape Punch (Figure 5)

Programming of the MCM66700 can be achieved by using the follow sequence:

1. Create the 128 characters in a 7 X 9 font using the format shown in Figure 2. Note that information at output D6 appears in column one, D5 in column two, through D0 information in column seven. The dots filled in and programmed as a logic 1 will appear at the outputs as V_{OH}; the dots left blank will be at V_{OL}. (Blank formats appear at the end of this data sheet for your convenience, they are not to be submitted to Motorola, however.)

2. Indicate which characters are shifted by filling in the extra square (dot) in the top row, at the left (column S).

3 Convert the characters to hexadecimal coding treating dots as 1s and blanks as 0s, and enter this information in the blocks to the right of the character font format. High order bits are at the left, in columns S and D3. For the bottom eight rows, the bit in Column S must be 0, so these locations have been omitted. For the top row, the bit in Column S will be 0 for an unshifted character, and 1 for a shifted character.

4. Transfer the hexadecimal figures either to punched cards (Figure 3) or to paper tape (Figure 5)

5. Assign row numbers to the unshifted font. These must be nine sequential numbers (values 0 through 15) assigned consecutively to the rows. The shifted font is similarly placed in any position in the 16 rows.

6 Provide, in writing, the information indicated in Figure 6 (a copy of Figure 10 may be used for this purpose). Submit this information to Motorola together with the punched cards or paper tape.

FIGURE 2 – CHARACTER FORMAT

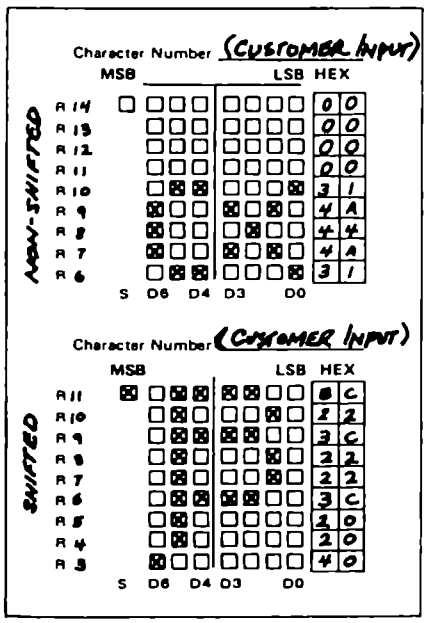


FIGURE 3 – CARD PUNCH FORMAT

Columns	
1 – 10	Blank
11	Asterisk (*)
12 – 29	Hex coding for first character
30	Slash (/)
31 – 48	Hex coding for second character
49	Slash (/)
50 – 67	Hex coding for third character
68	Slash (/)
69 – 76	Blank
77 – 78	Card number (starting 01, through 43)
79 – 80	Blank

Column 12 on the first card contains the hexadecimal equivalent of column S and D6 through D4 for the top row of the first character. Column 13 contains D3 through D0. Columns 14 and 15 contain the information for the next row. The entire first character is coded in columns 12 through 29. Each card contains the coding for three characters. 43 cards are required to program the entire 128 characters, the last card containing only two characters. The characters must be programmed in sequence from the first character to the last in order to establish proper addressing for the part. As an example, the first nine characters of the MCM66710 are correctly coded and punched in Figure 4.

*NOTE: Motorola can accept magnetic tape and truth table formats. For further information contact your local Motorola sales representative.

FIGURE 4 – EXAMPLE OF CARD PUNCH FORMAT
(First 9 Characters of MCM66710)

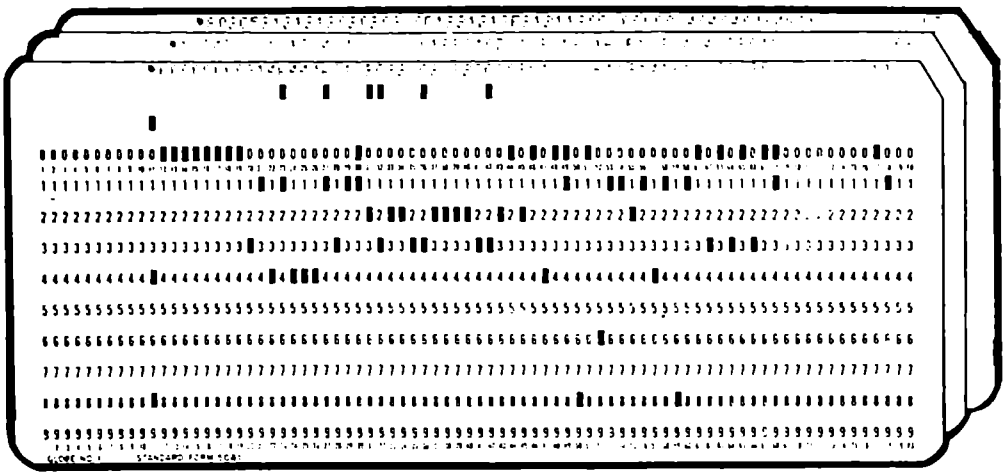


FIGURE 5 – PAPER TAPE FORMAT

Frames	
Leader	Blank Tape
1 to M	Allowed for customer use (M ≤ 64)
M + 1, M + 2	CR; LF (Carriage Return, Line Feed)
M + 3 to M + 66	First line of pattern information (64 hex figures per line)
M + 67, M + 68	CR; LF
M + 69 to M + 2378	Remaining 35 lines of hex figures, each line followed by a Carriage Return and Line Feed

Blank Tape

Frames 1 to M are left to the customer for internal identification, where M ≤ 64. Any combination of alphanumerics may be used. This information is terminated with a Carriage Return and Line Feed, delineating the start of data entry. (Note that the tape cannot begin with a CR and/or LF, or the customer identification will be assumed to be programming data.)

Frame M + 3 contains the hexadecimal equivalent of column S and D6 thru D4 for the top row of the first character. Frame M + 4 contains D3 thru D0. Frames M + 5 and M + 6 program the second row of the first character. Frames M + 3 to M + 66 comprise the first line of the printout. The line is terminated with a CR and LF.

The remaining 35 lines of data are punched in sequence using the same format, each line terminated with a CR and LF. The total 36 lines of data contain 36 x 64 or 2304 hex figures. Since 18 hex figures are required to program each 7 x 9 character, the full 128 (2304 ÷ 18) characters are programmed.

FIGURE 6 – FORMAT FOR ORGANIZATIONAL DATA

ORGANIZATIONAL DATA
MCM66700 MOS READ ONLY MEMORY

Customer _____

Customer Part No. _____ Rev _____

Row Number for top row of non-shifted font _____

Row Number for bottom row of non-shifted font _____

Row Number for top row of shifted font _____

Programmable Chip Select information. 1 = Active High 0 = Active Low X = Don't Care (Not Connected)

CS1 ___ CS2 ___ CS3 ___ CS4 ___

FIGURE 7 – MCM66710 PATTERN

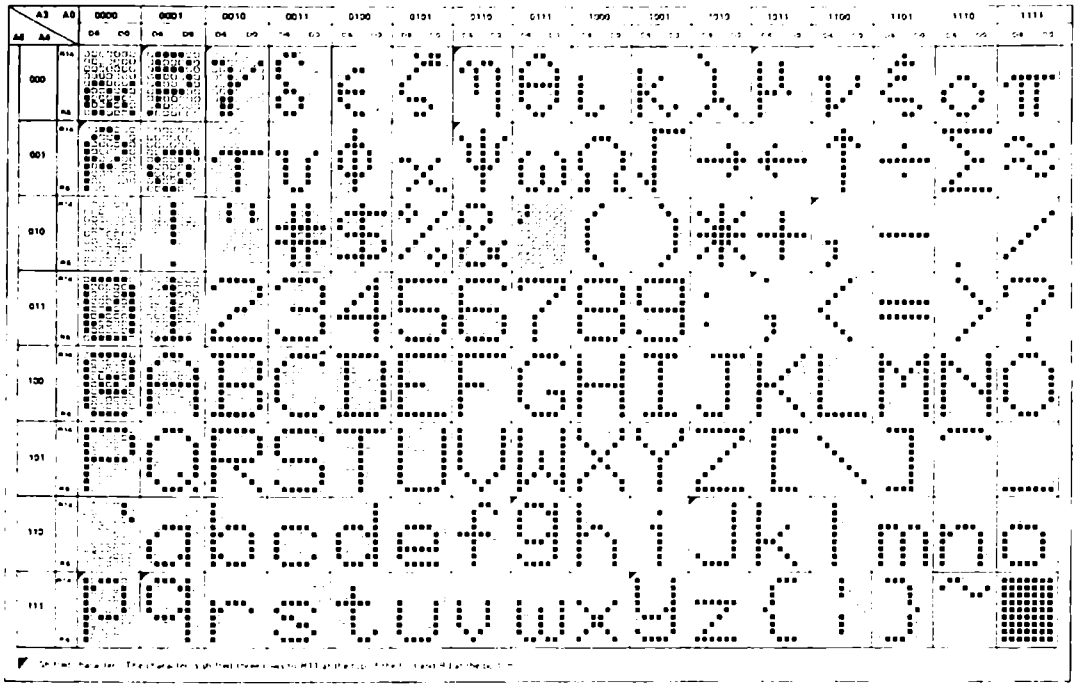


FIGURE 8 – MCM66714 PATTERN

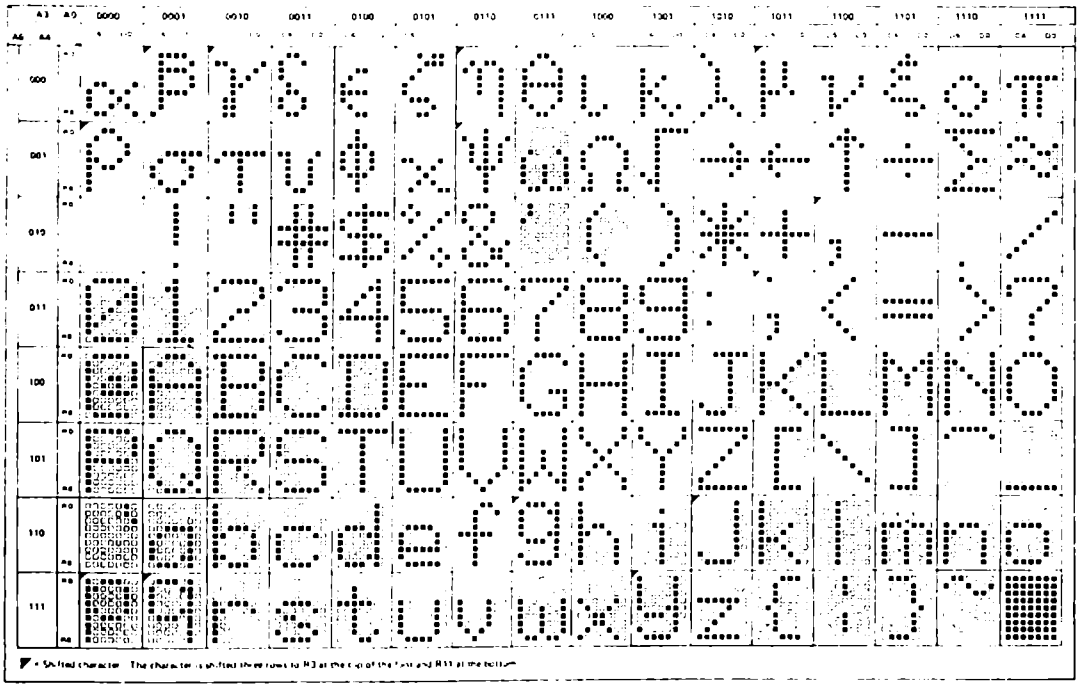
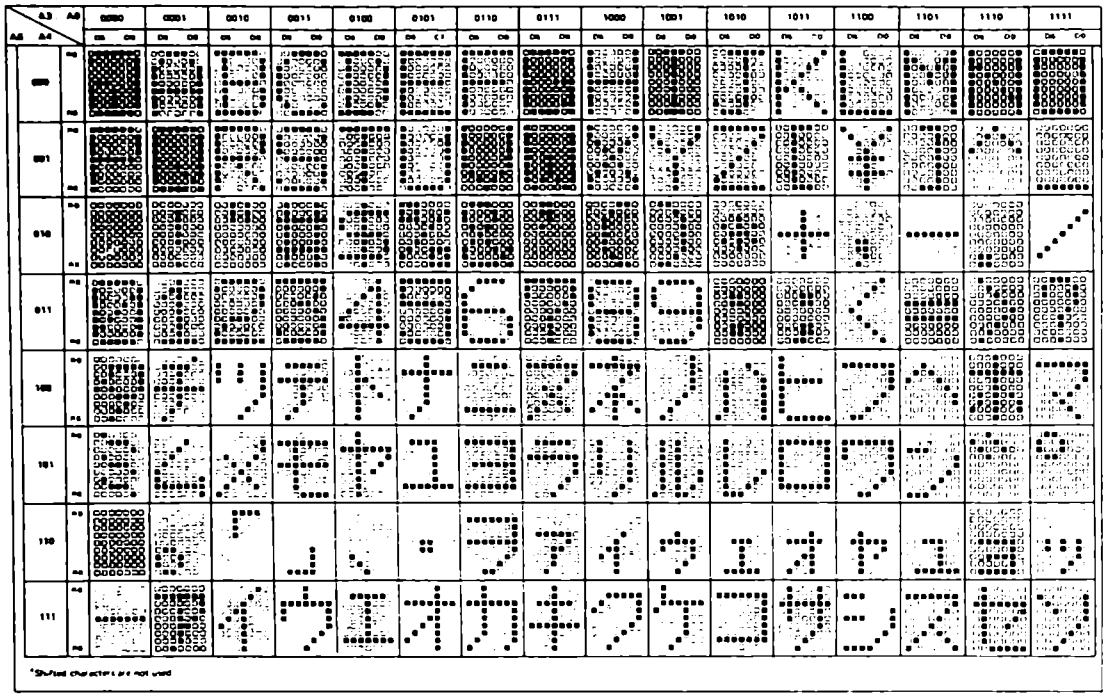
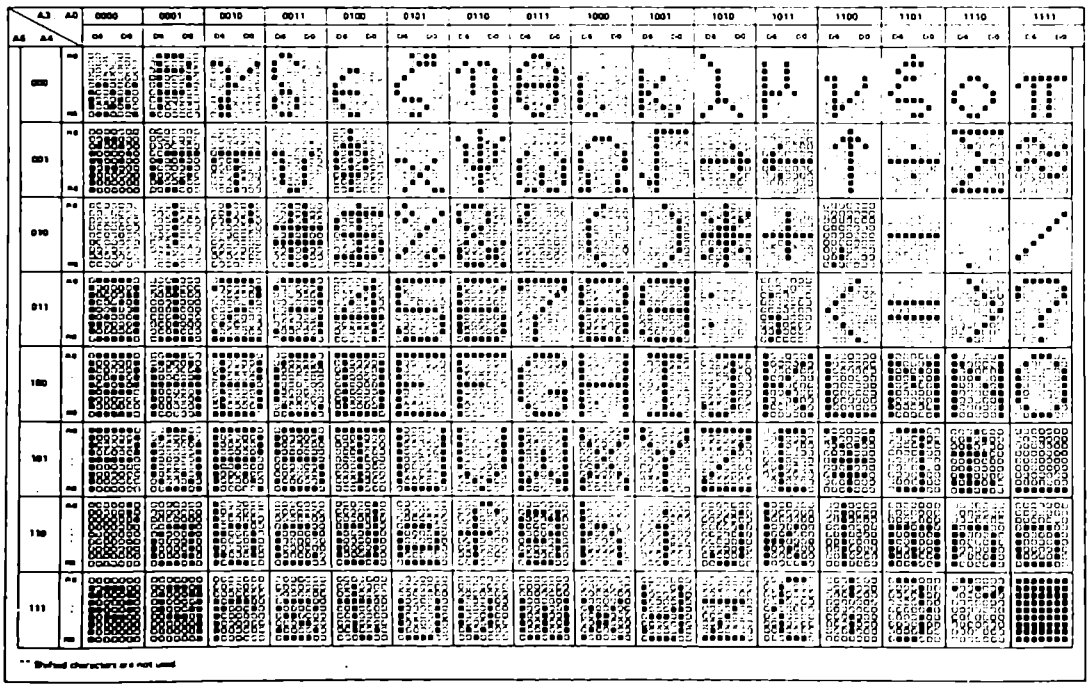


FIGURE 9 – MCM66734 PATTERN*



*Shifted characters are not used

FIGURE 10 – MCM66720 PATTERN**



**Shifted characters are not used

FIGURE 11 – MCM66730 PATTERN**

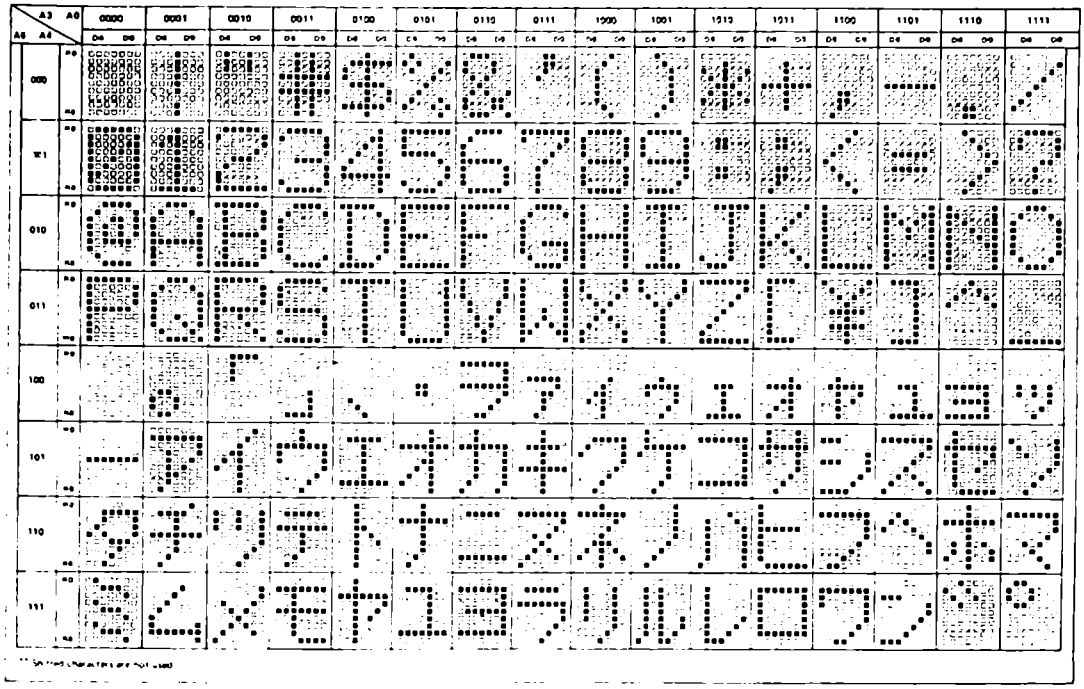


FIGURE 12 – MCM66740 PATTERN

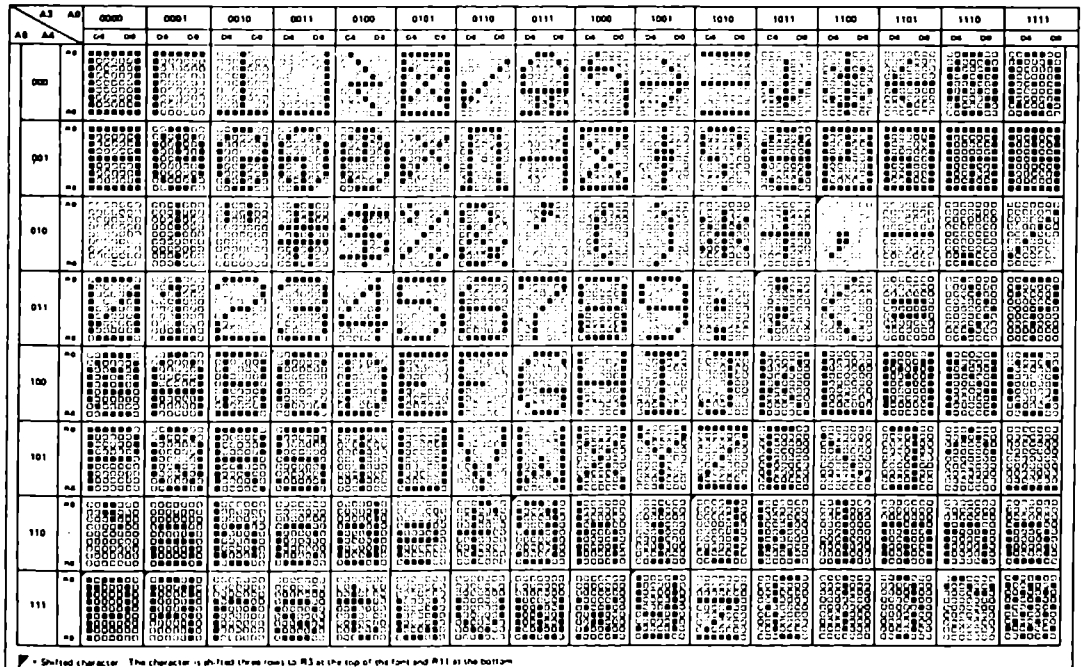
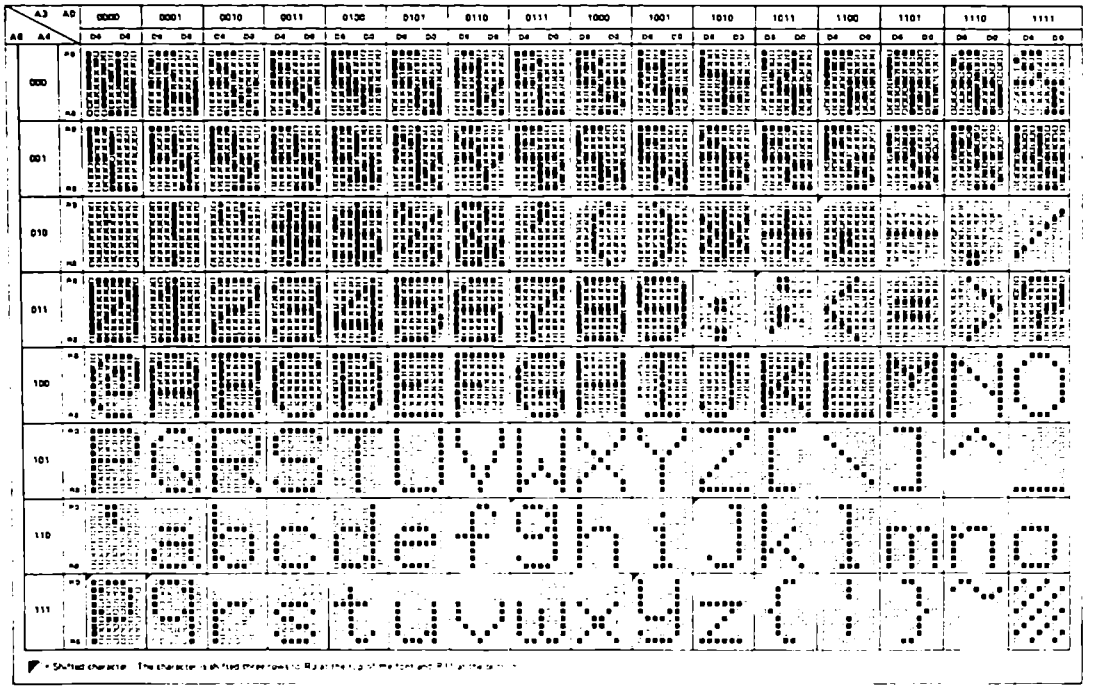


FIGURE 13 – MCM66750 PATTERN



MCM66751 – Same as MCM66750 except CS1 = 0, CS2 = 0, CS3 = X, and CS4 = X.

FIGURE 14 – MCM66760 PATTERN

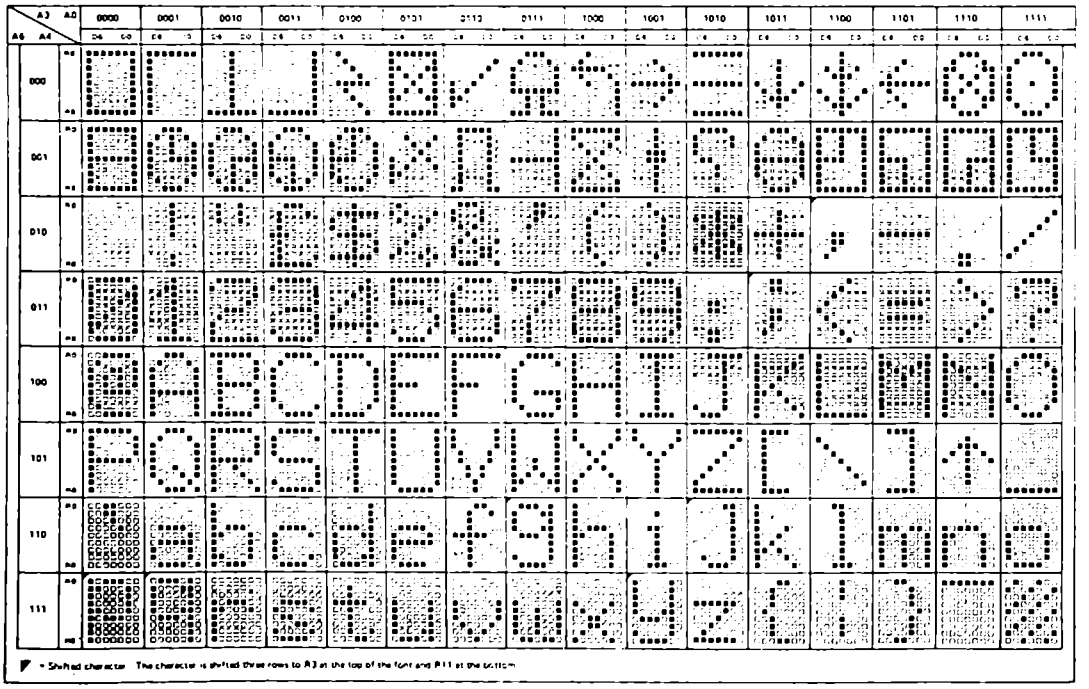


FIGURE 15 – MCM66770 PATTERN

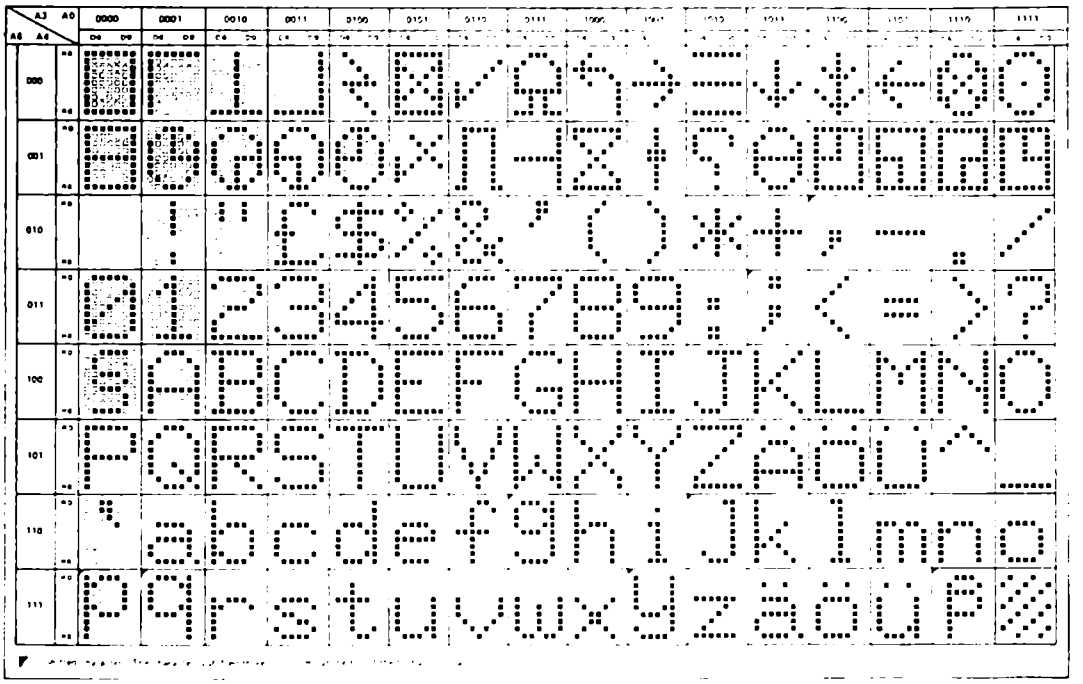


FIGURE 16 – MCM66780 PATTERN

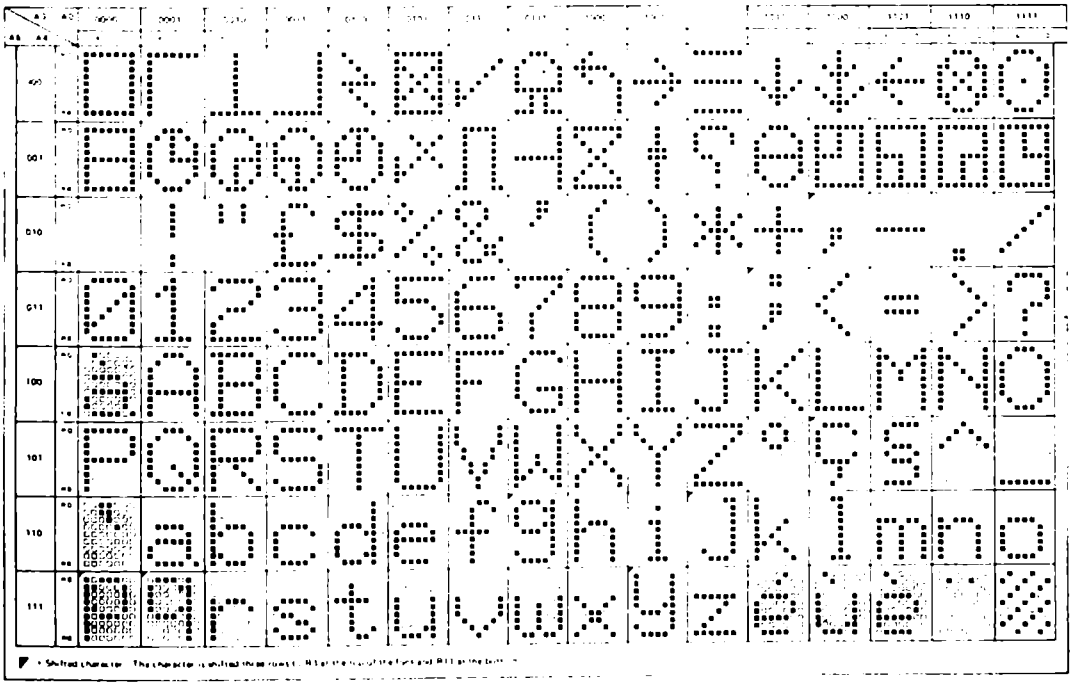
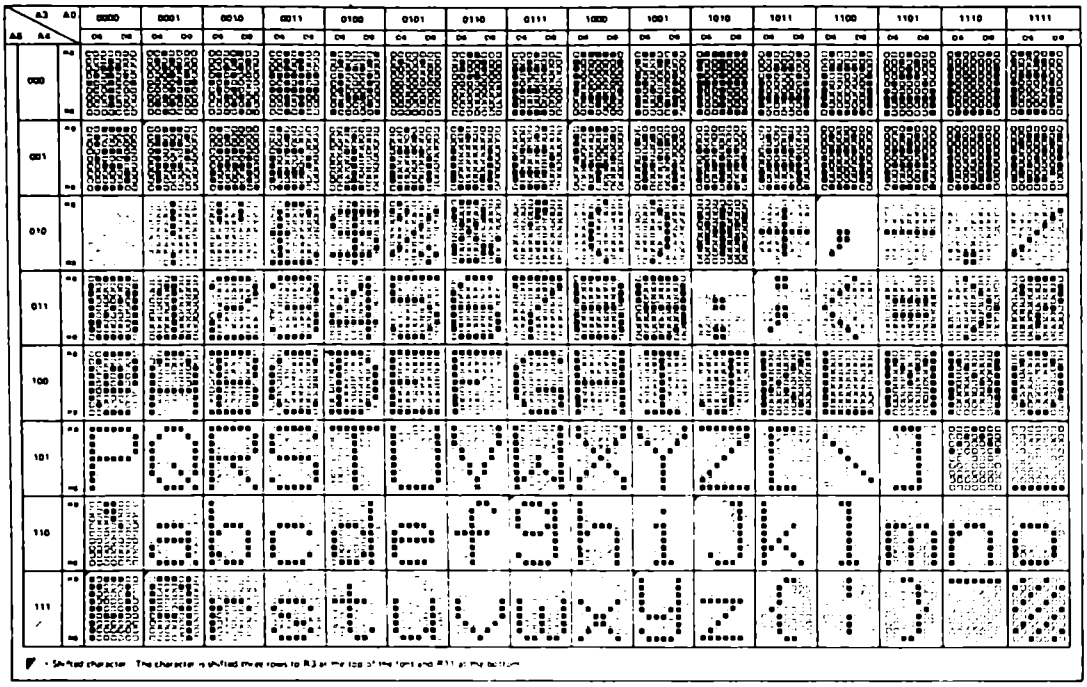
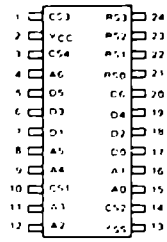


FIGURE 17 – MCM66790 PATTERN

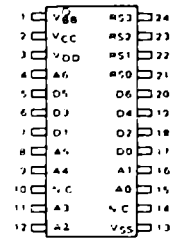


MCM6570 Series	MCM66700 Equivalent	Description
MCM6571	MCM66710	ASCII, shifted
MCM6571A	MCM66714	ASCII, shifted
MCM6572	MCM66720	ASCII
MCM6573	MCM66730	Japanese
MCM6573A	MCM66734	Japanese
MCM6574	MCM66740	Math Symbols
MCM6575	MCM66750	Alphanumeric Control
MCM6576	MCM66760	British, shifted
MCM6577	MCM66770	German, shifted
MCM6578	MCM66780	French, shifted
MCM6579	MCM66790	European, shifted

MCM66700 Series
Pin Assignment



MCM6570 Series
Pin Assignment

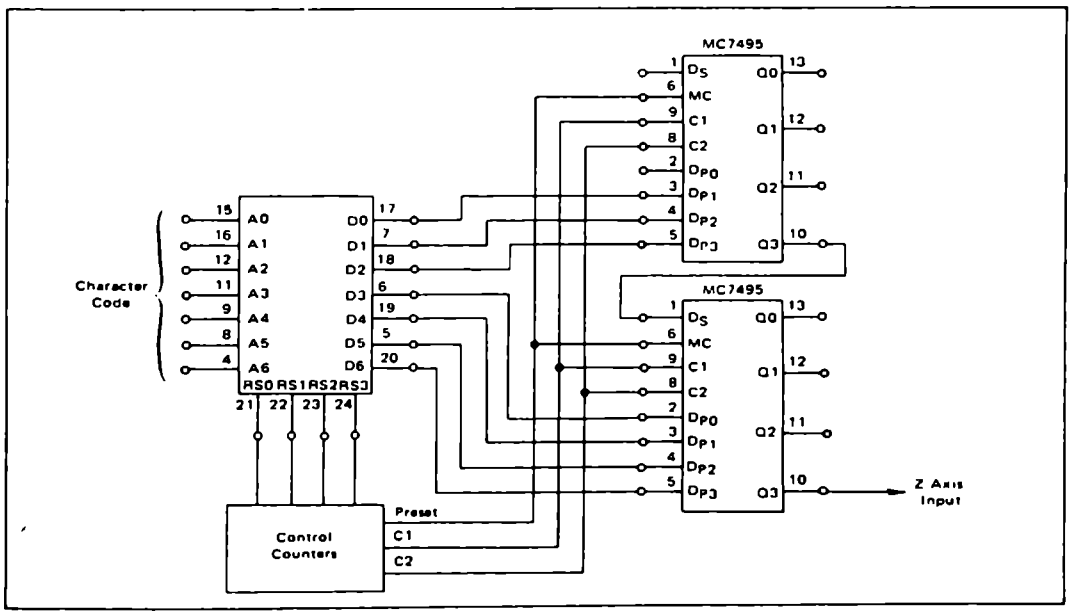


APPLICATIONS INFORMATION

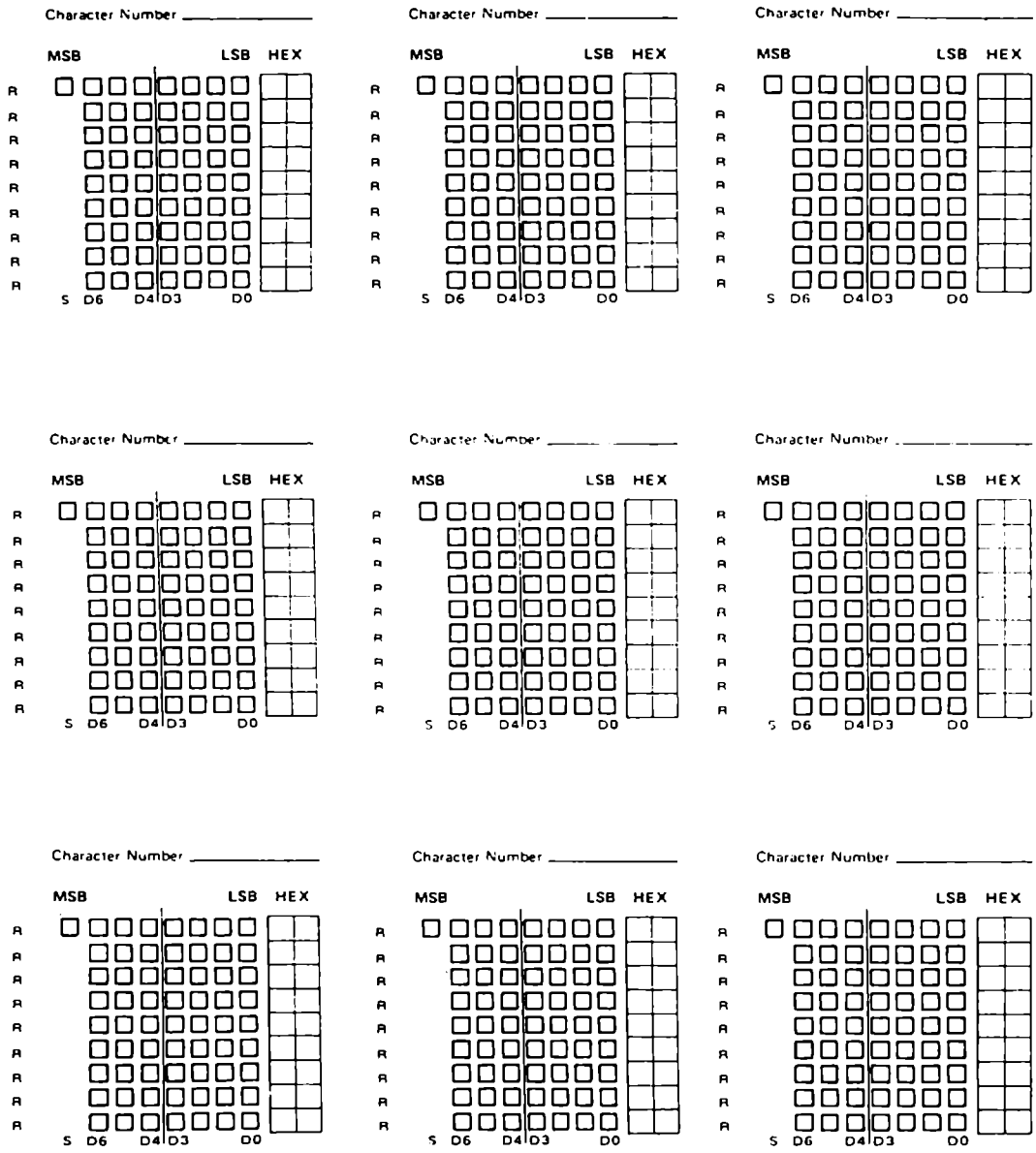
One important application for the MCM66700 series is in CRT display systems (Figure 18). A set of buffer shift registers or random access memories applies a 7-bit character code to the input of the character generator, which then supplies one row of the character according to the count at the four row select inputs. As each row is available, it is put into the TTL MC7495 shift registers. The parallel information in these shift registers is clocked serially out to the Z-axis where it modulates the raster to form the character.

The MCM66700 series require one power supply of +5.0 volts. When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit spikes or glitches on their outputs when the ac power is switched on and off.

FIGURE 18 – CRT DISPLAY APPLICATION USING MCM66710



The formats below are given for your convenience in preparing character information for MCM66700 programming. **THESE FORMATS ARE NOT TO BE USED TO TRANSMIT THE INFORMATION TO MOTOROLA.** Refer to the Custom Programming instructions for detailed procedures.



MOTOROLA

MCM68A30A
MCM68B30A

1024 X 8-BIT READ ONLY MEMORY

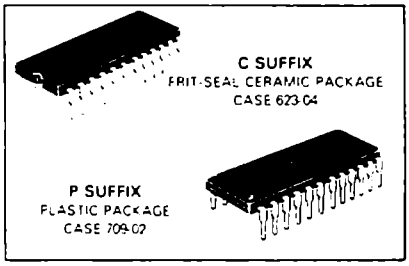
The MCM68A30A/MCM68B30A are mask-programmable byte-organized memories designed for use in bus-organized systems. They are fabricated with N-channel silicon-gate technology. For ease of use, the device operates from a single power supply, has compatibility with TTL and DTL, and needs no clocks or refreshing because of static operation.

The memory is compatible with the M6800 Microcomputer Family, providing read only storage in byte increments. Memory expansion is provided through multiple Chip Select inputs. The active level of the Chip Select inputs and the memory content are defined by the customer.

- Organized as 1024 Bytes of 8 Bits
- Static Operation
- Three-State Data Output
- Four Chip Select Inputs (Programmable)
- Single ±10% 5-Volt Power Supply
- TTL Compatible
- Maximum Access Time = 350 ns – MCM68A30A
  250 ns – MCM68B30A

MOS
(N-CHANNEL, SILICON-GATE)

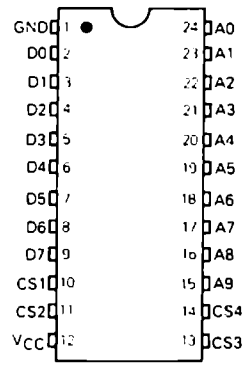
1024 X 8-BIT
READ ONLY MEMORY



C SUFFIX
FRIT-SEAL CERAMIC PACKAGE
CASE 623-04

P SUFFIX
PLASTIC PACKAGE
CASE 709-02

PIN ASSIGNMENT

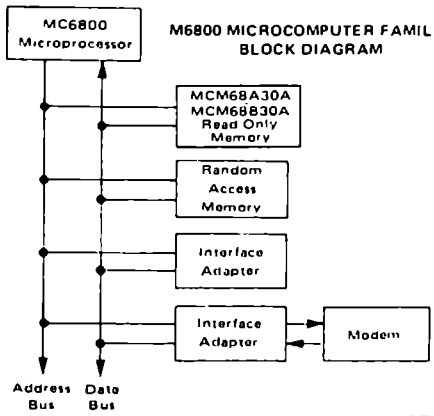


ABSOLUTE MAXIMUM RATINGS (See Note 1)

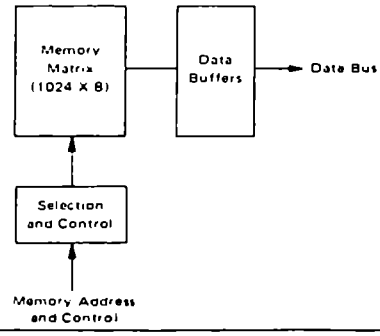
Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3 to +7.0	Vdc
Input Voltage	V_{in}	-0.3 to +7.0	Vdc
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

NOTE 1 Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

M6800 MICROCOMPUTER FAMILY
BLOCK DIAGRAM



MCM68A30A/MCM68B30A READ ONLY
MEMORY BLOCK DIAGRAM



DS9456 R1/6-78

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted.)

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Symbol	Min	Nom	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	Vdc
Input High Voltage	V_{IH}	2.0	-	5.5	Vdc
Input Low Voltage	V_{IL}	-0.3	-	0.8	Vdc

DC CHARACTERISTICS

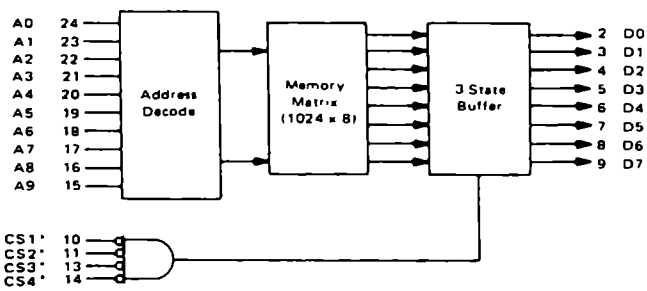
Characteristic	Symbol	Min	Typ	Max	Unit
Input Current (V_{in} = 0 to 5.5 V)	I_{in}	–	–	2.5	μAdc
Output High Voltage (I_{OH} = −205μA)	V_{OH}	2.4	–		Vdc
Output Low Voltage (I_{OL} = 1.6 mA)	V_{OL}	–	–	0.4	Vdc
Output Leakage Current (Three-State) (CS = 0.8 V or $\overline{CS}$ = 2.0 V, V_{out} = 0.4 V to 2.4 V)	I_{LO}	-	-	10	μAdc
Supply Current (V_{CC} = 5.5 V, T_A = 0°C)	I_{CC}	–	–	130	mAdc

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, periodically sampled rather than 100% tested.)

Characteristic	Symbol	Max	Unit
Input Capacitance	C_{in}	7.5	pF
Output Capacitance	C_{out}	12.5	pF

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

BLOCK DIAGRAM



*Active level defined by the customer.

V_{CC} = Pin 12
Gnd = Pin 1

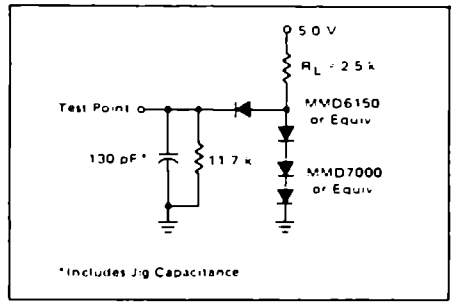
AC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature unless otherwise noted.)

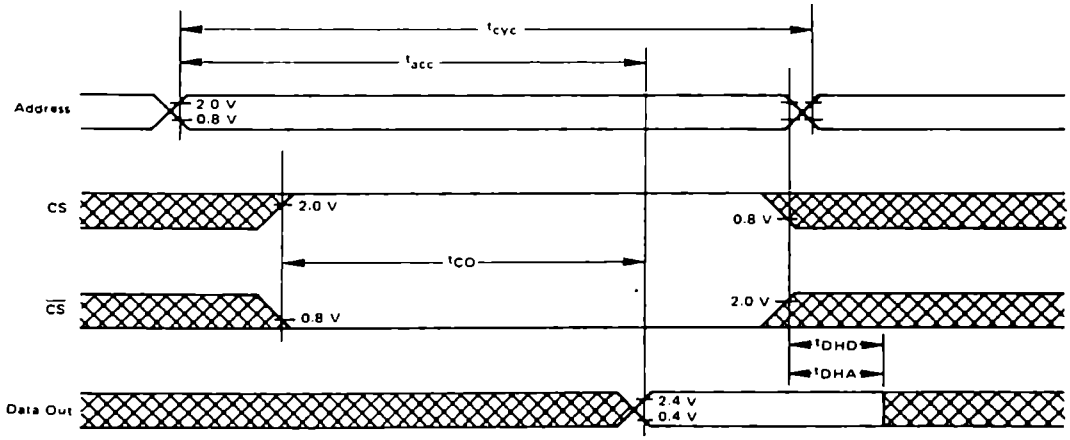
(All timing with $t_r = t_f = 20$ ns, Load of Figure 1)

Characteristic	Symbol	MCM68A30AL		MCM68B30AL		Unit
		Min	Max	Min	Max	
Cycle Time	t_{cyc}	350	–	250	–	ns
Access Time	t_{acc}	–	350	–	250	ns
Chip Select to Output Delay	t_{CO}	–	150	–	125	ns
Data Hold from Address	t_{DHA}	10	–	10	–	ns
Data Hold from Deselection	t_{DHD}	10	150	10	125	ns

FIGURE 1 – AC TEST LOAD



TIMING DIAGRAM



CUSTOM PROGRAMMING

By the programming of a single photomask for the MCM68A30A/MCM68B30A, the customer may specify the content of the memory and the method of enabling the outputs.

Information on the general options of the MCM68A30A/MCM68B30A should be submitted on an Organizational Data form such as that shown in Figure 3 ("No Connect" must always be the highest order Chip Select pin(s).)

Information for custom memory content may be sent to Motorola in one of four forms (shown in order of preference):

1. Paper tape output of the Motorola M6800 Software
2. Hexadecimal coding using IBM Punch Cards.
3. EPROM (MCM2708, MCM27A08, or MCM68708).
4. Hand-punched paper tape (Figure 3).

PAPER TAPE

Included in the software packages developed for the M6800 Microcomputer Family is the ability to produce a paper tape output for computerized mask generation. The assembler directives are used to control allocation of memory, to assign values for stored data, and for controlling the assembly process. The paper tape must specify the full 1024 bytes.

FIGURE 2 – BINARY TO HEXADECIMAL CONVERSION

Binary Data				Hexadecimal Character
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	A
1	0	1	1	B
1	1	0	0	C
1	1	0	1	D
1	1	1	0	E
1	1	1	1	F

IBM PUNCH CARDS

The hexadecimal equivalent (from Figure 2) may be placed on 80 column IBM punch cards as follows:

Step	Column	
1	12	Byte "0" Hexadecimal equivalent for outputs D7 thru D4 (D7 = M.S.B.)
2	13	Byte "0" Hexadecimal equivalent for outputs D3 thru D0 (D3 = M.S.B.)
3	14-75	Alternate steps 1 and 2 for consecutive bytes.
4	77-80	Card number (starting 0001)

FIGURE 3 – HAND PUNCHED PAPER TAPE FORMAT

Frames	
Leader	Blank Tape
1 to M	Allowed for customer use (M ≤ 64)
M + 1, M + 2	CR, LF (Carriage Return, Line Feed)
M + 3 to M + 66	First line of pattern information (64 hex figures per line)
M + 67, M + 68	CR, LF
M + 69 to M + 2112	Remaining 31 lines of hex figures, each line followed by a Carriage Return and Line Feed

Blank Tape

Frames 1 to M are left to the customer for internal identification, where M ≤ 64. Any combination of alphanumerics may be used. This information is terminated with a Carriage Return and Line Feed, delineating the start of data entry. (Note that the tape cannot begin with a CR and/or LF, or the customer identification will be assumed to be programming data.)

Option A (1024 x 8)

Frame M + 3 contains the hexadecimal equivalent of bits D7 thru D4 of byte 0. Frame M + 4 contains bits D3 thru D0. These two hex figures together program byte 0. Likewise, frames M + 5 and M + 6 program byte 1, while M + 7 and M + 8 program byte 2. Frames M + 3 to M + 66 comprise the first line of the printout and program, in sequence, the first 32 bytes of storage. The line is terminated with a CR and LF.

Option B (2048 x 4)

Frame M + 3 contains the hexadecimal equivalent of byte 0, bits D3 thru D0. Frame M + 4 contains byte 1, frame M + 5 byte 2, and so on. Frames M + 3 to M + 66 sequentially program bytes 0 to 31 (the first 32 bytes). The line is terminated with a CR and LF.

Both Options

The remaining 31 lines of data are punched in sequence using the same format, each line terminated with a CR and LF. The total 32 lines of data contain 32 x 64 or 2048 characters. Since each character programs 4 bits of information, a full 8192 bits are programmed.

As an example, a printout of the punched tape for Figure 13 would read as shown in Figure 10 (a CR and LF is implicit at the end of each line).

FIGURE 4 – FORMAT FOR PROGRAMMING GENERAL OPTIONS

ORGANIZATIONAL DATA
MCM68A30A/68B30A MOS READ ONLY MEMORY

Customer

Company _____

Part No _____

Originator _____

Phone No. _____

Motorola Use Only:

Quote _____

Part No. _____

Specif. No. _____

Chip Select Options:

	Active High	Active Low	No Connect "Don't Care"
CS1	☐	☐	☐
CS2	☐	☐	☐
CS3	☐	☐	☐
CS4	☐	☐	☐

MOTOROLA

MCM68A308
MCM68B308

1024 X 8-BIT READ ONLY MEMORY

The MCM68A308/MCM68B308 is a mask-programmable byte organized memory designed for use in bus-organized systems. It is fabricated with N-channel silicon-gate technology. For ease of use, the device operates from a single power supply, has compatibility with TTL and DTL, and needs no clocks or refreshing because of static operation.

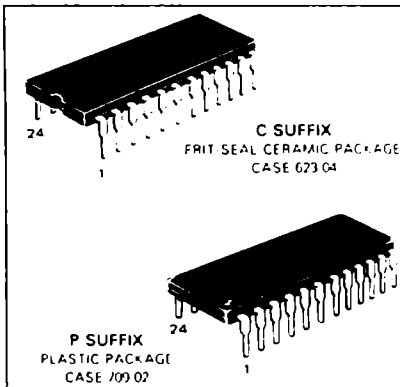
The memory is compatible with the M6800 Microcomputer Family, providing read only storage in byte increments. Memory expansion is provided through multiple Chip Select inputs. The active level of the Chip Select inputs and the memory content are defined by the customer.

- Organized as 1024 Bytes of 8 Bits
- Static Operation
- Three-State Data Output
- Mask-Programmable Chip Selects for Simplified Memory Expansion
- Single ±10% 5-Volt Power Supply
- TTL Compatible
- Maximum Access Time = 350 ns – MCM68A308
  250 ns – MCM68B308
- 350 mW Typical Power Dissipation

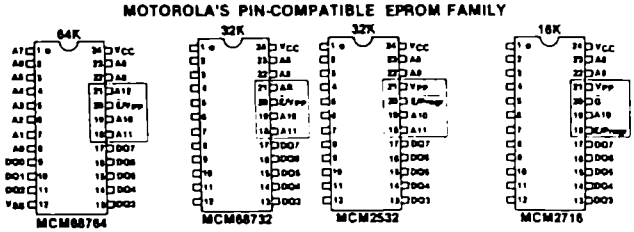
MOS

(N-CHANNEL, SILICON-GATE)

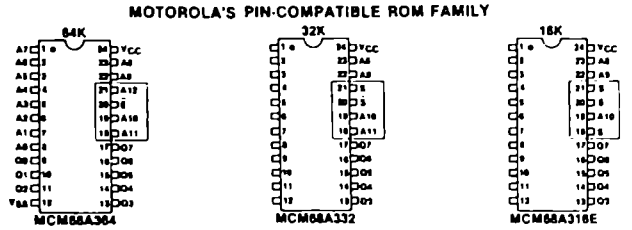
1024 X 8-BIT
READ ONLY MEMORY



MOTOROLA'S PIN-COMPATIBLE EPROM FAMILY

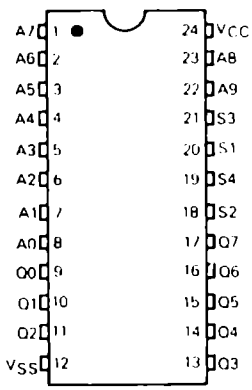


MOTOROLA'S PIN-COMPATIBLE ROM FAMILY



INDUSTRY STANDARD PINOUTS

PIN ASSIGNMENT



PIN NAMES	
A0 – A9	Address Inputs
S1 – S4	Chip Selects
O0 – O7	Data Output
VCC	+5 V Power Supply
VSS	Ground

DS9501/6-78

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted)

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	Vdc
Input High Voltage	V_{IH}	2.0	-	5.5	Vdc
Input Low Voltage	V_{IL}	-0.3		0.8	Vdc

DC CHARACTERISTICS

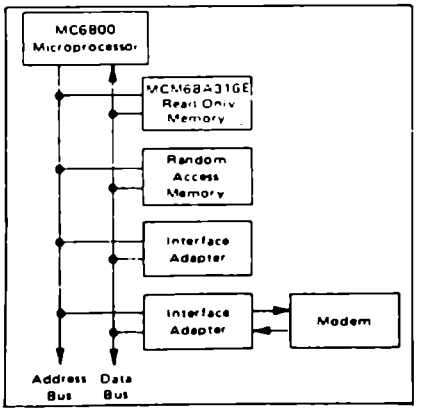
Characteristic	Symbol	Min	Max	Unit
Input Current (V_{in} = 0 to 5.5 V)	I_{in}	-	2.5	μAdc
Output High Voltage (I_{OH} = -205 μA)	V_{OH}	2.4		Vdc
Output Low Voltage (I_{OL} = 1.6 mA)	V_{OL}	-	0.4	Vdc
Output Leakage Current (Three-State) (S = 0.8 V or $\overline{S}$ = 2.0 V, V_{out} = 0.4 V to 2.4 V)	I_{LO}		10	μAdc
Supply Current (V_{CC} = 5.5 V, T_A = 0°C)	I_{CC}		130	mAdc

ABSOLUTE MAXIMUM RATINGS (See Note 1)

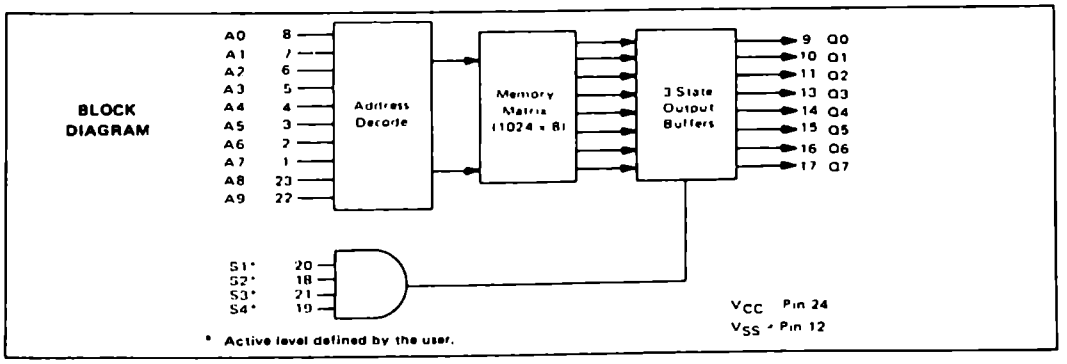
Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3 to +7.0	Vdc
Input Voltage	V_{in}	-0.3 to +7.0	Vdc
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

NOTE 1: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

M6800 MICROCOMPUTER FAMILY BLOCK DIAGRAM



BLOCK DIAGRAM



AC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature unless otherwise noted.
All timing with $t_r = t_f = 20$ ns, Load of Figure 1)

Characteristic	Symbol	MCM68A308		MCM68B308		Unit
		Min	Max	Min	Max	
Cycle Time	t_{cyc}	350	-	250	–	ns
Access Time	t_{acc}	–	350	–	250	ns
Chip Select to Output Delay	t_{SO}	–	150	–	150	ns
Data Hold from Address	t_{DHA}	10	–	10	–	ns
Data Hold from Deselection	t_{DHD}	10	150	10	150	ns

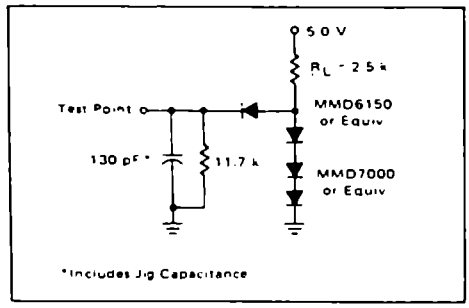
CAPACITANCE

(f = 2.0 MHz, $T_A = 25^{\circ}C$, periodically sampled rather than 100% tested)

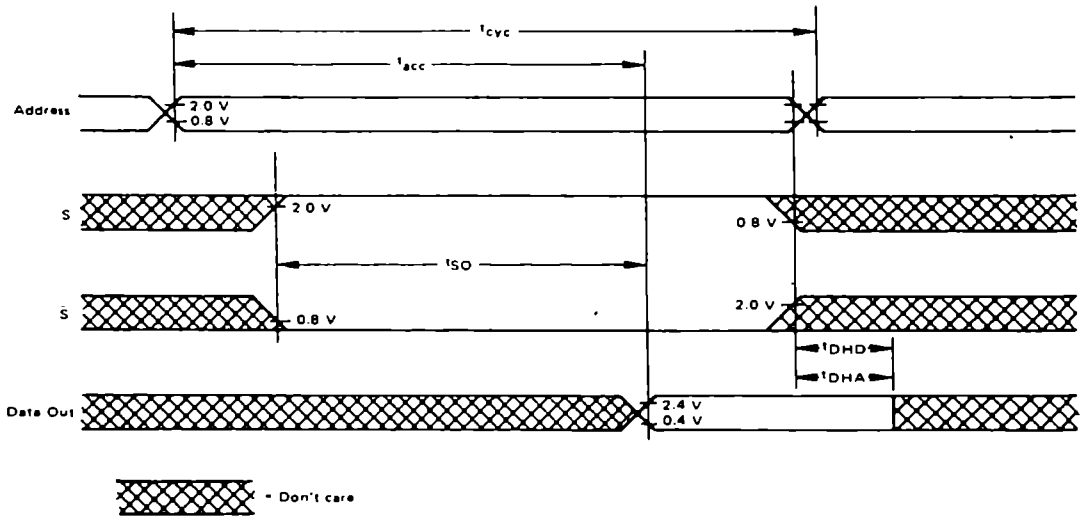
Characteristic	Symbol	Max	Unit
Input Capacitance	C_{in}	7.5	pF
Output Capacitance	C_{out}	12.5	pF

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields, however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

FIGURE 1 – AC TEST LOAD



TIMING DIAGRAM



CUSTOM PROGRAMMING

By the programming of a single photomask for the MCM68A308/MCM68B308, the customer may specify the content of the memory and the method of enabling the outputs. (A "no-connect" must always be the highest order chip-select(s).)

Information on the general options of the MCM68A308/MCM68B308 should be submitted on an Organizational Data form such as that shown in Figure 4.

Information for customer memory content may be sent to Motorola in one of four forms (shown in order of preference):

1. Paper tape output of the Motorola M6800 Software
2. Hexadecimal coding using IBM Punch Cards
3. EPROM one MCM68A708 or equivalent.
4. Hand punched paper tape (Figure 3).

PAPER TAPE

Included in the software packages developed for the M6800 Microcomputer Family is the ability to produce a paper tape output for computerized mask generation. The assembler directives are used to control allocation of memory, to assign values for stored data, and for controlling the assembly process. The paper tape must specify the full 1024 bytes.

FIGURE 2 – BINARY TO HEXADECIMAL CONVERSION

Binary Data				Hexadecimal Character
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	A
1	0	1	1	B
1	1	0	0	C
1	1	0	1	D
1	1	1	0	E
1	1	1	1	F

IBM PUNCH CARDS

The hexadecimal equivalent (from Figure 2) may be placed on 80 column IBM punch cards as follows:

Step	Column	
1	12	Byte "0" Hexadecimal equivalent for outputs Q7 thru Q4 (Q7 = M.S.B.)
2	13	Byte "0" Hexadecimal equivalent for outputs Q3 thru Q0 (Q3 = M.S.B.)
3	14-75	Alternate steps 1 and 2 for consecutive bytes
4	77-80	Card number (starting 0001)

FIGURE 3 – HAND-PUNCHED PAPER TAPE FORMAT

Frames	
Leader	Blank Tape
1 to M	Allowed for customer use ($M \leq 64$)
M + 1, M + 2	CR; LF (Carriage Return, Line Feed)
M + 3 to M + 66	First line of pattern information (64 hex figures per line)
M + 67, M + 68	CR; LF
M + 69 to M + 2112	Remaining 31 lines of hex figures, each line followed by a Carriage Return and Line Feed
Blank Tape	

Frames 1 to M are left to the customer for internal identification, where $M \leq 64$. Any combination of alpha-numerics may be used. This information is terminated with a Carriage Return and Line Feed, delineating the start of data entry. (Note that the tape cannot begin with a CR and/or LF, or the customer identification will be assumed to be programming data.)

Frame M + 3 contains the hexadecimal equivalent of bits Q7 thru Q4 of byte 0. Frame M + 4 contains bits Q3 thru Q0. These two hex figures together program byte 0. Likewise, frames M + 5 and M + 6 program byte 1, while M + 7 and M + 8 program byte 2. Frames M + 3 to M + 66 comprise the first line of the printout and program, in sequence, the first 32 bytes of storage. The line is terminated with a CR and LF.

The remaining 31 lines of data are punched in sequence using the same format, each line terminated with a CR and LF. The total 32 lines of data contain 32 x 64 or 2048 characters. Since each character programs 4 bits of information, a full 8192 bits are programmed.

FIGURE 4 – FORMAT FOR PROGRAMMING GENERAL OPTIONS

ORGANIZATIONAL DATA
MCM68308 MOS READ ONLY MEMORY

Customer:

Company _____

Part No. _____

Originator _____

Phone No. _____

Motorola Use Only:

Quote: _____

Part No _____

Specif. No.: _____

Chip Select:

	Active High	Active Low	No Connect
S1	☐	☐	☐
S2	☐	☐	☐
S3	☐	☐	☐
S4	☐	☐	☐

MOTOROLA

MCM68A316A

2048 X 8-BIT READ ONLY MEMORY

The MCM68A316A is a mask programmable byte-organized memory designed for use in bus organized systems. It is fabricated with N-channel silicon-gate technology. For ease of use, the device operates from a single power supply, has compatibility with TTL and DTL, and needs no clocks or refreshing because of fully static operation.

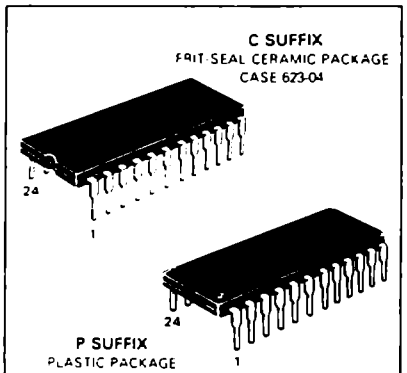
The memory is compatible with the M6800 Microcomputer Family, providing read-only storage in byte increments. Memory expansion is provided through multiple Chip Select inputs. The active level of the Chip Select inputs and the memory content are defined by the user.

- Fully Static Operation
- Three-State Data Output
- Mask-Programmable Chip Selects for Simplified Memory Expansion
- Single ± 10% 5-Volt Power Supply
- TTL Compatible
- Maximum Access Time = 350 ns
- Plug-in Compatible with 2316A

MOS

(N-CHANNEL, SILICON-GATE)

2048 X 8-BIT
READ ONLY MEMORY

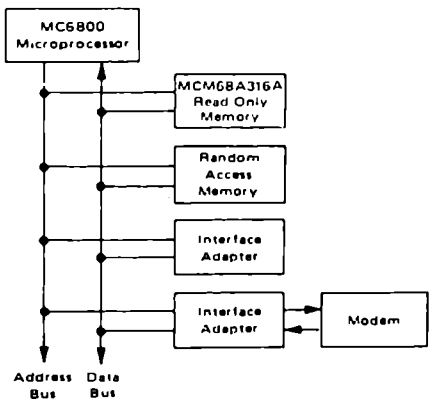


ABSOLUTE MAXIMUM RATINGS (See Note 1)

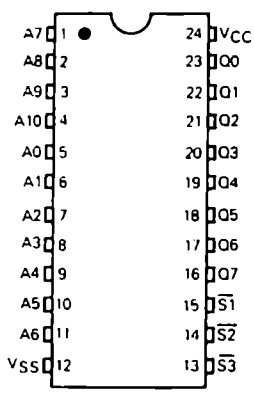
Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3 to +7.0	Vdc
Input Voltage	V_{in}	-0.3 to +7.0	Vdc
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

NOTE 1: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

M6800 MICROCOMPUTER FAMILY BLOCK DIAGRAM



PIN ASSIGNMENT



PIN NAMES	
A0-A10	Address Inputs
S1-S3	Chip Selects
Q0-Q7	Data Output
V_{CC}	+5 V Power Supply
V_{SS}	Ground

DS9502/6-78

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted)

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	Vdc
Input High Voltage	V_{IH}	2.0	-	5.5	Vdc
Input Low Voltage	V_{IL}	-0.3		0.8	Vdc

DC CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit
Input Current (V_{in} = 0 to 5.5 V)	I_{in}	-	2.5	μAdc
Output High Voltage (I_{OH} = -205 μA)	V_{OH}	2.4	–	Vdc
Output Low Voltage (I_{OL} = 1.6 mA)	V_{OL}		0.4	Vdc
Output Leakage Current (Three-State) (S = 0.8 V or $\overline{S}$ = 2.0 V, V_{out} = 0.4 V to 2.4 V)	I_{LO}		10	μAdc
Supply Current (V_{CC} = 5.5 V, T_A = 0°C)	I_{CC}	-	130	mAdc

CAPACITANCE

(f = 2.0 MHz, T_A = 25°C, periodically sampled rather than 100% tested)

Characteristic	Symbol	Max	Unit
Input Capacitance	C_{in}	7.5	pF
Output Capacitance	C_{out}	12.5	pF

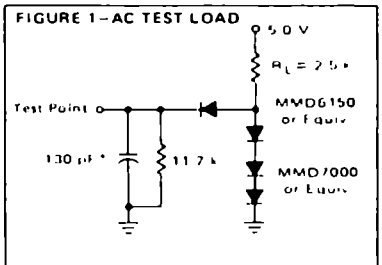
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

AC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature unless otherwise noted.
All timing with t_r, t_f = 20 ns, Load of Figure 1)

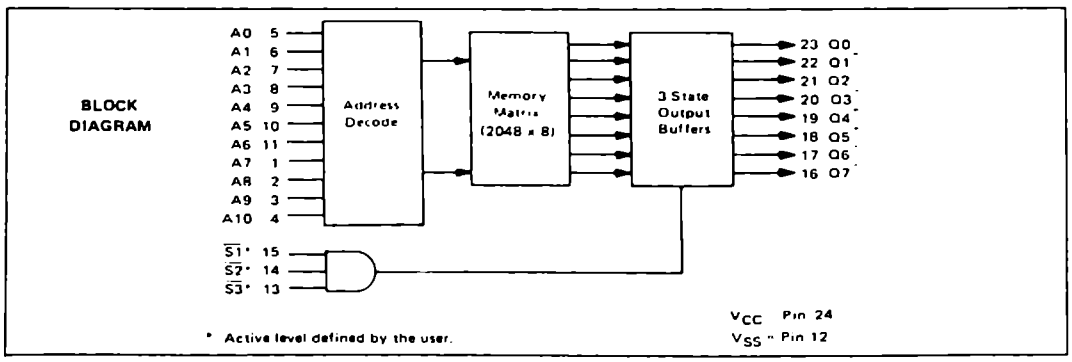
Characteristic	Symbol	Min	Max	Unit
Cycle Time	t_{cyc}	350	–	ns
Access Time	t_{acc}	-	350	ns
Chip Select to Output Delay	t_{SO}	-	150	ns
Data Hold from Address	t_{DHA}	10		ns
Data Hold from Deselection	t_H	10	150	ns

FIGURE 1–AC TEST LOAD



*Includes Jig Capacitance

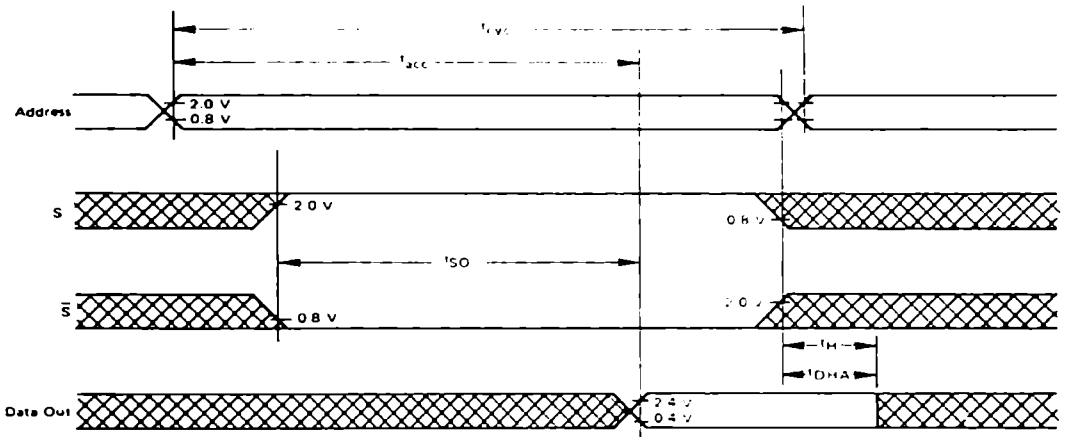
BLOCK DIAGRAM



* Active level defined by the user.

V_{CC} Pin 24
V_{SS} = Pin 12

TIMING DIAGRAM



CUSTOM PROGRAMMING

By the programming of a single photomask for the MCM68316A, the customer may specify the content of the memory and the method of enabling the outputs

Information on the general options of the MCM68A316A should be submitted on an Organizational Data form such as that shown in Figure 3.

Information for custom memory content may be sent to Motorola in one of four forms (shown in order of preference):

1. Paper tape output of the Motorola M6800 Software.
2. Hexadecimal coding using IBM Punch Cards.
3. EPROM (TMS2716 or MCM2716).
4. Hand-punched paper tape.

PAPER TAPE

Included in the software packages developed for the M6800 Microcomputer Family is the ability to produce a paper tape output for computerized mask generation. The assembler directives are used to control allocation of memory, to assign values for stored data, and for controlling the assembly process. The paper tape must specify the full 2048 bytes.

FIGURE 2 – BINARY TO HEXADECIMAL CONVERSION

Binary Data				Hexadecimal Character
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	A
1	0	1	1	B
1	1	0	0	C
1	1	0	1	D
1	1	1	0	E
1	1	1	1	F

IBM PUNCH CARDS

The hexadecimal equivalent (from Figure 2) may be placed on 80 column IBM punch cards as follows:

Step	Column	
1	12	Byte "0" Hexadecimal equivalent for outputs O7 thru O4 (O7 = M.S.B.)
2	13	Byte "0" Hexadecimal equivalent for outputs O3 thru O0 (O3 = M.S.B.)
3	14 – 75	Alternate steps 1 and 2 for consecutive bytes.
4	77 – 80	Card number (starting 0001) Total number of cards (64)

FIGURE 3 – FORMAT FOR PROGRAMMING GENERAL OPTIONS

ORGANIZATIONAL DATA
MCM68A316A MOS READ ONLY MEMORY

Customer:

Company _____

Part No. _____

Originator _____

Phone No _____

Motorola Use Only

Quote _____

Part No. _____

Specif. No. _____

Chip Select:

	Active High	Active Low	*Don't Care (No Connect)
$\overline{S1}$	☐	☐	☐
$\overline{S2}$	☐	☐	☐
$\overline{S3}$	☐	☐	☐

*A don't care must always be the highest order Chip Select(s).

MOTOROLA

MCM68A316E

2048 X 8 BIT READ ONLY MEMORY

The MCM68A316E is a mask-programmable byte-organized memory designed for use in bus-organized systems. It is fabricated with N-channel silicon-gate technology. For ease of use, the device operates from a single power supply, has compatibility with TTL and DTL, and needs no clocks or refeshing because of static operation.

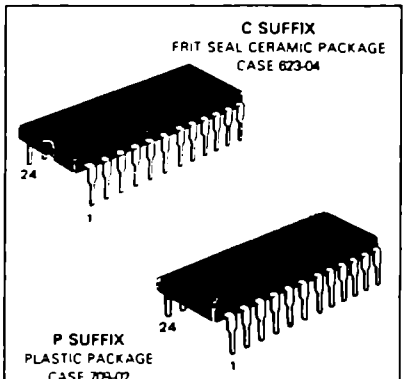
The memory is compatible with the M6800 Microcomputer Family, providing read only storage in byte increments. Memory expansion is provided through multiple Chip Select inputs. The active level of the Chip Select inputs and the memory content are defined by the user.

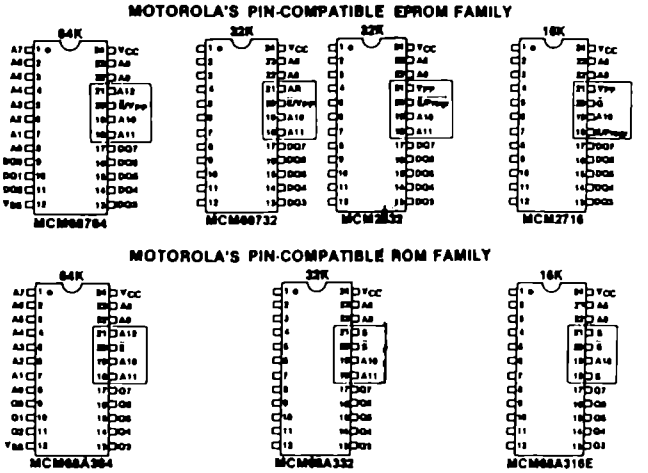
- Fully Static Operation
- Three-State Data Output
- Mask-Programmable Chip Selects for Simplified Memory Expansion
- Single ± 10% 5-Volt Power Supply
- TTL Compatible
- Maximum Access Time = 350 ns
- Plug-in Compatible with 2316E
- Pin Compatible with 2708 and TMS2716 EPROMs

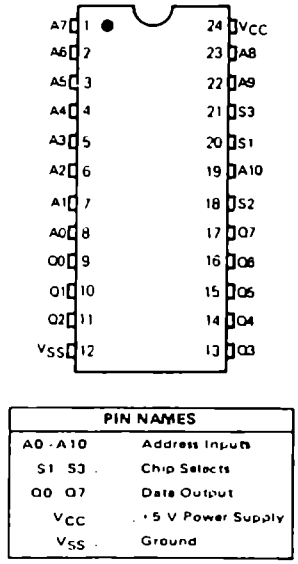
MOS

(N-CHANNEL, SILICON-GATE)

2048 X 8 BIT
READ ONLY MEMORY







PIN NAMES	
A0 - A10	Address Inputs
S1, S3	Chip Selects
O0 - O7	Data Output
V_{CC}	+5 V Power Supply
V_{SS}	Ground

DS9600/6-78

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted)

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	Vdc
Input High Voltage	V_{IH}	2.0	–	5.5	Vdc
Input Low Voltage	V_{IL}	-0.3	–	0.8	Vdc

DC CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit
Input Current (V_{in} = 0 to 5.5 V)	I_{in}	–	2.5	μAdc
Output High Voltage (I_{OH} = -205 μA)	V_{OH}	2.4	–	Vdc
Output Low Voltage (I_{OL} = 1.6 mA)	V_{OL}	–	0.4	Vdc
Output Leakage Current (Three-State) (S = 0.8 V or $\overline{S}$ = 2.0 V, V_{out} = 0.4 V to 2.4 V)	I_{LO}	–	10	μAdc
Supply Current (V_{CC} = 5.5 V, T_A = 0°C)	I_{CC}	–	130	mAdc

ABSOLUTE MAXIMUM RATINGS (See Note 1)

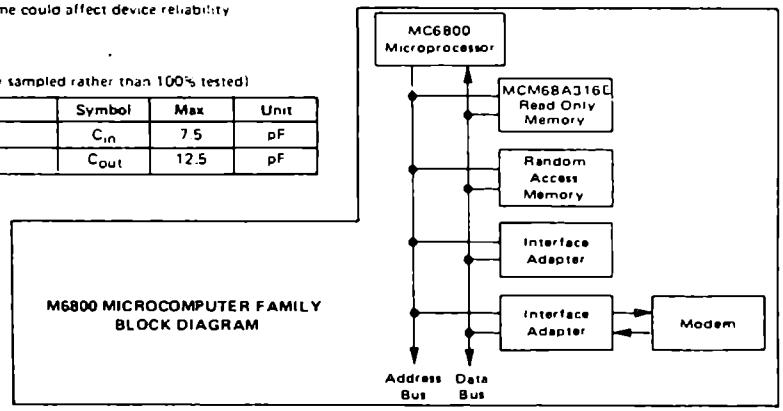
Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3 to +7.0	Vdc
Input Voltage	V_{in}	-0.3 to +7.0	Vdc
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

NOTE 1: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

CAPACITANCE

(f = 2.0 MHz, T_A = 25°C, periodically sampled rather than 100% tested)

Characteristic	Symbol	Max	Unit
Input Capacitance	C_{in}	7.5	pF
Output Capacitance	C_{out}	12.5	pF



M6800 MICROCOMPUTER FAMILY
BLOCK DIAGRAM

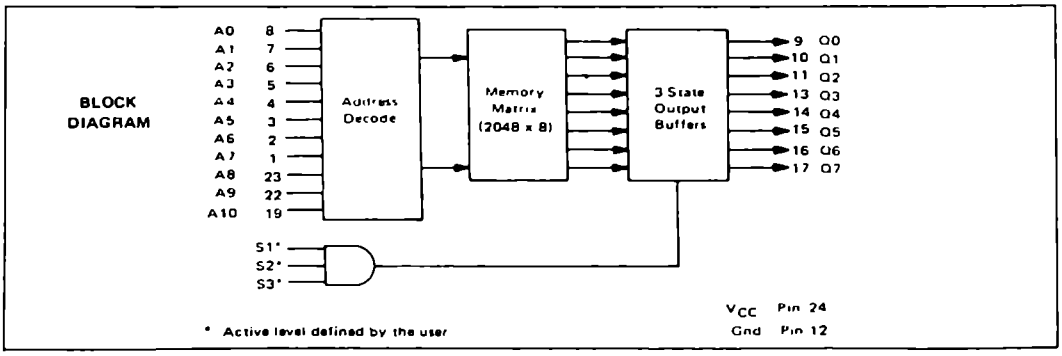
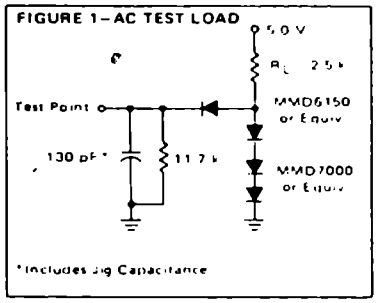


FIGURE 1–AC TEST LOAD



*Includes Jig Capacitance

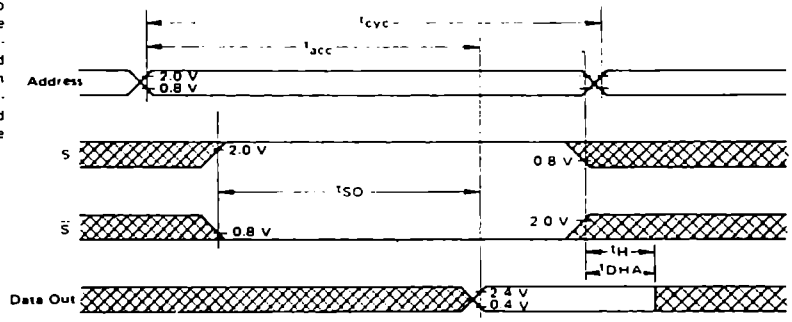
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

AC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature unless otherwise noted
All timing with t_r, t_f = 20 ns Load of Figure 1)

Characteristic	Symbol	Min	Max	Unit
Cycle Time	t_{cyc}	350	–	ns
Access Time	t_{acc}	–	350	ns
Chip Select to Output Delay	t_{SO}	–	150	ns
Data Hold from Address	t_{DHA}	10	–	ns
Data Hold from Deselection	t_H	10	150	ns

TIMING DIAGRAM



CUSTOM PROGRAMMING

By the programming of a single photomask for the MCM68A316E, the customer may specify the content of the memory and the method of enabling the outputs.

Information on the general options of the MCM68A316E should be submitted on an Organizational Data form such as that shown in Figure 3. ("No-Connect" must always be the highest order Chip Select(s).)

Information for custom memory content may be sent to Motorola in one of three forms (shown in order of preference):

1. Paper tape output of the Motorola M6800 Software.
2. Hexadecimal coding using IBM Punch Cards.
3. EPROM (TMS2716 or MCM2716).

PAPER TAPE

Included in the software packages developed for the M6800 Microcomputer Family is the ability to produce a paper tape output for computerized mask generation. The assembler directives are used to control allocation of memory, to assign values for stored data, and for controlling the assembly process. The paper tape must specify the full 2048 bytes.

FIGURE 2 – BINARY TO HEXADECIMAL CONVERSION

Binary Data				Hexadecimal Character
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	A
1	0	1	1	B
1	1	0	0	C
1	1	0	1	D
1	1	1	0	E
1	1	1	1	F

IBM PUNCH CARDS

The hexadecimal equivalent (from Figure 2) may be placed on 80 column IBM punch cards as follows

Step	Column	
1	12	Byte "0" Hexadecimal equivalent for outputs Q7 thru Q4 (Q7 = M.S.B.)
2	13	Byte "0" Hexadecimal equivalent for outputs Q3 thru Q0 (Q3 = M.S.B.)
3	14-75	Alternate steps 1 and 2 for consecutive bytes.
4	77-80	Card number (starting 0001) Total number of cards (64)

FIGURE 3 – FORMAT FOR PROGRAMMING GENERAL OPTIONS

ORGANIZATIONAL DATA
MCM68A316E MOS READ ONLY MEMORY

Customer:

Company _____

Part No. _____

Originator _____

Phone No. _____

Motorola Use Only

Quote. _____

Part No.. _____

Specif. No.. _____

Chip Select:

	Active High	Active Low	No Connect
S1	☐	☐	☐
S2	☐	☐	☐
S3	☐	☐	☐

MOTOROLA

MCM68A332

4096 X 8-BIT READ ONLY MEMORY

The MCM68A332 is a mask programmable byte-organized memory designed for use in bus-organized systems. It is fabricated with N-channel silicon-gate technology. For ease of use, the device operates from a single power supply, has compatibility with TTL and DTL, and needs no clocks or refreshing because of static operation.

The memory is compatible with the M6800 Microcomputer Family, providing read only storage in byte increments. Memory expansion is provided through multiple Chip Select inputs. The active level of the Chip Select inputs and the memory content are defined by the user.

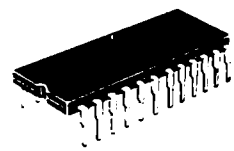
- Fully Static Operation
- Three-State Data Output for OR-Ties
- Mask-Programmable Chip Selects for Simplified Memory Expansion
- Single ±10% 5-Volt Power Supply
- Fully TTL Compatible
- Maximum Access Time = 350 ns
- Directly Compatible with 4732
- Pin Compatible with 2708 and 2716 EPROMs
- Preprogrammed MCM68A332-2 Available

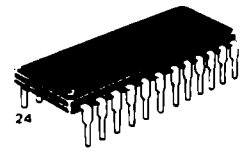
MOS

(N-CHANNEL, SILICON-GATE)

4096 X 8-BIT
READ ONLY MEMORY

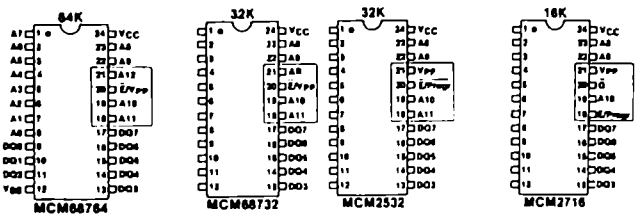
C SUFFIX
FRIT SEAL CERAMIC PACKAGE
CASE 623-04



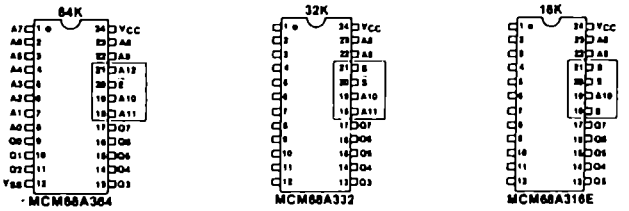


P SUFFIX
PLASTIC PACKAGE
CASE 709-02

MOTOROLA'S PIN-COMPATIBLE EPROM FAMILY

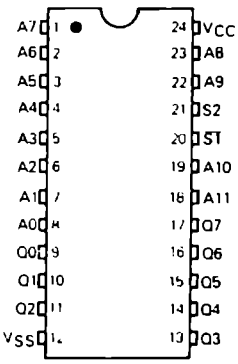


MOTOROLA'S PIN-COMPATIBLE ROM FAMILY



INDUSTRY STANDARD PINOUTS

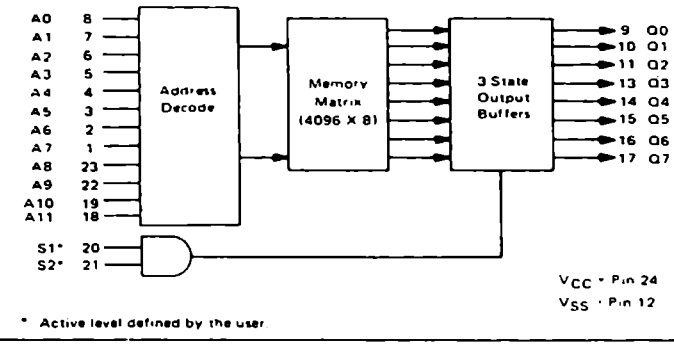
PIN ASSIGNMENT



PIN NAMES	
A0 - A11	Address Inputs
S	Programmable Chip Selects
O0 - O7	Data Output
V_{CC}	+5 V Power Supply
V_{SS}	Ground

DS9519/7-78

BLOCK DIAGRAM



* Active level defined by the user

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted)

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (V_{CC} must be applied at least 100 µs before proper device operation is achieved)	V_{CC}	4.5	5.0	5.5	Vdc
Input High Voltage	V_{IH}	2.0	–	5.5	Vdc
Input Low Voltage	V_{IL}	-0.3	–	0.8	Vdc

DC CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit
Input Current (V_{in} = 0 to 5.5 V)	I_{in}	–	2.5	µAdc
Output High Voltage (I_{OH} = -205 µA)	V_{OH}	2.4	–	Vdc
Output Low Voltage (I_{OL} = 1.6 mA)	V_{OL}	–	0.4	Vdc
Output Leakage Current (Three-State) (S1 = 0.8 V or S2 = 2.0 V, V_{out} = 0.4 V to 2.4 V)	I_{LO}	–	10	µAdc
Supply Current (V_{CC} = 5.5 V, T_A = 0°C)	I_{CC}	–	80	mAdc

ABSOLUTE MAXIMUM RATINGS (See Note 1)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3 to +7.0	Vdc
Input Voltage	V_{in}	-0.3 to +7.0	Vdc
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

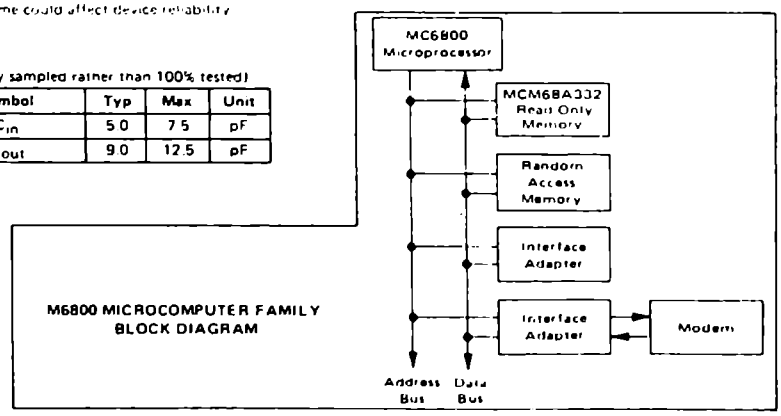
NOTE 1 Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

CAPACITANCE

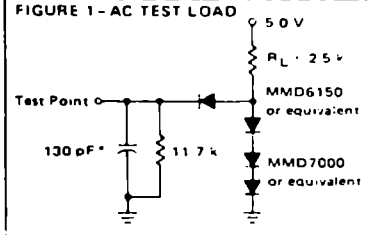
(f = 1.0 MHz, T_A = 25°C, periodically sampled rather than 100% tested)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance	C_{in}	5.0	7.5	pF
Output Capacitance	C_{out}	9.0	12.5	pF



M6800 MICROCOMPUTER FAMILY BLOCK DIAGRAM

FIGURE 1 – AC TEST LOAD



*Includes jig capacitance

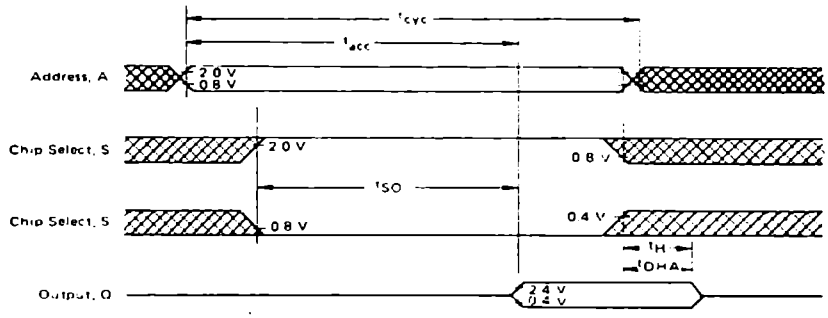
AC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature unless otherwise noted)

All timing with t_r, t_f = 20 ns, Load of Figure 1)

Characteristic	Symbol	Min	Max	Unit
Cycle Time	t_{cyc}	350		ns
Access Time	t_{acc}		350	ns
Chip Select to Output Delay	t_{SO}		150	ns
Data Hold from Address	t_{DHA}	10		ns
Data Hold from Deselection	t_H	10	150	ns

TIMING DIAGRAM



Waveform Symbol	Input	Output	Waveform Symbol	Input	Output	Waveform Symbol	Input	Output
———	MUST BE VALID	WILL BE VALID	▨	DON'T CARE ANY CHANGE PERMITTED	CHANGING STATE UNKNOWN	⟋⟍		HIGH IMPEDANCE

MCM68A332 CUSTOM PROGRAMMING

By the programming of a single photomask for the MCM68A332, the customer may specify the content of the memory and the method of enabling the outputs.

Information on the general options of the MCM68A332 should be submitted on an Organizational Data form such as that shown in Figure 3. (A "No-Connect" or "Don't Care" must always be the highest order Chip Select(s).)

Information for custom memory content may be sent to Motorola in one of four forms (shown in order of preference):

1. IBM Punch Cards:
   - A. Hexadecimal Format
   - B. Intel Format
   - C. Binary Negative-Postive Format
2. EPROMs—two 16K (MCM2716 or TMS2716) or four 8K (MCM2708)
3. Paper tape output of the Motorola M6800 software
4. Hand punched paper tape

PAPER TAPE

Included in the software packages developed for the M6800 Microcomputer Family is the ability to produce a paper tape output for computerized mask generation. The assembler directives are used to control allocation of memory, to assign values for stored data, and for controlling the assembly process. The paper tape must specify the full 4096 bytes.

IBM PUNCH CARDS, HEXADECIMAL FORMAT

The hexadecimal equivalent (from Figure 2) may be placed on 80 column IBM punch cards as follows:

Step	Column	
1	12	Byte "0" Hexadecimal equivalent for outputs Q7 through Q4 (Q7 = M.S.B.)
2	13	Byte "0" Hexadecimal equivalent for outputs Q3 through Q0 (Q3 = M.S.B.)
3	14–75	Alternate steps 1 and 2 for consecutive bytes.
4	77–79	Card number (starting 001).
5		Total number of cards must equal 128.

FIGURE 2 – BINARY TO HEXADECIMAL CONVERSION

Binary Data				Hexadecimal Character
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	A
1	0	1	1	B
1	1	0	0	C
1	1	0	1	D
1	1	1	0	E
1	1	1	1	F

PRE-PROGRAMMED MCM68A332P2, MCM68A332C2

The -2 standard ROM pattern contains sine-lookup and arctan-lookup tables.

Locations 0000 through 2001 contain the sine values. The sine's first quadrant is divided into 1000 parts with sine values corresponding to these angles stored in the ROM. Sin $\pi/2$ is included and is rounded to 0.9999.

The arctan values contain angles in radians corresponding to the arc tangents of 0 through 1 in steps of 0.001 and are contained in locations 2048 through 4049.

Locations 2002 through 2047 and 4050 through 4095 are zero filled.

All values are represented in absolute decimal format with four digit precision. They are stored in BCD format with the two most significant digits in the lower byte and the two least significant digits in the upper byte. The decimal point is assumed to be to the left of the most significant digit.

Example: $\sin\left(\frac{1}{1000}\ \frac{\pi}{2}\right) \approx 0.0016$ decimal

Address	Contents
0002	0000 0000
0003	0001 0110

FIGURE 3 – FORMAT FOR PROGRAMMING GENERAL OPTIONS

ORGANIZATIONAL DATA
MCM68A332 MOS READ ONLY MEMORY

Customer:

Company _____

Part No. _____

Originator _____

Phone No. _____

Motorola Use Only

Quote _____

Part No. _____

Specif. No. _____

Chip Select Options:	Active High	Active Low	No-Connect
S1	☐	☐	☐
S2	☐	☐	☐

MOTOROLA

MCM68A364
MCM68B364

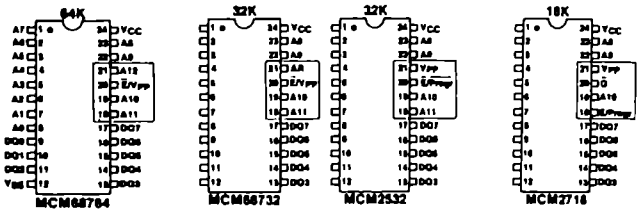
8192 X 8-BIT READ ONLY MEMORY

The MCM68A364/MCM68B364 is a mask-programmable byte-organized memory designed for use in bus-organized systems. It is fabricated with N-channel silicon-gate technology. For ease of use, the device operates from a single power supply, and has compatibility with TTL. The addresses are latched with the Chip Enable input — no external latches required.

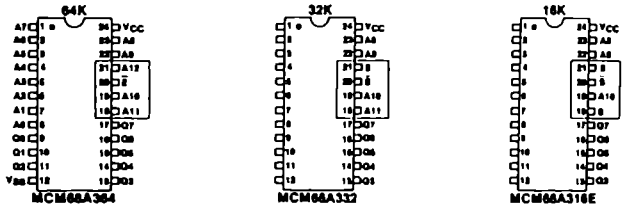
The memory is compatible with the M6800 Microcomputer Family, providing read only storage in byte increments. The Chip Enable input deselects the output and puts the chip in a power-down mode.

- Automatic Power Down
- Low Power Dissipation — 150 mW active (typical)
  35 mW standby (typical)
- Single ±10% 5-Volt Power Supply
- High Output Drive Capability (2 TTL Loads)
- Three-State Data Output for OR-Ties
- TTL Compatible
- Maximum Access Time — 250 ns — MCM68B364
  350 ns — MCM68A364
- Pin Compatible with 8K — MCM68A308, 16K — MCM68A316E, and 32K — MCM68A332 Mask-Programmable ROMs
- Pin Compatible with 24-pin 64K EPROM MCM68764

MOTOROLA'S PIN-COMPATIBLE EPROM FAMILY



MOTOROLA'S PIN-COMPATIBLE ROM FAMILY

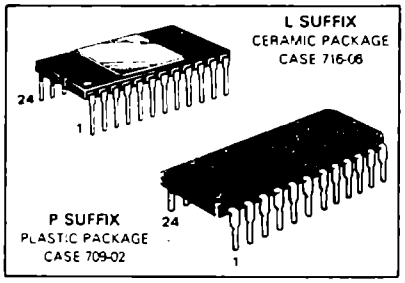


INDUSTRY STANDARD PINOUTS

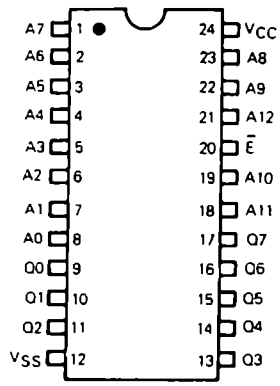
MOS

(N-CHANNEL, SILICON-GATE)

8192 X 8-BIT
READ ONLY MEMORY



PIN ASSIGNMENT

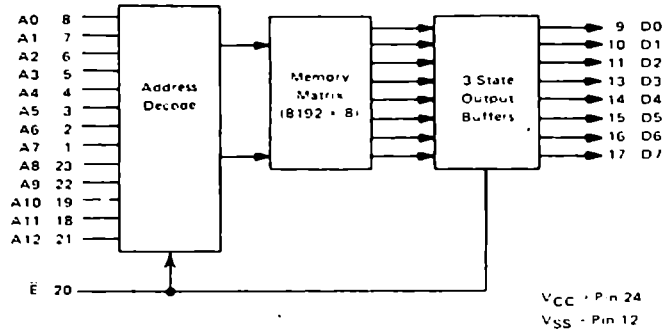


PIN NAMES	
A0 A12	Address
Ē	Chip Enable
Q0 Q7	Data Output
V_{CC}	+5 V Power Supply
V_{SS}	Ground

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

DS9805/7-79

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (See note)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.5 to +7.0	Vdc
Input Voltage	V_{in}	−0.5 to +7.0	Vdc
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

NOTE Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted.)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Nom	Max	Unit
Supply Voltage (V_{CC} must be applied at least 100 μs before proper device operation is achieved)	V_{CC}	4.5	5.0	5.5	Vdc
Input High Voltage	V_{IH}	2.0		5.5	Vdc
Input Low Voltage	V_{IL}	−0.5	–	0.8	Vdc

RECOMMENDED OPERATING CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
Input Current (V_{in} = 0 to 5.5 V)	I_{in}	10	–	10	μAdc
Output High Voltage (I_{OH} = −220 μA)	V_{OH}	2.4	–	–	Vdc
Output Low Voltage (I_{OL} = 3.2 mA)	V_{OL}	–	–	0.4	Vdc
Output Leakage Current (Three State) ($\overline{E}$ = 2.0 V, V_{out} = 0 V to 5.5 V)	I_{LO}	−10	–	10	μAdc
Supply Current — Active* (Minimum Cycle Rate)	I_{CC}	–	25	40	mAdc
Supply Current — Standby ($\overline{E}$ = V_{IH})	I_{SB}		7	10	mAdc

*Current is proportional to cycle rate

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, periodically sampled rather than 100% tested)

Characteristic	Symbol	Max	Unit
Input Capacitance	C_{in}	8	pF
Output Capacitance	C_{out}	15	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

Read Cycle

RECOMMENDED OPERATING CONDITIONS

(T_A = 0 to 70°C, V_{CC} = 5.0 V ± 10%. All timing with t_r = t_f = 20 ns, load of Figure 1)

Parameter	Symbol	MCM68B364		MCM68A364		Unit
		Min	Max	Min	Max	
Chip Enable Low to Chip Enable Low of Next Cycle (Cycle Time)	tELEL	375		450		ns
Chip Enable Low to Chip Enable High	tELEH	250		300		ns
Chip Enable Low to Output Valid (Access)	tELQV	–	250	–	300	ns
Chip Enable High to Output High Z (Off Time)	tEHQZ	–	60	–	75	ns
Chip Enable Low to Address Don't Care (Hold)	tELAX	60	–	75	–	ns
Address Valid to Chip Enable Low (Address Setup)	tAVEL	0	–	0	–	ns
Chip Enable Precharge Time	tEHEL	125	–	150	–	ns

TIMING DIAGRAM

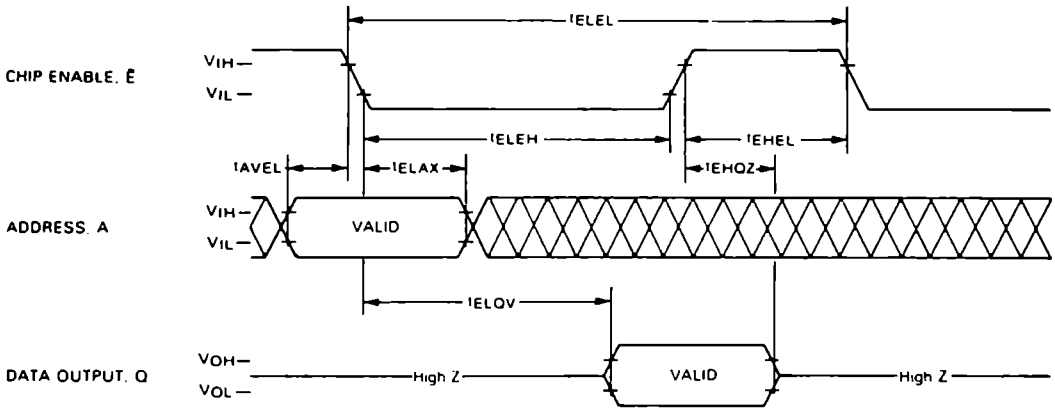
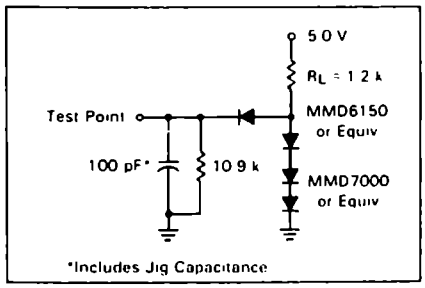
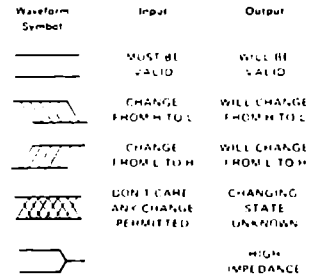


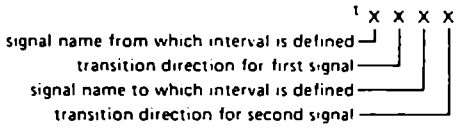
FIGURE 1 – AC TEST LOAD



WAVEFORMS



TIMING PARAMETER ABBREVIATIONS


t X X X X
signal name from which interval is defined
transition direction for first signal
signal name to which interval is defined
transition direction for second signal

The transition definitions used in this data sheet are:

H = transition to high
L = transition to low
V = transition to valid
X = transition to invalid or don't care
Z = transition to off (high impedance)

TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

CUSTOM PROGRAMMING

By the programming of a single photomask for the MCM68A364/MCM68B364, the customer may specify the contents of the memory.

Information for custom memory content may be sent to Motorola in one of two forms (shown in order of preference):

1. Magnetic Tape – 9 Track, 800 bpi, odd parity written in EBCDIC character code. Motorola's R.O.M.S. format
2. EPROMs – one 64K (MCM68764), two 32K (MCM2532), four 16K (MCM2716 or TMS2716), or eight 8K (MCM2708)
3. IBM Punch Cards
   - A. Hexadecimal Format
   - B. INTEL Hexadecimal Format

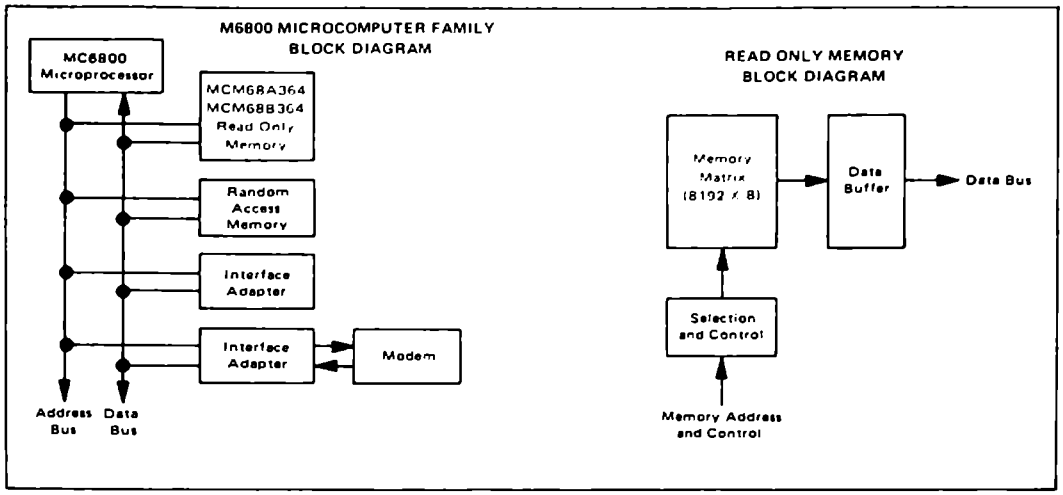
IBM PUNCH CARDS, HEXADECIMAL FORMAT

The hexadecimal equivalent (from Figure 2) may be placed on 80 column IBM punch cards as follows.

Step	Column	
1	12	Byte "0" Hexadecimal equivalent for outputs Q7 through Q4 (Q7 = M.S.B.)
2	13	Byte "0" Hexadecimal equivalent for outputs Q3 through Q0 (Q3 = M.S.B.)
3	14-75	Alternate steps 1 and 2 for consecutive bytes
4	77-79	Card number (starting 001)
5		Total number of cards must equal 256

FIGURE 2 – BINARY TO HEXADECIMAL CONVERSION

Binary Data				Hexadecimal Character
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	A
1	0	1	1	B
1	1	0	0	C
1	1	0	1	D
1	1	1	0	E
1	1	1	1	F



PRE-PROGRAMMED MCM68A364P3/L3

The -3 standard ROM pattern contains log (base 10) and antilog (base 10) lookup tables for the 64K ROM.

Locations 0000 through 3599 contain log base 10 values. The arguments for the log table range from 1.00 through 9.99 incrementing in steps of 1/100. Each log value is represented by an eight-digit decimal number with decimal point assumed to be to the left of the most-significant digit.

Antilog (base 10) are stored in locations 4096 through 8095. The arguments range from .000 through .999 incrementing in steps of 1/1000. Each antilog value is represented by an eight-digit decimal number with decimal point assumed to be to the right of the most-significant digit.

Locations 3600 through 4095 and 8096 through 8191 are zero filled.

All values are represented in absolute decimal format with eight digit precision. They are stored in BCD format with the two most significant digits in the lower byte and the remaining six digits in the three consecutive locations.

Example

$\log_{10}(1.01) = .00432137$ decimal

Address	Contents	
4	0000	0000
5	0100	0011
6	0010	0001
7	0011	0111

MOTOROLA

MCM68365

Advance Information

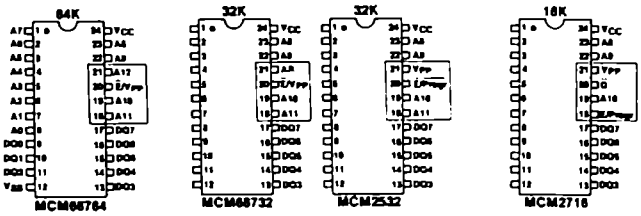
8192 × 8-BIT READ ONLY MEMORY

The MCM68365 is a mask-programmable byte-organized memory designed for use in bus-organized systems. It is fabricated with N-channel silicon-gate technology. For ease of use, the device operates from a single power supply, has compatibility with TTL, and needs no clocks or refreshing because of static operation.

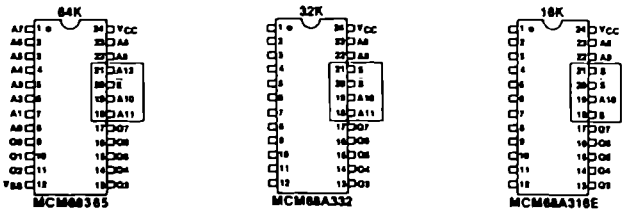
The memory is compatible with the M6800 Microcomputer Family, providing read only storage in byte increments. The active level of the Chip Enable input and the memory content is defined by the user. The Chip Enable input deselects the output and puts the chip in a power-down mode.

- Fully Static Operation
- Automatic Power Down
- Low Power Dissipation – 225 mW Active (Typical)
  30 mW Standby (Typical)
- Single ± 10% 5-Volt Power Supply
- High Output Drive Capability (2 TTL Loads)
- Three-State Data Output for OR-Ties
- Mask Programmable Chip Enable
- TTL Compatible
- Maximum Access Time – 250 ns – MCM68365-25
  350 ns – MCM68365-35
- Pin Compatible with 8K – MCM68A308, 16K – MCM68A316E, and 32K – MCM68A332 Mask-Programmable ROMs

MOTOROLA'S PIN-COMPATIBLE EPROM FAMILY



MOTOROLA'S PIN-COMPATIBLE ROM FAMILY

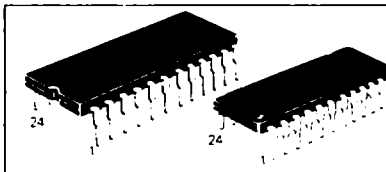


INDUSTRY STANDARD PINOUTS

MOS

(N-CHANNEL, SILICON-GATE)

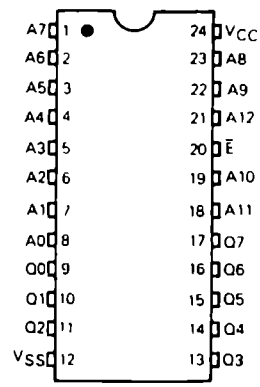
8192 × 8-BIT
READ ONLY MEMORY



C SUFFIX
FRIT-SEAL
CERAMIC PACKAGE
CASE 623

P SUFFIX
PLASTIC PACKAGE
CASE 709

PIN ASSIGNMENT

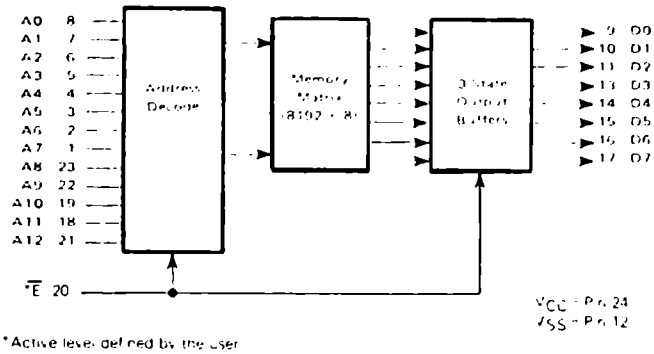


PIN NAMES	
A0-A12	Address
Ē	Chip Enable
O0-O7	Data Output
V_{CC}	+5 V Power Supply
V_{SS}	Ground

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields, however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

ADI844/9-80

BLOCK DIAGRAM



*Active level defined by the user

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3 to +7.0	V
Input Voltage	V_{in}	-0.3 to +7.0	V
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Nom	Max	Unit
Supply Voltage (V_{CC} must be applied at least 100 µs before proper device operation is achieved)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.0	–	5.5	V
Input Low Voltage	V_{IL}	-0.3	–	0.8	V

RECOMMENDED OPERATING CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
Input Current (V_{in} = 0 to 5.5 V)	I_{in}	–	–	10	µA
Output High Voltage (I_{OH} = – 205 µA)	V_{OH}	2.4	–	–	V
Output Low Voltage (I_{OL} = 3.2 mA)	V_{OL}	–	–	0.4	V
Output Leakage Current (Three-State) ($\overline{E}$ = 2.0 V, V_{out} = 0.4 V to 2.4 V)	I_{LO}	–	–	10	µA
Supply Current – Active (V_{CC} = 5.5 V, T_A = 0°C)	I_{CC}	–	45	80	mA
Supply Current – Standby (V_{CC} = 5.5 V, T_A = 0°C, $\overline{E}$ = V_{IH})	I_{SB}	–	6.0	15	mA

CAPACITANCE

(f = 1.0 MHz, T_A = 25°C, periodically sampled rather than 100% tested)

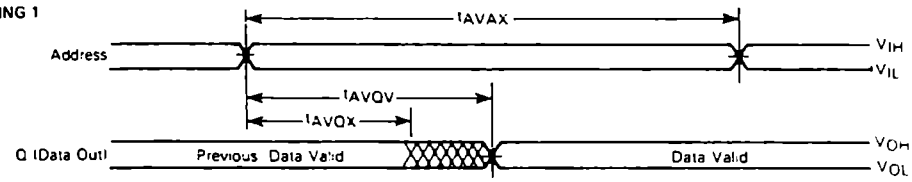
Characteristic	Symbol	Max	Unit
Input Capacitance	C_{in}	7.5	pF
Output Capacitance	C_{out}	12.5	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS
Read Cycle

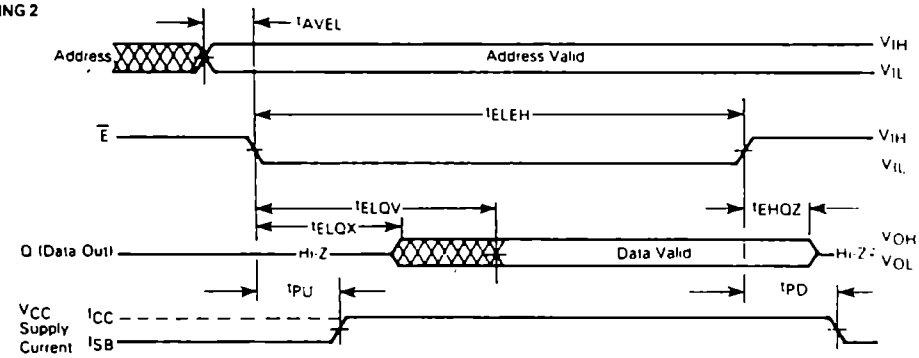
RECOMMENDED OPERATING CONDITIONS
(T_A = 0 to 70°C, V_{CC} = 5.0 V ± 10%. All timing with $t_r = t_f$ = 10 ns, load of Figure 1)

Parameter	Symbol	MCM68365-25		MCM68365-35	
		Min	Max	Min	Max
Address Valid to Address Don't Care (Cycle Time when Chip Enable is held Active)	t_{AVAX}	250	–	350	–
Chip Enable Low to Chip Enable High	t_{ELEH}	250	–	350	–
Address Valid to Output Valid (Access)	t_{AVQV}	–	250	–	350
Chip Enable Low to Output Valid (Access)	t_{ELQV}	–	250	–	350
Address Valid to Output Invalid	t_{AVQX}	10	–	10	–
Chip Enable Low to Output Invalid	t_{ELQX}	10	–	10	–
Chip Enable High to Output High-Z	t_{EHQZ}	0	70	0	80
Chip Selection to Power Up Time	t_{PU}	0	–	0	–
Chip Deselection to Power Down Time	t_{PD}	–	100	–	120
Address Valid to Chip Enable Low (Address Setup)	t_{AVEL}	0	–	0	–

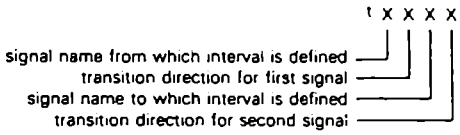
READ CYCLE TIMING 1
(E Held Low)



READ CYCLE TIMING 2



TIMING PARAMETER ABBREVIATIONS

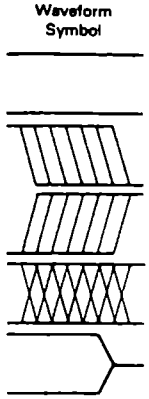

t X X X X
signal name from which interval is defined
transition direction for first signal
signal name to which interval is defined
transition direction for second signal

The transition definitions used in this data sheet are:
- H = transition to high
- L = transition to low
- V = transition to valid
- X = transition to invalid or don't care
- Z = transition to off (high impedance)

TIMING LIMITS

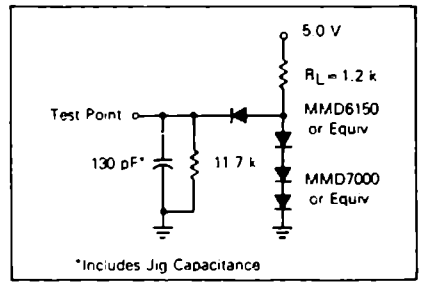
The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

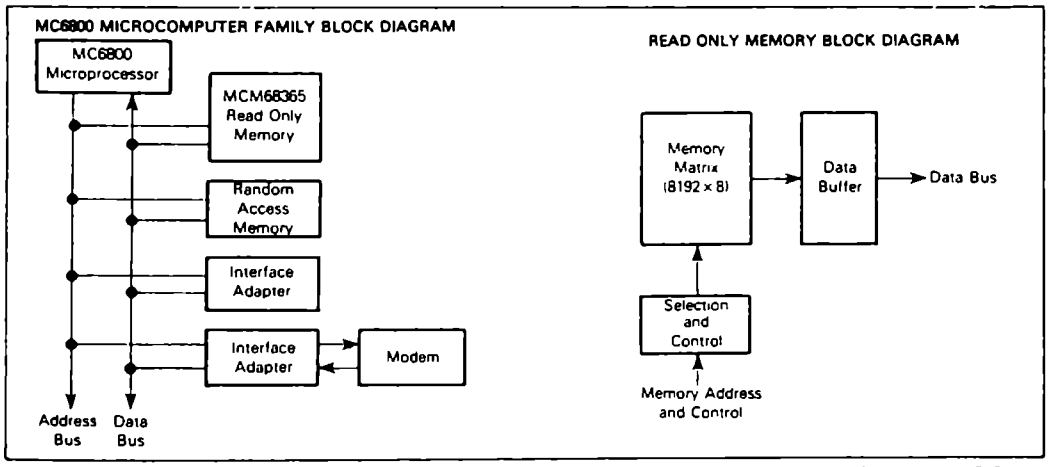
WAVEFORMS



Waveform Symbol	Input	Output
	Must Be Valid	Will Be Valid
	Change From H to L	Will Change From H to L
	Change From L to H	Will Change From L to H
	Don't Care Any Change Permitted	Changing State Unknown
	—	High Impedance

FIGURE 1 – AC TEST LOAD





PRE-PROGRAMMED MCM68365P35-3/C35-3, MCM68365P25-3/C25-3

The –3 standard ROM pattern contains log (base 10) and antilog (base 10) lookup tables for the 64K ROM.

Locations 0000 through 3599 contain log base 10 values. The arguments for the log table range from 1.00 through 9.99 incrementing in steps of 1/100. Each log value is represented by an eight-digit decimal number with decimal point assumed to be to the left of the most-significant digit.

Antilog (base 10) are stored in locations 4096 through 8095. The arguments range from .000 through .999 incrementing in steps of 1/1000. Each antilog value is represented by an eight-digit decimal number with decimal point assumed to be to the right of the most-significant digit.

Locations 3600 through 4095 and 8096 through 8191 are zero filled.

All values are represented in absolute decimal format with eight digit precision. They are stored in BCD format with the two most significant digits in the lower byte and the remaining six digits in the three consecutive locations.

Example: $\log_{10}(1.01) = 0.00432137$ decimal

Address	Contents	
4	0000	0000
5	0100	0011
6	0010	0001
7	0011	0111

CUSTOM PROGRAMMING

By the programming of a single photomask for the MCM68365, the customer may specify the content of the memory and the method of enabling the outputs.

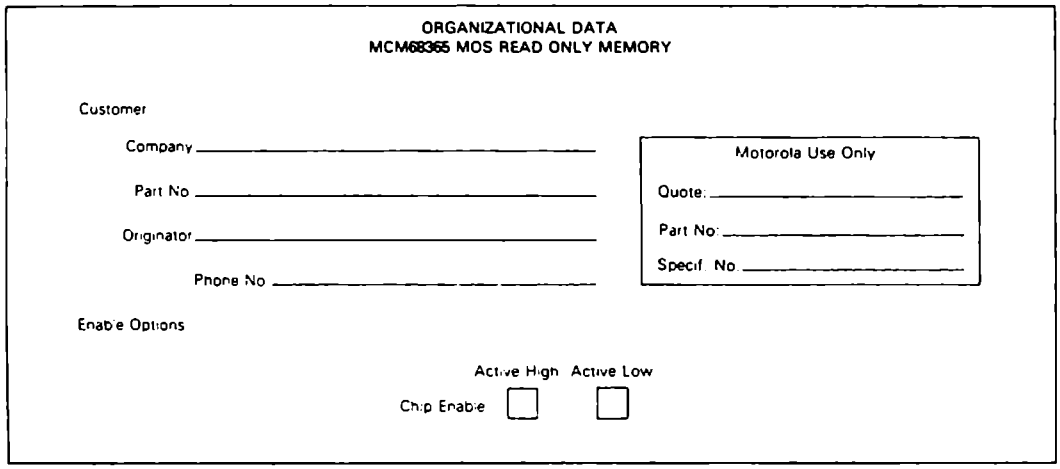
Information on the general options of the MCM68365 should be submitted on an Organizational Data form such as that shown in Figure 2.

Information for custom memory content may be sent to Motorola in one of two forms (shown in order of preference):

1 Magnetic Tape
9 track, 800 bpi, odd parity written in EBCDIC character code. Motorola R O.M.S. format.

2 EPROMs – four 16K (MCM2716, or TMS2716, or eight 8K (MCM2708), one 64K or two 32K)

FIGURE 2 – FORMAT FOR PROGRAMMING GENERAL OPTIONS



MOTOROLA

MCM68366

Advance Information

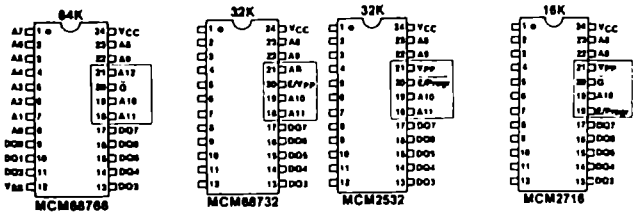
8192 × 8-BIT READ ONLY MEMORY

The MCM68366 is a mask-programmable byte-organized memory designed for use in bus-organized systems. It is fabricated with N-channel silicon-gate technology. For ease of use, the device operates from a single power supply, has compatibility with TTL and DTL, and needs no clocks or refreshing because of static operation.

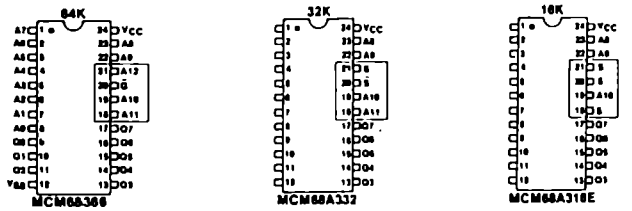
The memory is compatible with the M6800 Microcomputer Family, providing read only storage in byte increments. The active level of the Output Enable input and the memory content is defined by the user. The Output Enable input deselects the output.

- Fully Static Operation
- Fast Data Valid Time for High Speed Microprocessors
- Low Power Dissipation — 225 mW Active (Typical)
- Single ± 10% 5-Volt Power Supply
- High Output Drive Capability (2 TTL Loads)
- Three-State Data Output for OR-Ties
- Mask Programmable Output Enable
- TTL Compatible
- Maximum Access Time — 120 ns from Output Enable
  250 ns from Address — MCM68366-25
  350 ns from Address — MCM68366-35
- Pin Compatible with 8K and 32K — Mask-Programmable ROMs
- Pin Compatible with MCM68766 64K EPROM

MOTOROLA'S PIN-COMPATIBLE EPROM FAMILY



MOTOROLA'S PIN-COMPATIBLE ROM FAMILY

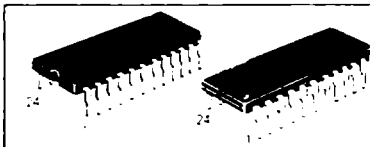


INDUSTRY STANDARD PINOUTS

MOS

(N-CHANNEL SILICON-GATE)

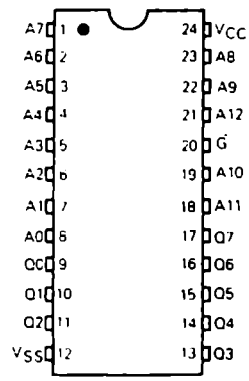
8192 × 8-BIT
READ ONLY MEMORY



C SUFFIX
FRIT SEAL
CERAMIC PACKAGE
CASE 623

P SUFFIX
PLASTIC PACKAGE
CASE 709

PIN ASSIGNMENT

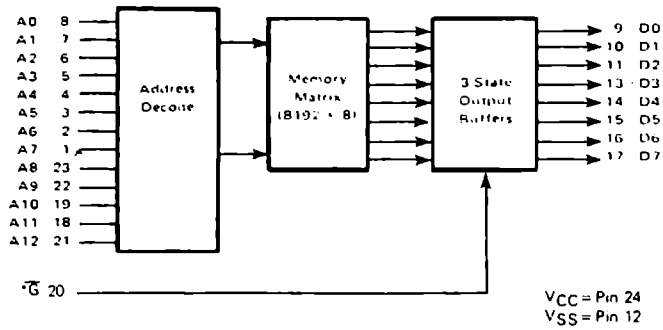


PIN NAMES	
A0-A12	Address
$\overline{G}$	Output Enable
Q0-Q7	Data Output
V_{CC}	+5 V Power Supply
V_{SS}	Ground

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

ADI842/9-80

BLOCK DIAGRAM



*Active Level Defined by the User

ABSOLUTE MAXIMUM RATINGS (See Note 1)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	Vdc
Input Voltage	V_{in}	−0.3 to +7.0	Vdc
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

NOTE 1: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Nom	Max	Unit
Supply Voltage (V_{CC} must be applied at least 100 μs before proper device operation is achieved)	V_{CC}	4.5	5.0	5.5	Vdc
Input High Voltage	V_{IH}	2.0	–	5.5	Vdc
Input Low Voltage	V_{IL}	−0.3	–	0.8	

RECOMMENDED OPERATING CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
Input Current (V_{in} = 0 to 5.5 V)	I_{in}	–	–	10	μAdc
Output High Voltage (I_{OH} = −205μA)	V_{OH}	2.4	–	–	Vdc
Output Low Voltage (I_{OL} = 3.2 mA)	V_{OL}	–	–	0.4	Vdc
Output Leakage Current (Three-State) ($\overline{G}$ = 2.0 V, V_{out} = 0.4 V to 2.4 V)	I_{LO}	–	–	10	μAdc
Supply Current (V_{CC} = 5.5 V, T_A = 0°C)	I_{CC}	–	45	80	mAdc

CAPACITANCE

(f = 1.0 MHz, T_A = 25°C, periodically sampled rather than 100% tested)

Characteristic	Symbol	Max	Unit
Input Capacitance	C_{in}	7.5	pF
Output Capacitance	C_{out}	12.5	pF

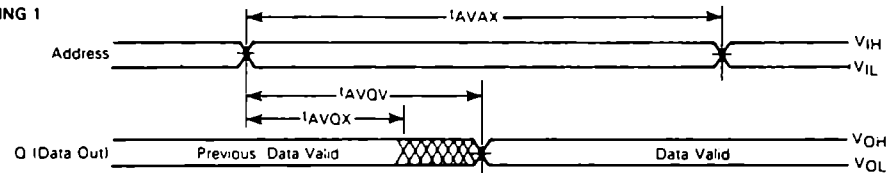
AC OPERATING CONDITIONS AND CHARACTERISTICS
Read Cycle

RECOMMENDED OPERATING CONDITIONS

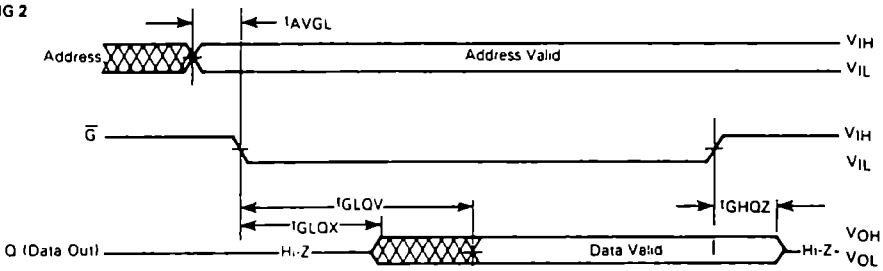
(T_A = 0 to 70°C, V_{CC} = 5.0 V ± 10%. All timing with t_t = t_f = 10 ns, load of Figure 1)

Parameter	Symbol	MCM68366-25		MCM68366-35		Unit
		Min	Max	Min	Max	
Address Valid to Address Don't Care (Cycle Time when Output Enable is Held Active)	t_{AVAX}	250	–	350	–	ns
Address Valid to Output Valid (Access)	t_{AVQV}	–	250	–	350	ns
Output Enable Low to Output Valid (Access)	t_{GLQV}	–	120	–	120	ns
Address Valid to Output Invalid	t_{AVQX}	10	–	10	–	ns
Output Enable Low to Output Invalid	t_{GLQX}	10	–	10	–	ns
Output Enable High to Output High-Z	t_{GHZQ}	0	70	0	80	ns
Address Valid to Output Enable Low (Address Set-up)	t_{AVGL}	0	–	0	–	ns

READ CYCLE TIMING 1
($\overline{G}$ Held Low)



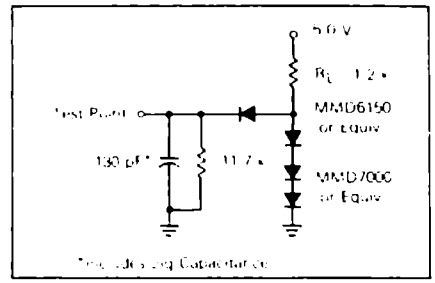
READ CYCLE TIMING 2



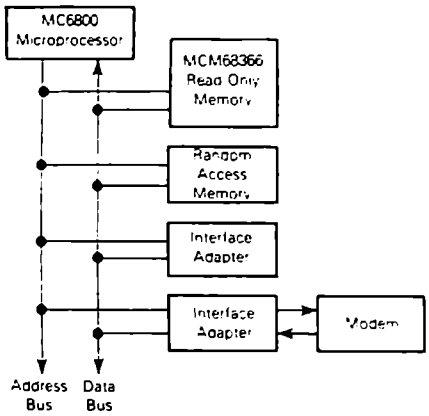
WAVEFORMS

Waveform Symbol	Input	Output
	Must Be Valid	Will Be Valid
	Change From H to L	Will Change From H to L
	Change From L to H	Will Change From L to H
	Don't Care: Any Change Permitted	Changing State Unknown
	—	High Impedance

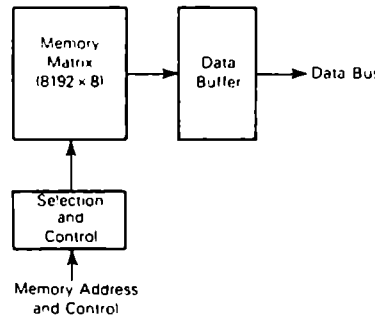
FIGURE 1 – AC TEST LOAD



MC6800 MICROCOMPUTER FAMILY BLOCK DIAGRAM



READ ONLY MEMORY BLOCK DIAGRAM



PRE-PROGRAMMED MCM68366P35-3/C35-3, MCM68366P25-3/C25-3

The –3 standard ROM pattern contains log (base 10) and antilog (base 10) lookup tables for the 64K ROM.

Locations 0000 through 3599 contain log base 10 values. The arguments for the log table range from 1.00 through 9.99 incrementing in steps of 1/100. Each log value is represented by an eight-digit decimal number with decimal point assumed to be to the left of the most-significant digit.

Antilog (base 10) are stored in locations 4096 through 8095. The arguments range from 0.000 through 0.999 incrementing in steps of 1/1000. Each antilog value is represented by an eight-digit decimal number with decimal point assumed to be to the right of the most-significant digit.

Locations 3600 through 4095 and 8096 through 8191 are zero filled.

All values are represented in absolute decimal format with eight digit precision. They are stored in BCD format with the two most significant digits in the lower byte and the remaining six digits in the three consecutive locations.

Example: $\log_{10}(1.01) = .00432137$ decimal

Address	Contents	
4	0000	0000
5	0100	0011
6	0010	0001
7	0011	0111

CUSTOM PROGRAMMING

By the programming of a single photomask for the MCM68366, the customer may specify the content of the memory and the method of enabling the outputs.

Information on the general options of the MCM68366 should be submitted on an Organizational Data form such as that shown in Figure 3.

Information for custom memory content may be sent to Motorola in one of two forms (shown in order of preference):

1. Magnetic Tape
   9 track, 800 bpi, odd parity written in EBCDIC character Code. Motorola's R O M S format.
2. EPROMs – one 64K (MCM68764, MCM68766), two 32K (MCM2532), four 16K (MCM2716, or TMS2716), or eight 8K (MCM2708).

FIGURE 3 – FORMAT FOR PROGRAMMING GENERAL OPTIONS

ORGANIZATIONAL DATA
MCM68366 MOS READ ONLY MEMORY

Customer

Company _____

Part No _____

Originator _____

Phone No _____

Motorola Use Only

Quote _____

Part No _____

Specif. No _____

Enable Options

	Active High	Active Low
Output Enable	☐	☐

MOTOROLA Semiconductors

MCM2802

Advance Information

MOS

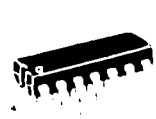
(N-CHANNEL, SILICON GATE)

32 X 32 BIT
ELECTRICALLY ERASABLE PROM

32 X 32 BIT SERIAL ELECTRICALLY ERASABLE PROM

The MCM2802 is a 1K-bit serial Electrically Erasable PROM designed for applications requiring both non-volatile memory and in-system information updates. In digital tuning systems, it provides storage for up to 32 channels. It has external control of timing functions and serial format for data and address.

- Single 5V supply in Read mode
- 5V and 25V supply for Erase and Program
- In-System Program/Erase Capability
- 0-100kHz clock rate
- Floating gate process
- Expandable to 16K-bit systems
- Word and Array erasable

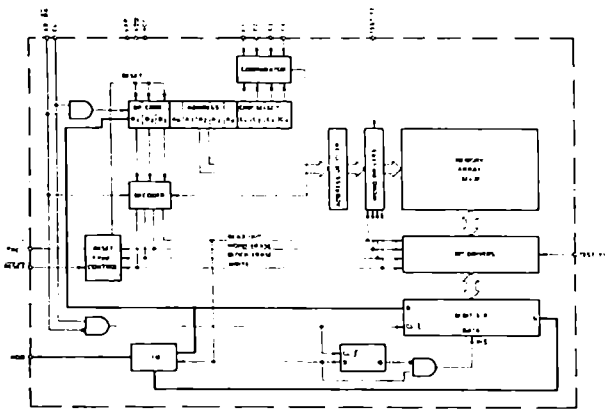


L SUFFIX
CERAMIC PACKAGE
CASE 632.06

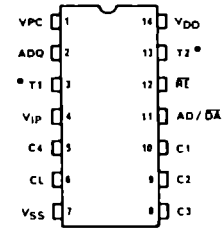
P SUFFIX

PLASTIC PACKAGE ALSO AVAILABLE
CASE 646.05

FIGURE 1 – BLOCK DIAGRAM



PIN ASSSIGNMENT



* For normal operation, hardwired to V_{SS}

PIN NAMES

VPC	Program Voltage Control
ADQ	Address Input + Data Input/Output
T1, T2	Margin Testing
C1, C2, C3, C4	Chip Address 1 to 4
CL	Clock
$\overline{RE}$	Reset
AD/$\overline{DA}$	Shift Register Select

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

This is advance information and specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (Voltages referred to V_{SS})

Rating	Symbol	Min	Max	Unit
DC Supply Voltage	V_{DD}	−0,5	8	Vdc
Programming Voltage	V_{PP}	−0.5	28	Vdc
Input Voltage	V_{IN}	−0.5	8	Vdc
VP Control Output	V_{PC}	−0.5	28	Vdc
Operating Temperature Range	T_A	−40	85	°C
Storage Temperature Range	T_{STC}	−55	150	°C

NOTE – Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

SWITCHING CHARACTERISTICS ($T_A = 0 \ldots 70\,°C$; $V_{DD} = 5V \pm 10\,\%$; $V_P = 24.5V \pm 1.5\,V$

Pin	Symbol	Parameter	Fig No	Min	Max	Unit
	t_{ER}	Erase time		100		ms
	t_{WR}	Write time		10		ms
CL	F_{CL}	Clock Frequency $F_{CL} = 1/T_{CL}$	2		100	kHz
CL	t_{CLH}	Clock High Level Hold Time	2	4		µs
CL	t_{CLL}	Clock Low Level Hold Time	2	4		µs
CL	t_{CLRF}	Clock Fall Time and Rise Time	2		1	µs
AD/DA	$t_{AD/DA}$	Register Control to Clock Delay Time except for t_{READ}	2	1		µs
	t_{READ}	After READ opcode only	3	2	100	µs
I/O	t_{DSUP}	Data In Set-Up	2, 3	2		µs
	t_{DH}	Data In Hold	2, 3	0.1		µs
I/O	t_{DOUTS}	Data Out Serial Delay	3		1	µs
	t_{DOUTP}	Data Out Parallel Delay	3		3	µs
O	C_{out}	Output Capacitance ($V_{out} = 0\,V$)			12	pF

DC CHARACTERISTICS (T_A = 0 . . . 70 °C; V_{DD} = 5V ± 10 %; V_P = 24.5V ± 1.5 V

Pin	Characteristic	Condition	Symbol	Min	Max	Unit
V_{PP}	Supply Current		I_{PP}		3	mA
V_{DD}	Supply Current		I_{DD}		20	mA
I/O	Tristate Input/	V_{OH} = 2.4V	I_{OH}	− 0.1		mA
	Output	V_{OL} = 0.5V	I_{OL}	1.6		mA
		Tristate	I_{IN}		10	µA
All Inputs Except I/O	Input Leakage		I_{IN}		10	µA
V_{PC}	VP Control Pull down device	V_{ON} = 1V	I_{ON}	0.7		mA
		OFF state	V_{MAX}		V_{PP}	
		V_{OFF} = VP	I_{OFF}		10	µA
All Inputs	Input Low Voltage	V_{IL}			0.8	V
	Input High Voltage	V_{IH}		2.4		V

FIGURE 2 – GENERAL TIMINGS

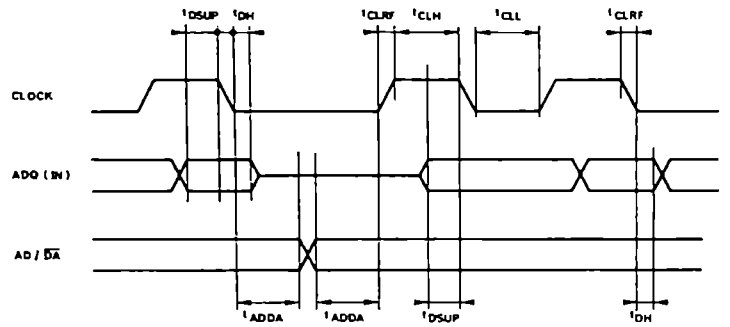
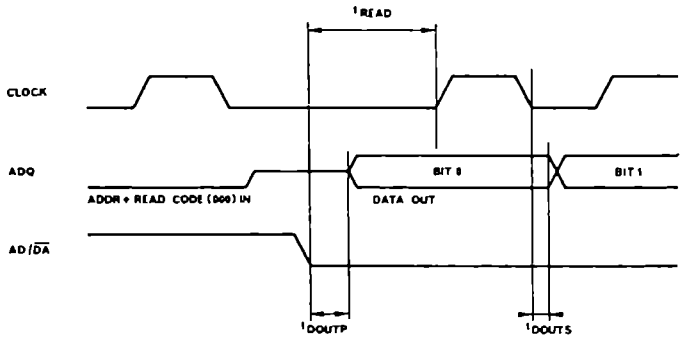


FIGURE 3 – READOUT TIMINGS



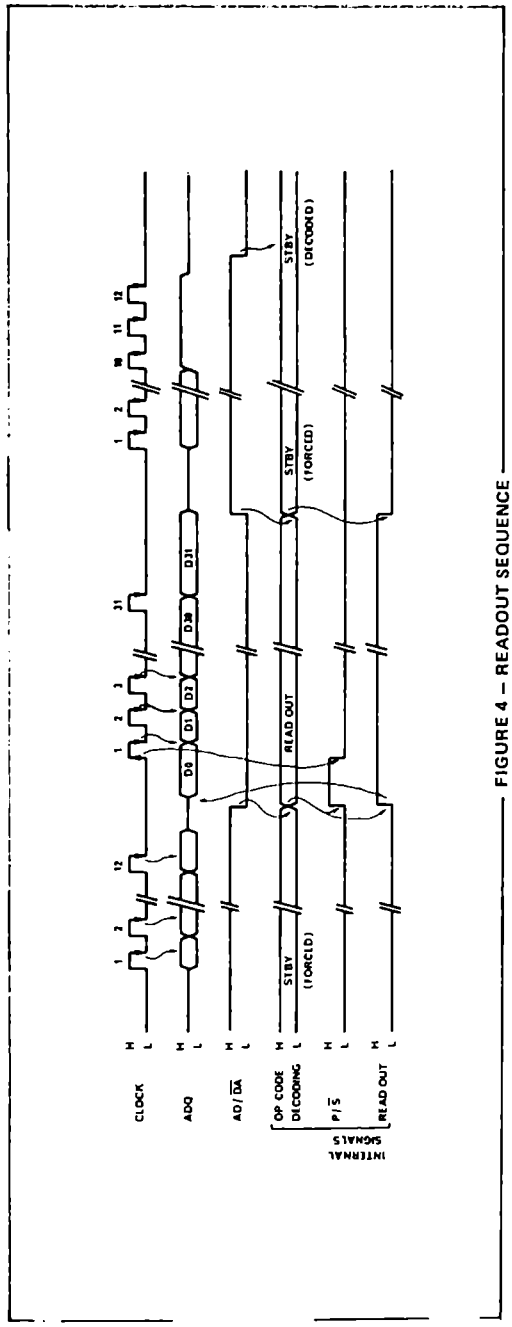


FIGURE 4 – READOUT SEQUENCE

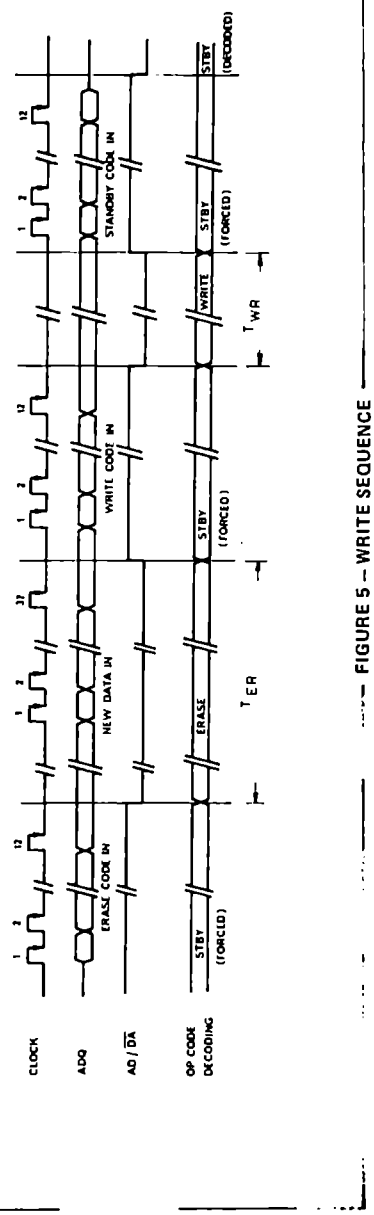


FIGURE 5 – WRITE SEQUENCE

FUNCTIONAL DESCRIPTION

The circuit accepts 12 bits of Address/Op code in the address register and 32 bits of data in the data register (see figure 1: Block diagram).

Address/Op code format (figure 1)

The four shifted bits C1 to C4 are used as chip select word in multichip systems. The chip address is defined by hardwiring the C1 to C4 pins. These bits are adjacent to the address field, so that no software modification is required in a program designed for a multi-1K memory application.

The five following A1 to A5 bits select one of the word addresses. The last 3 bits 01 to 03 control the operating modes.

Function	01	02	03
Read	0	0	0
Word Erase	0	1	0
Block Erase	1	1	0
Write	1	0	0
Standby	X	X	1

Read operation (figure 4)

1) The ADDRESS/OP CODE is loaded. The address selecting the word to be read and the op code bits being the READ code.

2) The AD/$\overline{DA}$ is switched to the data mode, thus initiating the parallel transfer from the core to the shift register. First bit of data is present at the output.

3) As soon as the first of the 31 data out clock pulses is applied, the parallel transfer is stopped and data is shifted at the output. Data is recirculated in the data register.

4) The output buffer is turned on only, when READ is internally decoded, AD/$\overline{DA}$ is low and chip is selected by C1 and C4. Otherwise it is in the high impedance state.

Addresses and data are clocked in and out with the falling edge of block.

Writing (figure 5)

1) ADDRESS/OP CODE is shifted in, the op code being either BLOCK ERASE or WORD ERASE

2) Switching the AD/$\overline{DA}$ line low for t = t_{ERASE} initiates the erase process. During this period of time, a data word can be shifted into the data register.

3) Then the WRITE code and the same address is loaded to the address register.

4) The AD/$\overline{DA}$ line is switched low again for a t = t_{WRITE}, during which the selected word is programmed.

5) At the end of the WRITE operation it is recommended to load op code STANDBY and to return input AD/$\overline{DA}$ to the low state.

Erase

Both BLOCK ERASE and WORD ERASE are provided and are controlled by the op code. V_{PP} has to be applied for BLOCK ERASE, WORD ERASE and for WRITE. For all other conditions it can be switched off to high impedance or V_{DD} or V_{SS}.

Standby

When AD/$\overline{DA}$ is high, the instruction decoder is disabled and hence STANDBY is forced. By shifting the STANDBY op code into the address register, STANDBY will be recognized independently of the state of AD/$\overline{DA}$.

Clock

The active high clock is only used for shifting data and addresses. This shift occurs on the clock falling edge.

Chip selection

The ADDRESS/DATA line can be used as a chip select in a system having other serial I/O devices DATA and CLOCK lines being shared the non-volatile memory is only activated when the AD/$\overline{DA}$ line is low. Shifting information to the data register has no effect to the core while the chip is deselected.

In a multi-memory arrangement, all the lines including ADDRESS/DATA, CLOCK and DATA, are shared, with the exception of C1 to C4 which are hardwired to V_{DD} or V_{SS}, thus defining the circuit address. All V_P control outputs of the memory circuits can be combined in a wired OR configuration.

Data protection

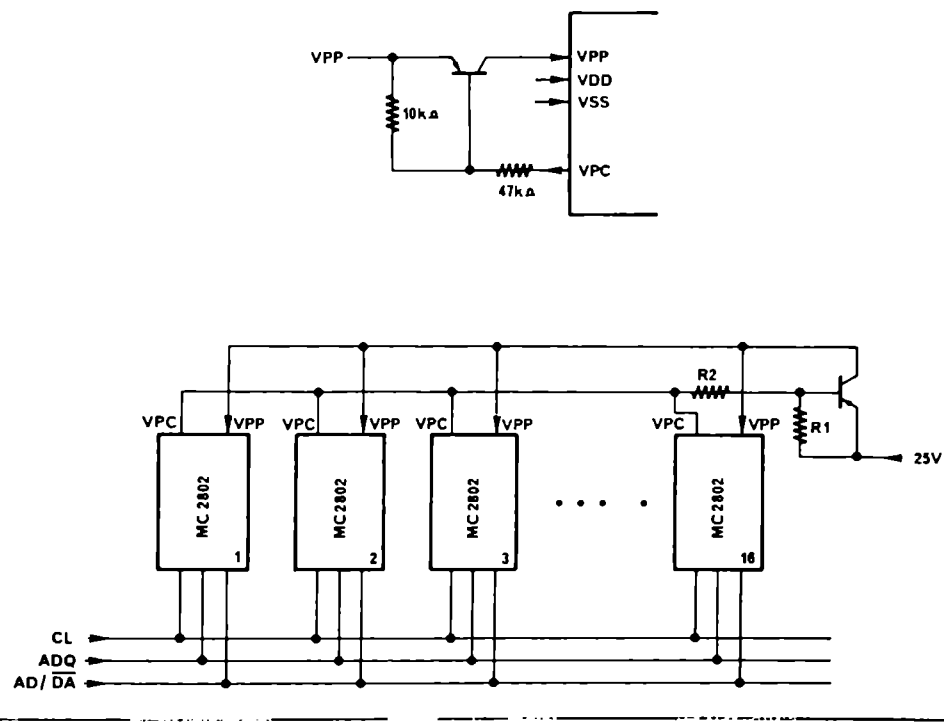
When V_{PP} is turned off, data stored in the array is always protected. A V_{PP} control output is provided for switching the V_{PP} supply. It consists of a pull down device to V_{SS}. This device is turned on only when : V_{DD} is present, a WRITE or ERASE code has been loaded in the address register *and* AD/$\overline{DA}$ is low.

Schematics for this external V_{PP} control are proposed in figure 6.

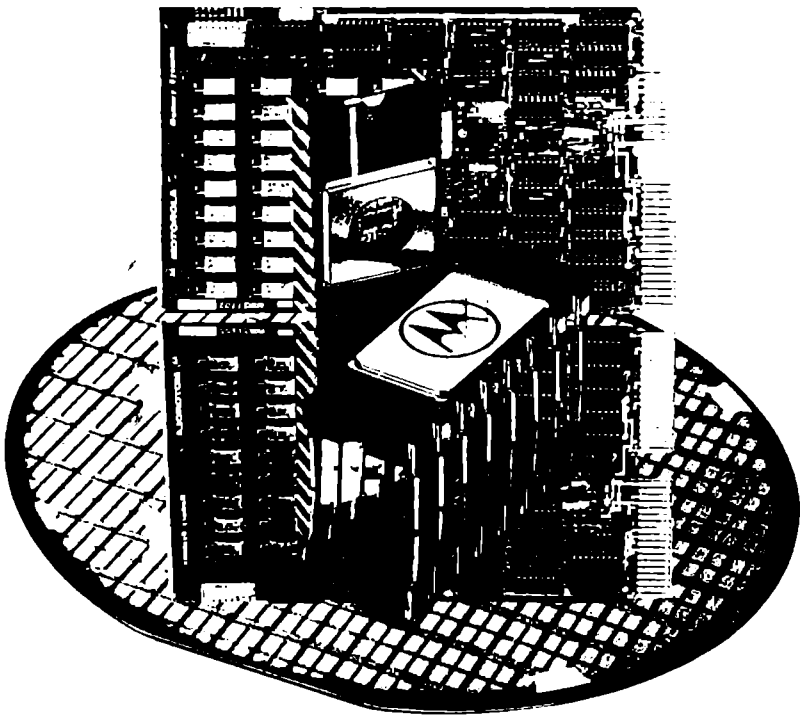
Reset

V_{PP} and V_{DD} may be turned on or off in any sequence without disturbing data in the NVM array. During power-up, the op code is preset to the standby mode. The $\overline{RESET}$ input can be connected to the system $\overline{RESET}$.

FIGURE 6 – Vpp CONTROL AND MULTICHIP SETUP



CMOS Memories
RAM, ROM



MOTOROLA

MCM14505

CMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

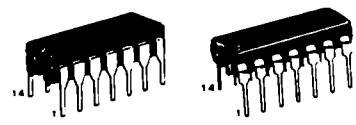
64-BIT (64 x 1) STATIC RANDOM ACCESS MEMORY

64-BIT STATIC RANDOM ACCESS MEMORY

The MCM14505 64-bit random access memory is fully decoded on the chip and organized as 64 one-bit words (64 X 1). Medium speed operation and micropower supply requirements make this device useful for scratch pad or buffer memory applications where power must be conserved or where battery operation is required.

When used with a battery backup, the MCM14505 can be utilized as an alterable read-only memory, allowing the battery to retain information in the memory when the system is powered down, and allowing the battery to charge when power is applied. The micropower requirements of this memory allow quiescent battery operation for great lengths of time without significant discharging.

- Quiescent Current = 50 nA/package typical @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Single Read/Write Control Line
- Wired-OR Output Capability (3-State Output) for Memory Expansion
- Access Time = 180 ns typical at V_{DD} = 10 Vdc
- Write Cycle Time = 275 ns typical at V_{DD} = 10 Vdc
- Fully Buffered Low Capacitance Inputs
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range



L SUFFIX
CERAMIC PACKAGE
CASE 632

P SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

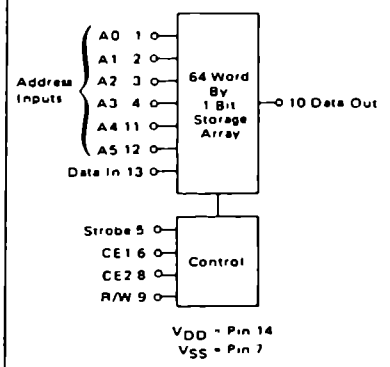
MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range - AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0		0.05	-	0	0.05	-	0.05	Vdc
V_{in} = V_{DD} or 0		10		0.05		0	0.05	-	0.05	
		15		0.05	-	0	0.05	-	0.05	
"1" Level	V_{OH}	5.0	4.95	-	4.95	5.0		4.95	-	Vdc
V_{in} = 0 or V_{DD}		10	9.95		9.95	10		9.95		
		15	14.95	-	14.95	15	-	14.95	-	
Noise Immunity #	V_{NL}									Vdc
(V_{out} = 0.8 Vdc)		5.0	1.5		1.5	2.25	-	1.4	-	
(V_{out} = 1.0 Vdc)		10	3.0		3.0	4.50		2.9	-	
(V_{out} = 1.5 Vdc)		15	4.5		4.5	6.75	-	4.4	-	
(V_{out} = 0.8 Vdc)	V_{NH}	5.0	1.4		1.5	2.25		1.5	-	Vdc
(V_{out} = 1.0 Vdc)		10	2.9		3.0	4.50	-	3.0	-	
(V_{out} = 1.5 Vdc)		15	4.4	-	4.5	6.75	-	4.5	-	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-1.2	-	-1.0	-1.7	-	-0.7	-	
(V_{OH} = 4.6 Vdc)		5.0	-0.25	-	-0.2	-0.36	-	-0.14	-	
(V_{OH} = 9.5 Vdc)		10	-0.62	-	-0.5	-0.9	-	-0.35	-	
(V_{OH} = 13.5 Vdc)		15	-1.8	-	-1.5	-3.5	-	-1.1	-	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.3	-	0.25	0.35	-	0.18	-	mAdc
(V_{OL} = 0.5 Vdc)		10	0.9	-	0.75	1.2	-	0.50	-	
(V_{OL} = 1.5 Vdc)		15	2.2	-	1.7	4.5	-	1.2	-	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-1.0	-	-0.8	-1.7	-	-0.6		
(V_{OH} = 4.6 Vdc)		5.0	-0.2	-	-0.16	-0.36	-	-0.12	-	
(V_{OH} = 9.5 Vdc)		10	-0.5	-	-0.4	-0.9	-	-0.3		
(V_{OH} = 13.5 Vdc)		15	-1.4	-	-1.2	-3.5	-	-1.0	-	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.2	-	0.15	0.35	-	0.1	-	mAdc
(V_{OL} = 0.5 Vdc)		10	0.6		0.5	1.2		0.4	-	
(V_{OL} = 1.5 Vdc)		15	3.9	-	0.75	4.5	-	0.6	-	
Input Current (AL Device)	I_{in}	15	-	±0.1		±0.00001	±0.1	-	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15		±1.0		±0.00001	±1.0	-	±14	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	-		-	-	5.0	7.5	-	-	pF
Quiescent Current (AL Device)	I_{DD}	5.0		5.0	-	0.050	5.0	-	150	µAdc
(Per Package)		10		10	-	0.100	10		300	
		15		20	-	0.150	20	-	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0		50	-	0.050	50	-	375	µAdc
(Per Package)		10	-	100	-	0.100	100	-	750	
		15	-	200	-	0.150	200	-	1500	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (1.28 µA/kHz) f + I_{DD}							µAdc
		10	I_T = (2.56 µA/kHz) f + I_{DD}							
		15	I_T = (3.85 µA/kHz) f + I_{DD}							
Three-State Leakage Current (AL Device)	I_{TL}	15		±0.1		±0.00001	±0.1		±3.0	µAdc
Three-State Leakage Current (CL/CP Device)	I_{TL}	15	-	±1.0		±0.00001	±1.0		±7.5	µAdc

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
†To calculate total supply current at loads other than 50 pF.

$$I_T(C_L) = I_T(50\ pF) + 1 \times 10^{-3} (C_L - 50) V_{DD} f$$

where: I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (2.43 ns/pF) C_L + 58.5 ns		5.0	–	180	360	
t_{TLH} = (1.08 ns/pF) C_L + 36 ns		10	–	90	180	
t_{TLH} = (0.72 ns/pF) C_L + 39 ns		15	–	75	150	
Output Fall Time	t_{THL}					ns
t_{THL} = (2.16 ns/pF) C_L + 52 ns		5.0	–	160	320	
t_{THL} = (0.96 ns/pF) C_L + 32 ns		10	–	80	160	
t_{THL} = (0.69 ns/pF) C_L + 33 ns		15	–	65	130	
Propagation Delay Time	$t_{acc(R)}$					ns
Read Access Time						
$t_{acc(R)}$ = (1.4 ns/pF) C_L + 385 ns		5.0	–	455	750	
$t_{acc(R)}$ = (10.7 ns/pF) C_L + 175 ns		10	–	210	400	
$t_{acc(R)}$ = (0.5 ns/pF) C_L + 105 ns		15	–	130	300	
Strobe Down Time	t_{WL}					ns
		5.0	500	100	–	
		10	125	50	–	
		15	95	75	–	
Address Setup Time	t_{su}					ns
		5.0	300	-100	–	
		10	120	-40	–	
		15	90	-25	–	
Data Setup Time	$t_{su(D)}$					ns
		5.0	200	70	–	
		10	75	25	–	
		15	55	20	–	
Read Setup Time	$t_{su(R)}$					ns
		5.0	270	90	–	
		10	60	20	–	
		15	45	15	–	
Write Setup Time	$t_{su(W)}$					ns
		5.0	400	80	–	
		10	100	25	–	
		15	75	11	–	
Address Release Time	$t_{rel(R)}$					ns
		5.0	75	15	–	
		10	25	10	–	
		15	20	5.0	–	
Data Hold Time	$t_{h(D)}$					ns
		5.0	50	0	–	
		10	15	0	–	
		15	10	0	–	
Read Release Time	$t_{rel(R)}$					ns
		5.0	0	-90	–	
		10	0	-25	–	
		15	0	-10	–	
Write Release Time	$t_{rel(W)}$					ns
		5.0	0	5.0	–	
		10	0	10	–	
		15	0	30	–	
Read Cycle Time	$t_{cyc(R)}$					ns
		5.0	–	500	750	
		10	–	200	400	
		15	–	150	300	
Write Cycle Time	$t_{cyc(W)}$					ns
		5.0	–	440	700	
		10	–	275	550	
		15	–	200	415	
Output Disable Delay	t_{dis}					ns
(10% Output Change into 1.0 kΩ Load)		5.0	–	200	600	
		10	–	80	200	
		15	–	60	150	

*The formula is for the typical characteristics only.

FIGURE 1 – READ CYCLE TIMING DIAGRAM

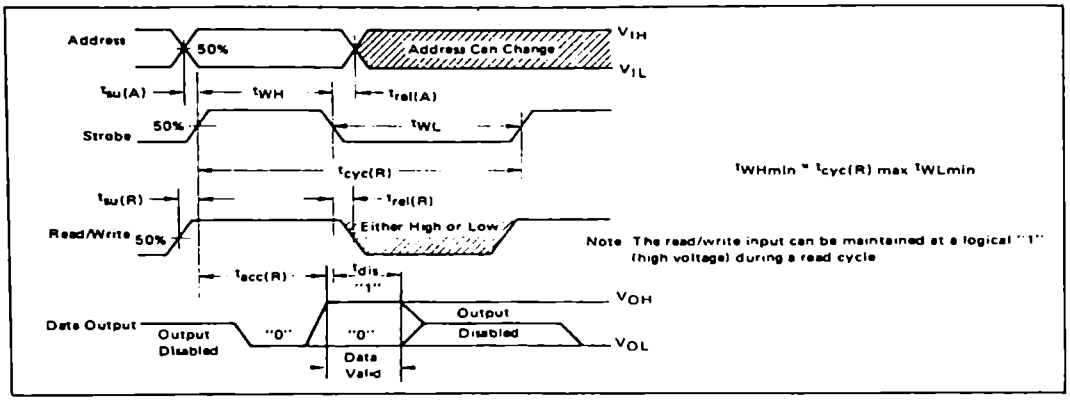


FIGURE 2 – WRITE CYCLE TIMING DIAGRAM

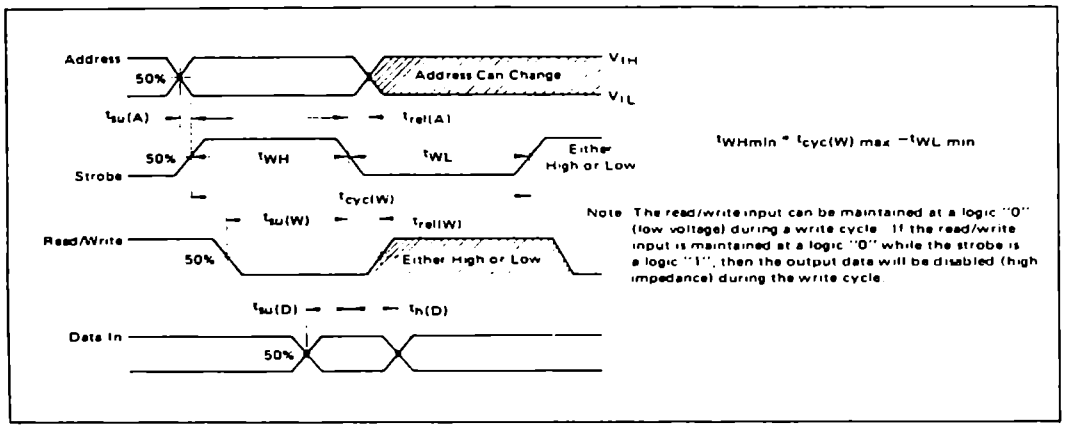


FIGURE 3 – MAXIMUM STROBE PULSE WIDTH versus TEMPERATURE

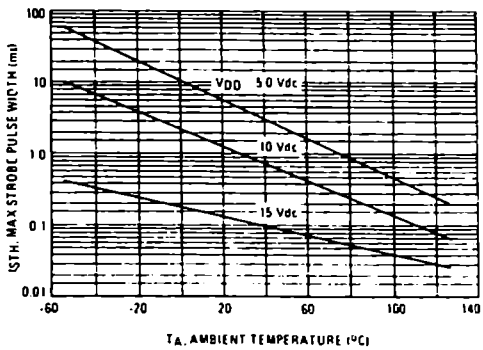


FIGURE 4 – TYPICAL READ ACCESS TIME versus LOAD CAPACITANCE

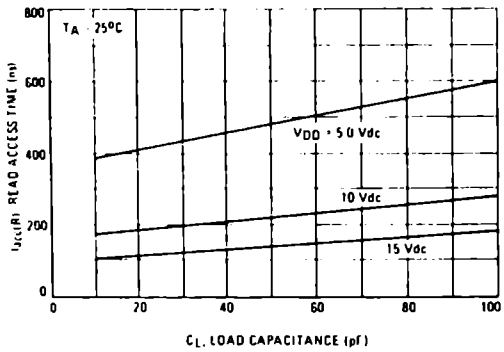
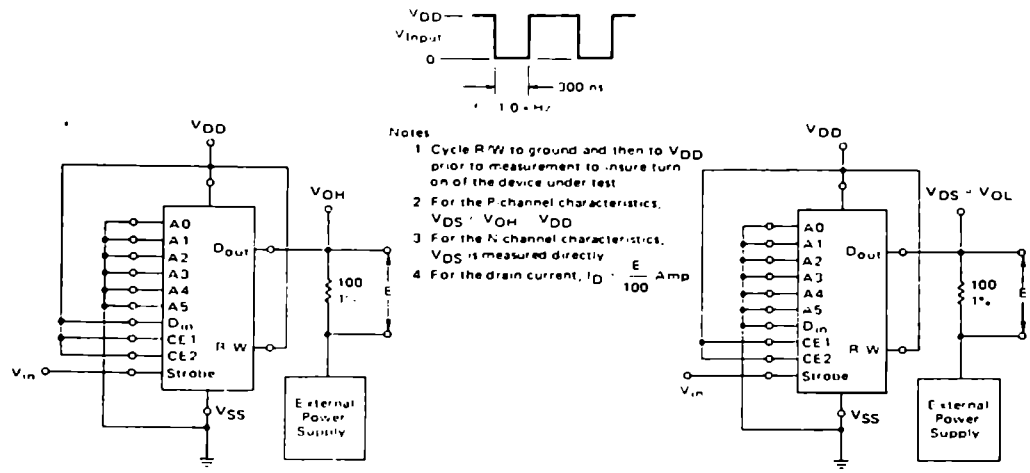
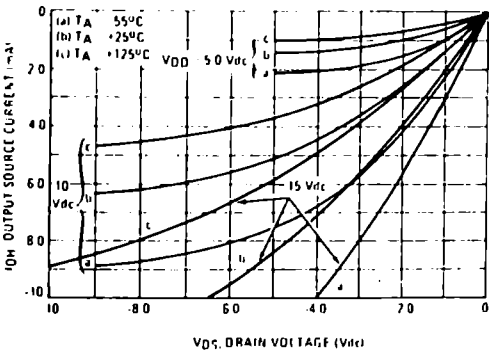


FIGURE 5 – TYPICAL OUTPUT SOURCE CAPABILITY versus TEMPERATURE

FIGURE 6 – TYPICAL OUTPUT SINK CAPABILITY versus TEMPERATURE





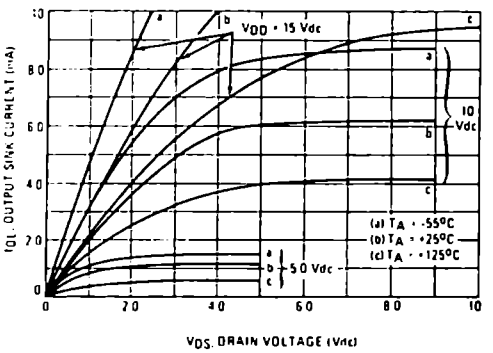
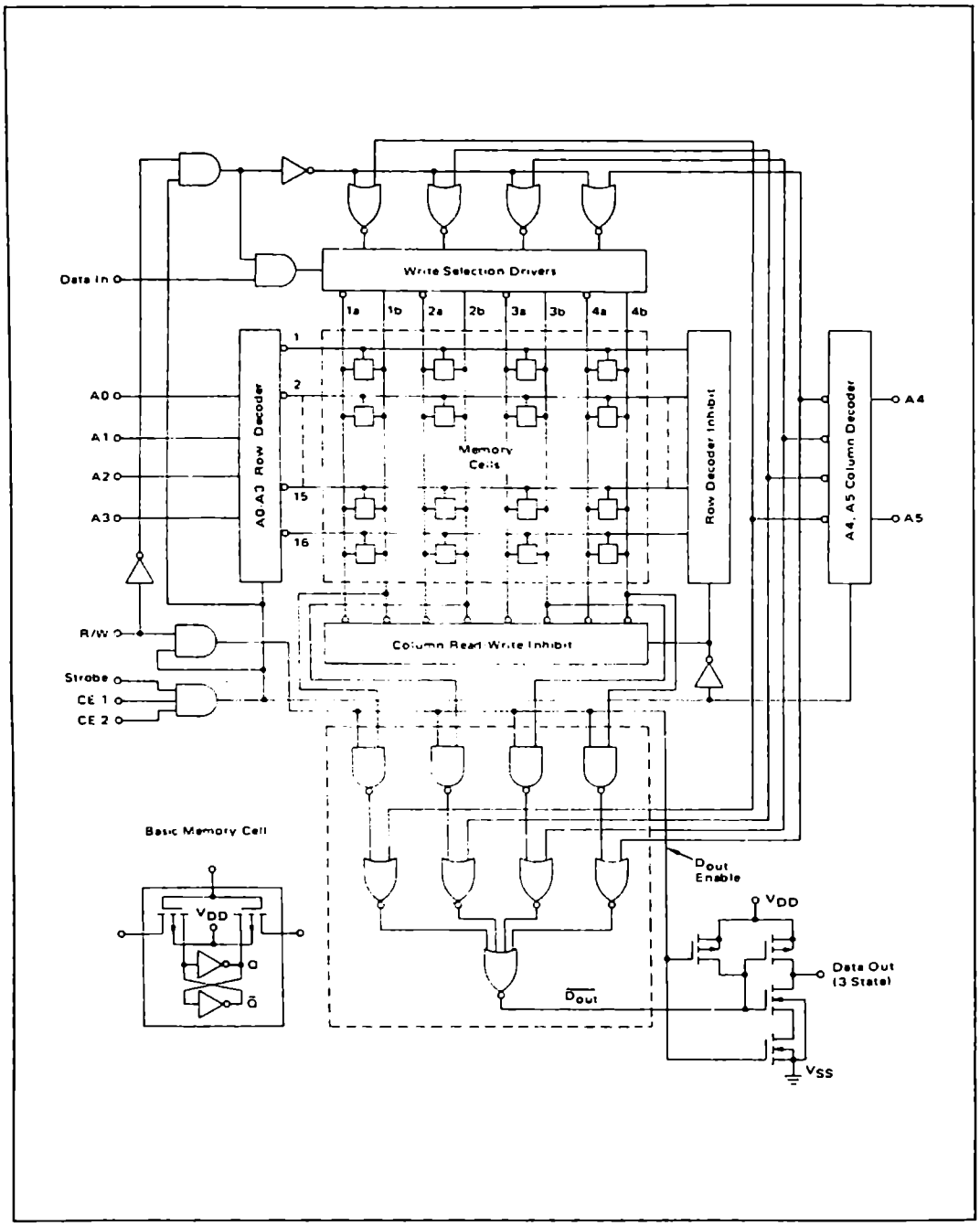


FIGURE 7 – FUNCTIONAL CIRCUIT DIAGRAM



OPERATING CHARACTERISTICS

In considering the operation of the MCM14505 CMOS memory, refer to the functional circuit diagram of Figure 7 and timing diagrams shown in Figures 1 and 2. The basic memory cell is a cross-coupled flip-flop consisting of two inverter gates and two P-channel devices for read/write control. The push-pull cell provides high speed as well as low power.

During a read cycle, when the strobe line is high the write selection drivers are disabled and the data from the selected row is available on columns 1b, 2b, 3b, and 4b. The A4 and A5 address bits are decoded to select output data from one of the four columns. The output data is available on the data output pin only when the strobe and read/write lines are high simultaneously and after the read access time, $t_{acc(R)}$, has occurred (see Figure 1). Note that the output is initially disabled and always goes to the logic "0" state (low voltage) before data is valid. The output is in the high-impedance state (disabled) when the strobe line or the R/W line is in the low state. The memory is strobed for reading or writing only when the strobe, CE1, and CE2 are high simultaneously. The R/W line can be a dc voltage during a read or write cycle and need not be pulsed, as shown in the timing diagrams. For this case the R/W line should be a logic "1" (high) for reading and a logic "0" for writing.

When the strobe line is high, the column read/write inhibit gates and the row decoder inhibit gates are disabled, the selected row is in the low state, and the unselected 15 rows retain their logic "1" level due to the row capacitance that exists when the row decoder inhibit gates are disabled. This capacitive storage mechanism requires a maximum strobe width (see Figure 3) equal to the junction reverse bias RC time constant. When the strobe is returned to a logic "0" the rows are forced to V_{DD} by the row decoder inhibit gates (pullup devices). Similarly the column read/write inhibit gates (pulldown devices) force the column lines to a logic "0" state.

Two column lines are associated with each memory cell in order to write into the cell. The write selection drivers are enabled when the R/W line is a logic "0" and the strobe line is a logic "1". The input data is written into the column selected by the column decoder. For instance, if a "1" is to be written in the memory cell associated with row 1 and column 1, then row 1 would be enabled (logic "0") while column 1b is forced high and column 1a is forced low by the write selection drivers. If a logic "0" is to be written into the cell, then column 1a is forced high and 1b is forced low. The data that is retained in the memory cell is the data that was present on the data input pin at the moment the strobe goes low when R/W is low, or when R/W goes high when the strobe is high.

APPLICATIONS INFORMATION

Figure 8 shows a 256-word by n-bit static RAM memory system. The outputs of four MCM14505 devices are tied together to form 256 words by 1 bit. Additional bits are attained by paralleling the inputs in groups of four. Memories of larger words can be attained by decoding the most significant bits of the address and ANDing them with the strobe input.

Fan-in and fan-out of the memory is limited only by speed requirements. The extremely low input and output leakage current (100 nA maximum) keep the output voltage levels from changing significantly as more outputs are tied together. With the output levels independent of fan-out, most of the power supply range is available as logic swing, regardless of the number of units wired together. As a result, high noise immunity is maintained under all conditions.

Power dissipation is 0.1 μW per bit at a 1.0-kHz rate for a 5.0-volt power supply, while the static power dissipation is 2.0 nW per bit. This low power allows non-volatile information storage when the memory is powered by a small standby battery.

Figure 9 shows an optional standby power supply circuit for making a CMOS memory "non-volatile". When the usual power fails, a battery is used to sustain operation or maintain stored information. While normal power supply voltage is present, the battery is trickle-charged through a resistor which sets the charging rate. V_B is the sustaining voltage, and V^+ is the ordinary voltage from a power supply. V_{DD} connects to the power pin on the memory. Low-leakage diodes are recommended to conserve battery power.

The memory system shown in Figure 8 can be interfaced directly with the other devices in the McMOS family. No external components are required.

At the inputs to the CMOS memory, TTL devices can interface directly if an open-collector logic gate such as the MC7407 is used as shown in Figure 10. Driver circuits are not required since the input capacitance is low (4.0 to 6.0 pF). The address, data, and read/write inputs do not need to be fast since they can be changed for the duration when the strobe pulse is low, t_{STL} (see Figures 1 and 2). For high-speed operation, a push-pull driver should be used if more than five strobe inputs must be driven at one time. One circuit of the type shown in Figure 10 can be used for every ten strobe inputs.

Figures 11, 12, and 13 show methods of interfacing the memory output to TTL logic at various memory voltages. If a V_{DD} of 5.0 volts is used for slow-speed, low-power applications, one transistor and one resistor must be used (Figure 11). The MCM14505AL will drive one low-power TTL gate directly.

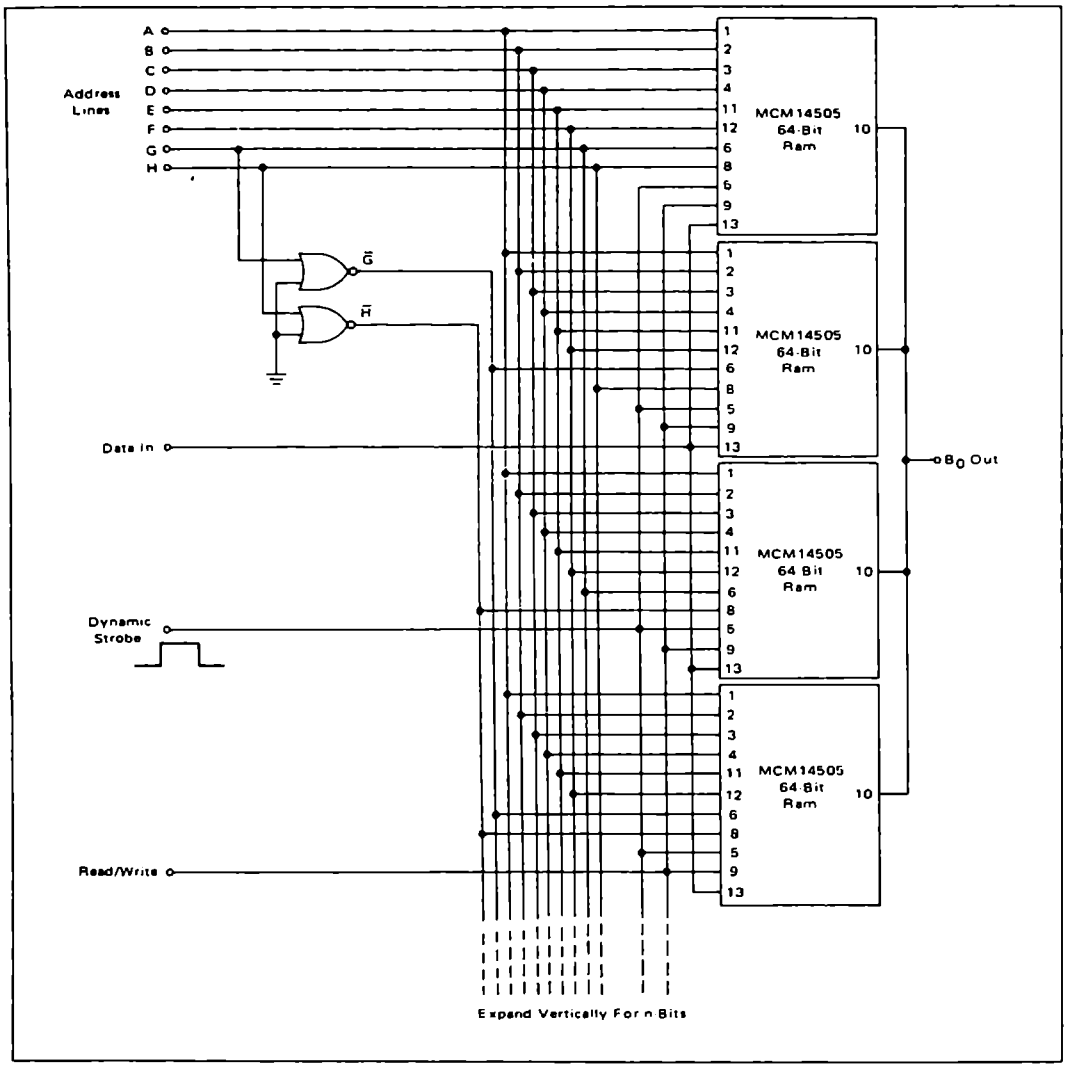
If a V_{DD} of 10 volts is used, the output of the memory device can fan out to two low-power TTL gates (Figure 12a) or to a discrete transistor (Figure 12b). The discrete transistor circuit provides higher speed and/or high fan-out. A pulldown resistor at the base of the transistor is not needed for fast turn-off because of the push-pull output of the memory. Turn-on time of the transistor is much faster in Figure 12b since the voltage rise is only 0.75 volt. The low output capacitance of the MCM14505 means that several outputs can be wire-ORed without significantly degrading performance. The read access time is increased by only 20 ns typically for 16 outputs tied together when Figure 12b is used.

Five low-power TTL gates can be driven from the memory output if a V_{DD} of 15 volts is used (Figure 13a). Figure 13b shows the interface if a discrete transistor is used. The 1.0 kilohm resistor in the base is required to insure that not more than 10 mA flows through the output as listed in the maximum ratings. If a 2.0 kilohm collector resistor is used (fan-out = 3), the turn-on time of the transistor is only slightly faster than in the circuit shown in Figure 12b due to the lower output impedance when V_{DD} = 15 volts. The voltage at the memory data output has to rise to only 1.3 volts to insure driving a fan-out of three TTL devices.

If a 510-ohm collector resistor is used, 20 TTL loads may be driven. The read access time is increased about 20 ns when four memory outputs are tied together since the output voltage must rise to 3.7 volts before the transistor can sink the full I_{OL} for a fan-out of 20 TTL devices. Almost any NPN transistor with a minimum beta of 15 can be used for the interface shown in Figures 11, 12 and 13.

The high source current from the push-pull output stage of the MCM14505 makes for a simpler interface circuit since a low source current memory requires a differential comparator to achieve high-speed operation.

FIGURE 8 – CMOS 256-WORD BY n-BIT STATIC READ/WRITE MEMORY



Circuit diagrams utilizing Motorola products are included as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of Motorola Inc. or others.

FIGURE 9 – STAND BY BATTERY CIRCUIT

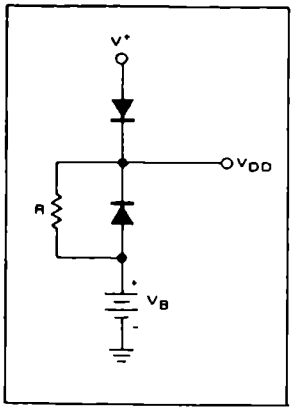


FIGURE 10 – TTL TO CMOS INTERFACE

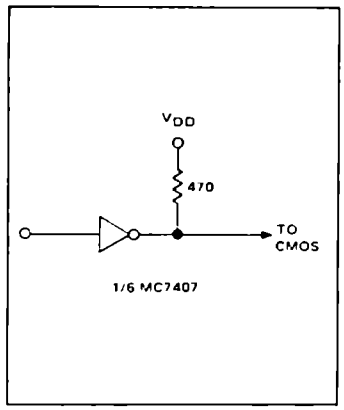


FIGURE 11 – CMOS-TO-TTL INTERFACE FOR V_{DD} = 5.0 V

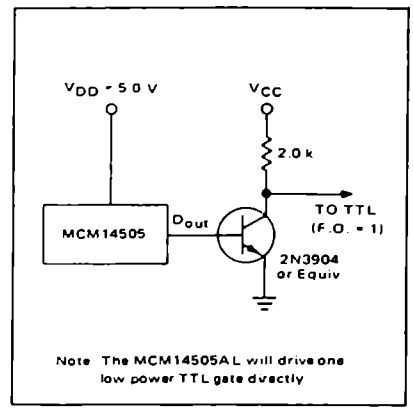


FIGURE 12 – CMOS-TO-TTL INTERFACE FOR V_{DD} = 10 V

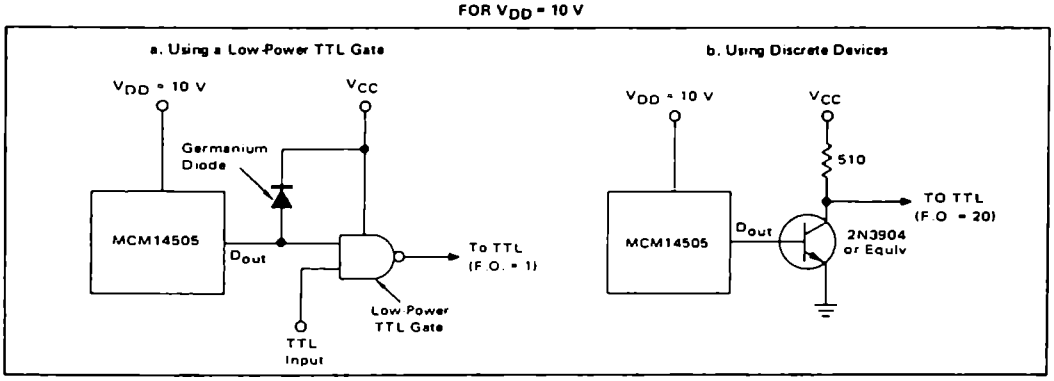
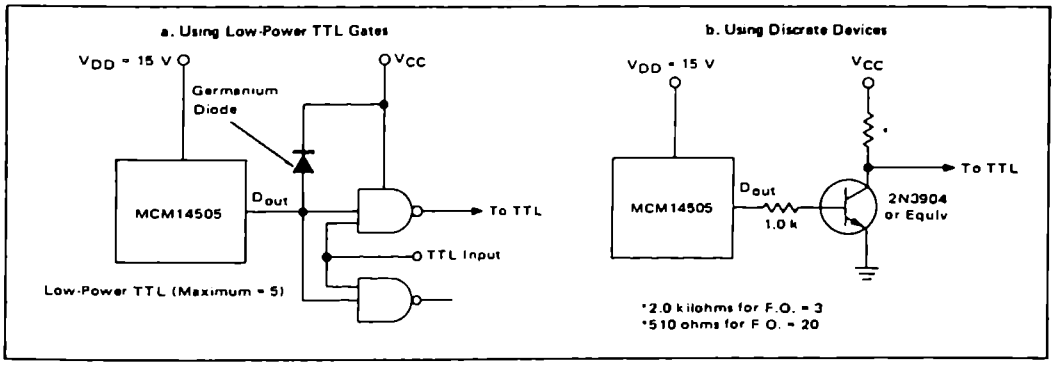


FIGURE 13 – CMOS-TO-TTL INTERFACE FOR V_{DD} = 15 V



MOTOROLA

MCM14537

256-BIT STATIC RANDOM ACCESS MEMORY

The MCM14537 is a static random access memory (RAM) organized in a 256 x 1-bit pattern and constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. The circuit consists of eight address inputs (A_n), one data input (D_{in}), one write enable input (WE), one strobe input (ST), two chip enable inputs (CE_n), and one data output (D_{out}).

Using both chip enable inputs as extensions of the address inputs, a 10-bit address scheme may be employed. Four MCM14537 devices may be used to comprise a 1024-bit memory without additional address decoding. The CE and ST inputs are dissimilary designed to enable usage of the memory in a variety of applications. An output latch is provided on the chip for storing the data read or written into memory, making a data-out storage register unnecessary. The CE inputs control the data output for third-state (high output impedance) or active operation which makes the memory very useful in a bus oriented system. When CE2 is high the chip is fully disabled. When CE1 is high the output is in the third state but data can be written into the output latch during a read cycle. This enables the use of the memory for fast reading by using the CE1 input to enable the latch. The memory is also designed so that dc signals can operate the memory with no maximum pulse width required on the CE and ST lines.

Medium speed operation and micropower operation make the device useful in scratch pad and buffer applications where micropower or battery operation and high noise immunity are required

- Quiescent Current = 0.5 μA/package typical @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- 3-state Output Capability for Memory Expansion
- Output Data Latch Eliminates Need for Storage Buffer
- Access Time = 700 ns typical @ V_{DD} = 10 Vdc
- Fully Decoded and Buffered
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range

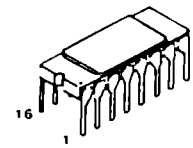
MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

CMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

256-BIT (256 x 1) STATIC RANDOM ACCESS MEMORY

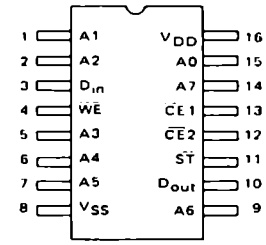


CERAMIC PACKAGE
CASE 690

ORDERING INFORMATION

MCM14XXX — Suffix Denotes
- L Ceramic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields, however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05		0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10		0.05		0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0		4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95		9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Noise Immunity #	V_{NL}									Vdc
(V_{out} = 0.8 Vdc)		5.0	1.5		1.5	2.25	–	1.4	–	
(V_{out} = 1.0 Vdc)		10	3.0		3.0	4.50		2.9	–	
(V_{out} = 1.5 Vdc)		15	4.5		4.5	6.75	–	4.4	–	
(V_{out} = 0.8 Vdc)	V_{NH}	5.0	1.4		1.5	2.25		1.5	–	Vdc
(V_{out} = 1.0 Vdc)		10	2.9	–	3.0	4.50	–	3.0	–	
(V_{out} = 1.5 Vdc)		15	4.4	–	4.5	6.75	–	4.5	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-1.2		1.0	-1.7	–	-0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.25		-0.2	-0.36	–	-0.14	–	
(V_{OH} = 9.5 Vdc)		10	-0.62	–	-0.5	-0.9		-0.35	–	
(V_{OH} = 13.5 Vdc)		15	-1.8		-1.5	-3.5		-1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64		0.51	0.88		0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6		1.3	2.25		0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2		3.4	8.8		2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-1.0		-0.8	-1.7		-0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.2	–	-0.16	-0.36	–	-0.12	–	
(V_{OH} = 9.5 Vdc)		10	-0.5	–	-0.4	-0.9	–	-0.3	–	
(V_{OH} = 13.5 Vdc)		15	-1.4	–	-1.2	-3.5		-1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88		0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3		1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1		±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15		±1.0		±0.00001	±1.0	–	±14	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–		–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	100	–	0.5	100	–	1800	µAdc
(Per Package)		10		200	–	1.0	200	–	3600	
		15		400		1.5	400	–	7200	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	100		0.5	100	–	1800	µAdc
(Per Package)		10	–	200	–	1.0	200	–	3600	
		15		400	–	1.5	400	–	7200	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (1.46 µA/kHz) f + I_{DD}							µAdc
		10	I_T = (2.91 µA/kHz) f + I_{DD}							
		15	I_T = (4.37 µA/kHz) f + I_{DD}							
Three State Leakage Current (AL Device)	I_{TL}	15		±0.1	–	±0.00001	±0.1	–	±3.0	µAdc
Three-State Leakage Current (CL/CP Device)	I_{TL}	15		±1.0		±0.00001	±1.0	–	±7.5	µAdc

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device
T_{high} = +125°C for AL Device, +85°C for CL/CP Device
#Noise immunity specified for worst-case input combination
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc
†To calculate total supply current at loads other than 50 pF
$I_T(C_L) = I_T(50\ pF) + 1 \times 10^{-3} (C_L - 50) V_{DD} f$
where I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency
**The formulas given are for the typical characteristics only at 25°C

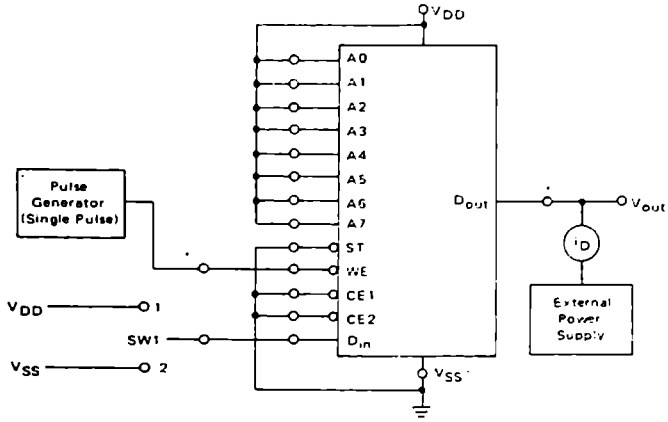
SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Figure	Symbol	V_{DD}	Min	Typ	Max	Unit
Output Rise Time	3	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns			5.0	–	180	360	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns			10	–	90	180	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns			15	–	65	130	
Output Fall Time	3	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns			5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns			10	–	50	100	
t_{THL} = (0.55 ns/pF) C_L + 9.5 ns			15	–	40	80	
Read Access Time from $\overline{ST}$ or $\overline{CE2}$	4, 5	$t_{acc(R)}$					ns
t_{acc} = (1.4 ns/pF) C_L + 2480 ns			5.0	400	2500	6000	
t_{acc} = (0.7 ns/pF) C_L + 690 ns			10	150	700	2000	
t_{acc} = (0.5 ns/pF) C_L + 393 ns			15	115	400	1500	
Output Enable Delay from $\overline{CE1}$ or $\overline{CE2}$	5, 6	$t_{acc(\overline{CE}_n)}$	5.0	70	300	900	ns
			10	25	100	300	
			15	20	70	225	
Setup Time from A_n to $\overline{ST}$ or $\overline{CE2}$	4, 5, 6, 7	$t_{su(A)}$	5.0	1800	600	–	ns
			10	600	200	–	
			15	450	140	–	
Hold Time from A_n to $\overline{ST}$ or $\overline{CE2}$	4, 5, 6, 7	$t_{h(A)}$	5.0	600	200	–	ns
			10	240	80	–	
			15	180	55	–	
Data Hold Time	7	$t_{h(D)}$	5.0	1400	480	–	ns
			10	500	160	–	
			15	375	110	–	
Data Setup Time	7	$t_{su(D)}$	5.0	3600	1200	–	ns
			10	1800	600	–	
			15	1350	420	–	
Write Enable Hold Time	7	$t_{h(\overline{WE})}$	5.0	150	50	–	ns
			10	60	20	–	
			15	45	15	–	
Write Enable Setup Time	7	$t_{su(\overline{WE})}$	5.0	720	240	–	ns
			10	240	80	–	
			15	180	55	–	
Write Enable to D_{out} Disable**	4	$t_{\overline{WE}}$	5.0	720	240	–	ns
			10	240	80		
			15	180	55		
Strobe or $\overline{CE2}$ Pulse Width When Reading	4, 5, 6	$t_{WL(R)}$	5.0	1350	450	–	ns
			10	450	150	–	
			15	340	100	–	
Strobe, $\overline{CE1}$ or $\overline{CE2}$ Pulse Width When Writing	7	$t_{WL(W)}$	5.0	2400	1200	–	ns
			10	1260	600	–	
			15	945	420	–	
Write Recovery Time	4	$t_{R(W)}$					ns
t_W = (1.4 ns/pF) C_L + 219 ns			5.0	70	240	720	
t_W = (0.7 ns/pF) C_L + 70 ns			10	25	80	240	
t_W = (0.5 ns/pF) C_L + 47.5 ns			15	20	55	180	
$\overline{CE1}$ or $\overline{CE2}$ to D_{out} Disable Delay**	6	$t_{\overline{CE}_n}$	5.0	70	300	900	ns
			10	25	100	300	
			15	20	70	225	
Read Setup Time	4, 5	$t_{su(R)}$	5.0	0	-100	–	ns
			10	0	-40	–	
			15	0	-30	–	
Read Hold Time	4, 5	$t_{h(R)}$	5.0	540	180	–	ns
			10	240	60	–	
			15	180	45	–	
Read Cycle Time	4, 5	$t_{cyc(R)}$	5.0	–	2500	6000	ns
			10	–	700	2100	
			15	–	500	1575	
Write Cycle Time	7	$t_{cyc(W)}$	5.0	–	1400	4800	ns
			10	–	700	2100	
			15	–	500	1575	

* The formula given is for the typical characteristics only

** 10% output change into a 1.0 kΩ load.

FIGURE 1 – TYPICAL OUTPUT SOURCE AND SINK CURRENT CHARACTERISTICS TEST CIRCUIT



Input	Output Source Characteristics	Output Sink Characteristics
$\overline{WE}$	Pulse Once	Pulse Once
D_{in}	SW1 in Position 1	SW1 in Position 2
V_{GS}	$-V_{DD}$	V_{DD}
V_{DS}	$V_{out} - V_{DD}$	V_{out}

FIGURE 2 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORMS

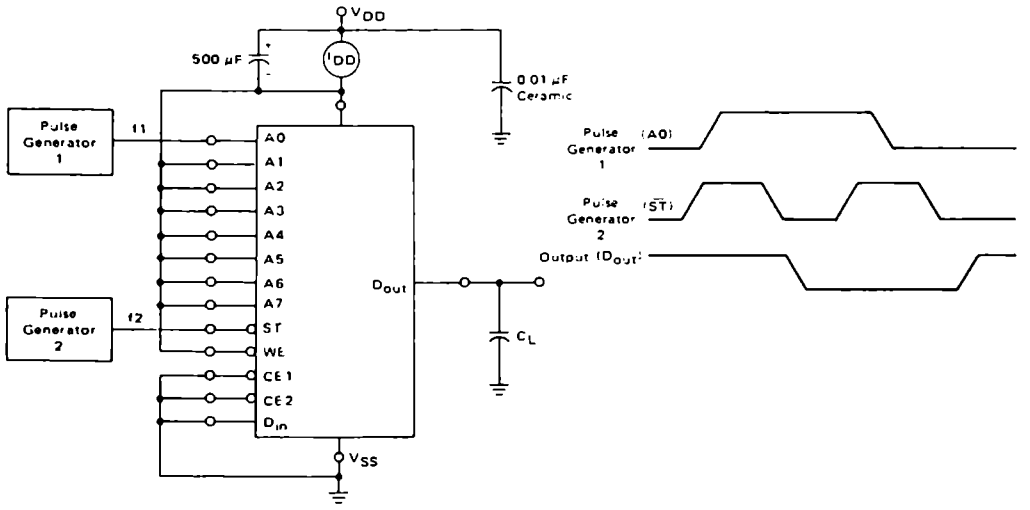


FIGURE 3 – AC TEST CIRCUIT

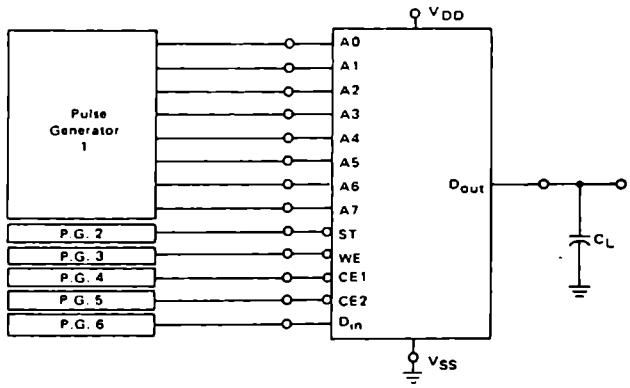
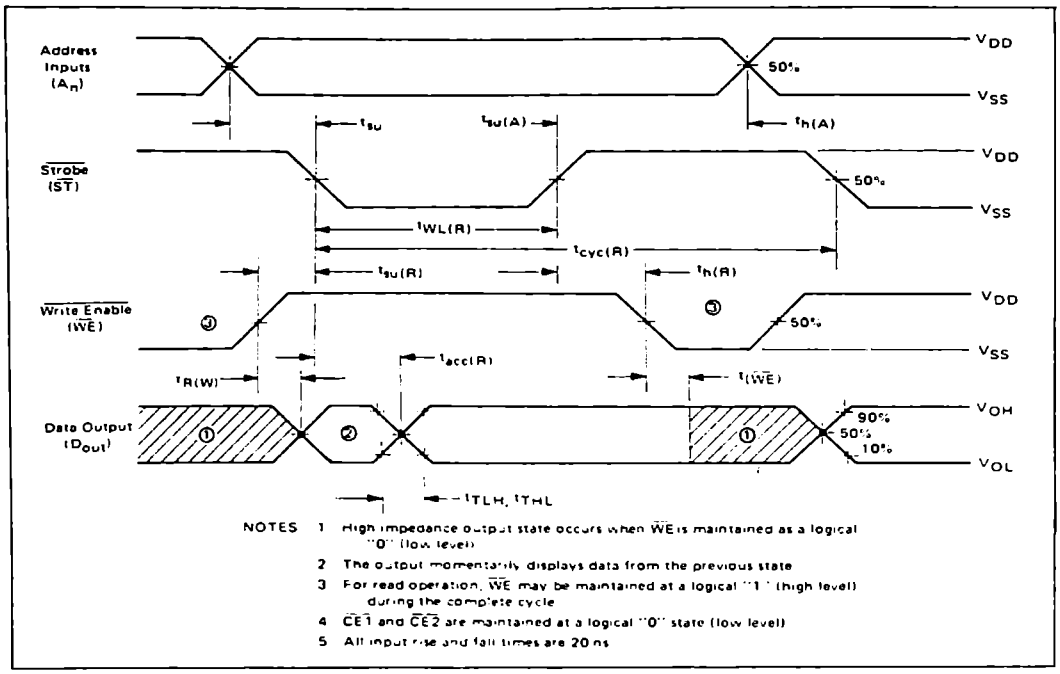
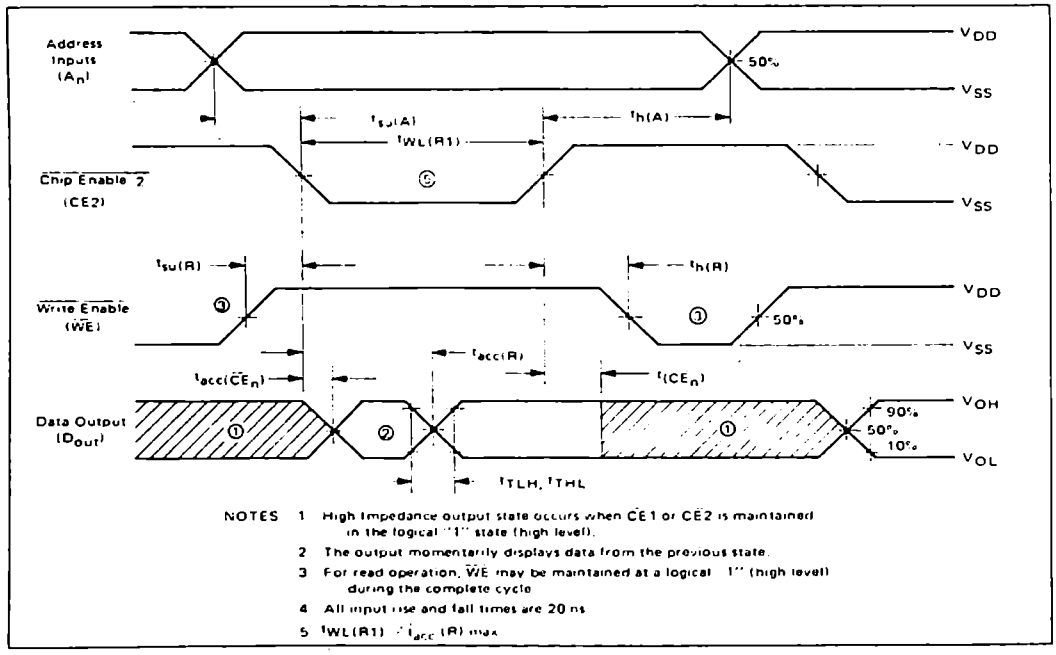


FIGURE 4 – READ CYCLE WAVEFORMS UTILIZING STROBE-TO-ACCESS MEMORY



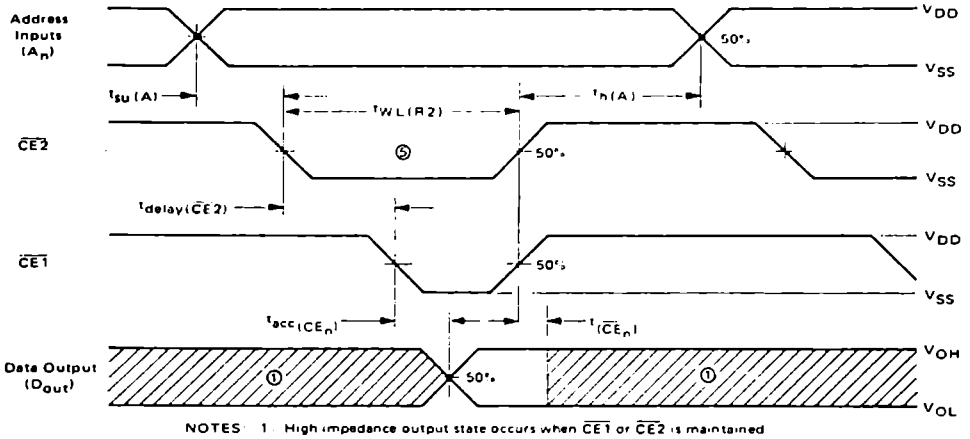
NOTES
1. High impedance output state occurs when $\overline{WE}$ is maintained as a logical "0" (low level)
2. The output momentarily displays data from the previous state
3. For read operation, $\overline{WE}$ may be maintained at a logical "1" (high level) during the complete cycle
4. $\overline{CE1}$ and $\overline{CE2}$ are maintained at a logical "0" state (low level)
5. All input rise and fall times are 20 ns

FIGURE 5 – READ CYCLE WAVEFORMS UTILIZING $\overline{CE2}$ FOR ACCESS MEMORY



NOTES
1. High impedance output state occurs when $\overline{CE1}$ or $\overline{CE2}$ is maintained in the logical "1" state (high level).
2. The output momentarily displays data from the previous state.
3. For read operation, $\overline{WE}$ may be maintained at a logical "1" (high level) during the complete cycle
4. All input rise and fall times are 20 ns
5. $t_{WL(R1)} \geq t_{acc(R)}$ max

FIGURE 6 – READ CYCLE WAVEFORMS UTILIZING $\overline{CE1}$ AND $\overline{CE2}$ TO ACCESS MEMORY

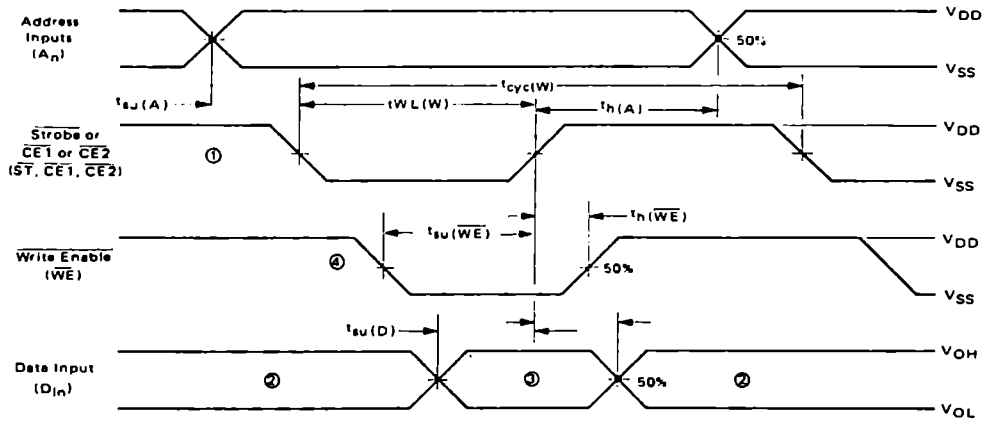


NOTES:
1. High impedance output state occurs when $\overline{CE1}$ or $\overline{CE2}$ is maintained in the logical "1" state (high level).
2. $\overline{WE}$ is maintained at the logical "1" state for this example.
3. All input rise and fall times are 20 ns.
4. $t_{delay(\overline{CE2})}$ minimum assuares that only data presently addressed will appear at the output.

$$t_{delay(\overline{CE2})\ min} \geq t_{acc_{R\ max.}} - t_{acc(\overline{CE1})\ min}$$

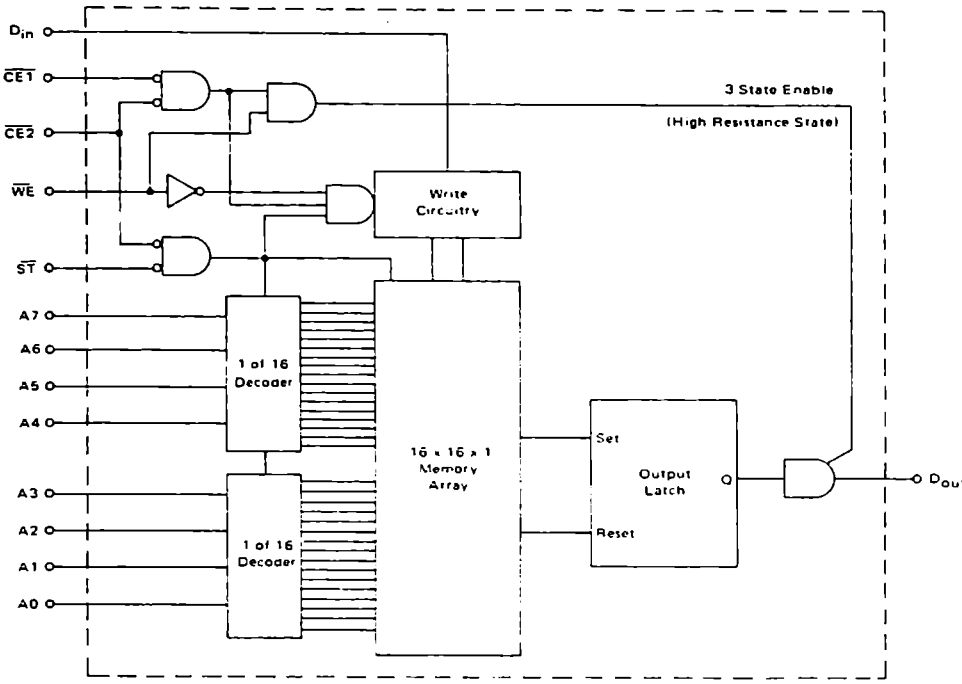
5. $t_{WL(R2)} \geqslant t_{delay\ (CE2)\ min} + t_{acc\ (CE_n)\ max}$

FIGURE 7 – WRITE CYCLE WAVEFORMS



NOTES:
1. The Strobe, $\overline{CE1}$ and $\overline{CE2}$ may be utilized to control a write cycle, however, during changes of address either Strobe or $\overline{CE2}$ must be in the logical "1" state (high level).
2. Data input logic level is don't care during the indicated intervals.
3. Data input logic level must remain fixed.
4. Write Enable may be maintained as a logical "0" during the write cycle.
5. All input rise and fall times are 20 ns.

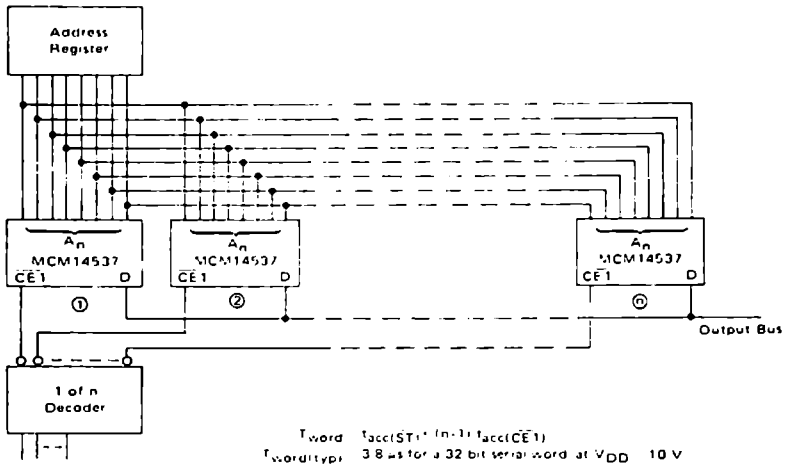
LOGIC/BLOCK DIAGRAM



FUNCTION	$\overline{CE1}$	$\overline{CE2}$	$\overline{ST}$	$\overline{WE}$	D_{in}	D_{out}	COMMENTS
Address changing valid	X	X	1	X	X	R/A	D_{out} will be active if $\overline{CE1}$ and $\overline{CE2}$ = "0" and $\overline{WE}$ = "1"
	X	1	X	X	X	R	$\overline{CE2}$ = "1" fully disables internal logic and output
Address changing not valid	X	0	0	X	X	R/A	Changing address in this mode may result in altered data
D_{out} disabled in high resistance state	1	X	X	X	X	R	$\overline{CE1}$ = "1" disables write cycle and D_{out}
	X	1	X	X	X	R	The chip is fully disabled
	X	X	X	0	X	R	$\overline{WE}$ = "0" enables writing into memory if $\overline{CE1}$, $\overline{CE2}$, and $\overline{ST}$ = "0"
D_{out} enabled in active state	0	0	X	1	X	A	If $\overline{ST}$ = "1" the output stores and reads the previous data from or written into memory
Read addressed memory location into output latch.	0	0	0	1	X	A	The output reads the present contents that are addressed
	1	0	0	1	X	R	The addressed location is read into output latch with output in the "R" state.
Disable reading from memory	X	1	X	X	X	R	Address changing can take
	X	X	1	X	X	R/A	place in this condition
Write into memory	0	0	0	0	A	R	D_{in} is written into memory and into the output latch
Write disabled	1	X	X	X	X	R	$\overline{WE}$ = "1" is a read enable
	X	1	X	X	X	R	$\overline{WE}$ = "0" is a write enable.
	X	X	1	X	X	R/A	
	X	X	X	1	X	R/A	

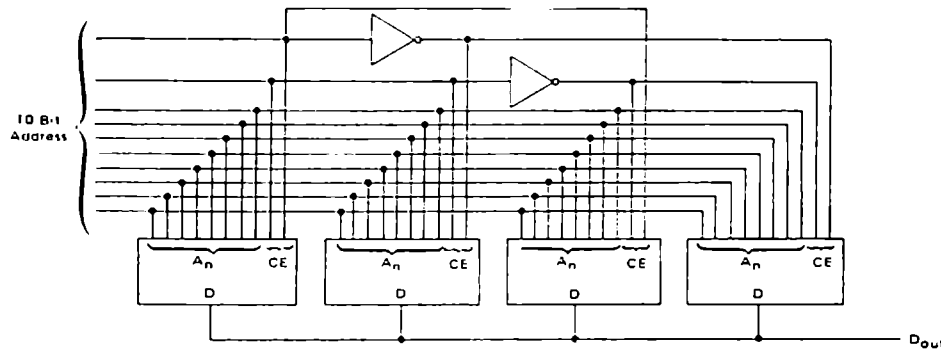
R = High resistance state at D_{out}
A = An active level of either V_{SS} or V_{DD}
R/A = An R or A condition depending on the don't care condition
X = Don't care condition (must be in the "1" or "0" state)
1 = A high level at V_{DD}
0 = A low level at V_{SS}

TYPICAL APPLICATION FOR SERIAL WORDS UTILIZING BUS TECHNIQUES

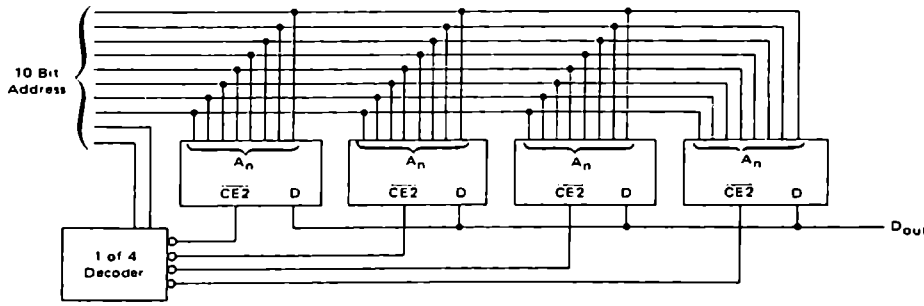


T_{word} $t_{acc(ST)}$ + (n-1) $t_{acc(\overline{CE}1)}$

$T_{word(typ)}$ 3.8 µs for a 32 bit serial word at V_{DD} 10 V



Typical 1024 x 1 RAM Utilizing Four MCM14537's



Typical Low Power 1024 x 1 RAM Utilizing Four MCM14537's.

MOTOROLA

MCM14552

CMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

256-BIT (64 x 4) STATIC RANDOM ACCESS MEMORY

256-BIT STATIC RANDOM ACCESS MEMORY

The MCM14552 is a static random access memory (RAM) organized in a 64 x 4 bit pattern. The three chip enable inputs can be used as extensions of the six address inputs, creating 9-bit address scheme. Eight MCM14552 devices may be used to comprise a 2048-bit memory (512 x 4) without additional address decoding.

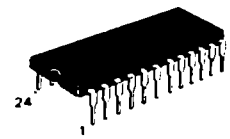
The mode control (M) is used to change the control logic characteristic of the circuit. For example, with M high, the 3-state input (T) fully controls the 3-state characteristic of the output. With M low, the output 3-state characteristic is controlled by chip enable inputs (CE), write enable input (WE) and T.

The memory is designed so that dc signals may operate the memory, with no maximum pulse width restrictions.

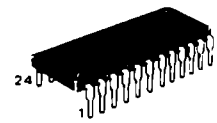
Medium speed, micropower operation, and control flexibility make the device useful in scratch pad or buffer applications where battery operation or high noise immunity are required.

- Quiescent Current = 50 μA/package typical @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- 3-state Output Capability for Memory Expansion
- Output Data Latch Eliminates Need for Storage Buffer
- Access Time = 700 ns typical @ V_{DD} = 10 Vdc
- Fully Decoded and Buffered
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range

NOTE: Pin 20(LE)) must be connected to V_{SS}



L SUFFIX
CERAMIC PACKAGE
CASE 623



P SUFFIX
PLASTIC PACKAGE
CASE 709

ORDERING INFORMATION

MCM14XXX — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

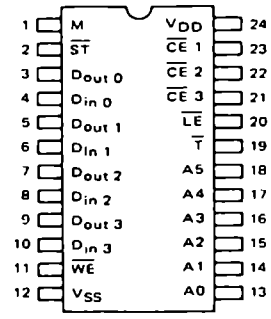
MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields, however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

PIN ASSIGNMENT



ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0		0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10		0.05		0	0.05		0.05	
		15		0.05		0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0		4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10		9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0		1.5		2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10		3.0		4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15		4.0		6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5		3.5	2.75		3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0		7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-1.2		-1.0	-1.7	–	-0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.25	–	-0.2	-0.36		-0.14	–	
(V_{OH} = 9.5 Vdc)		10	-0.62		-0.5	-0.9	–	-0.35	–	
(V_{OH} = 13.5 Vdc)		15	-1.6	–	-1.5	-3.5	–	-1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-1.0		-0.8	-1.7		-0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.2	–	-0.16	-0.36	–	-0.12	–	
(V_{OH} = 9.5 Vdc)		10	-0.5	–	-0.4	-0.9		-0.3	–	
(V_{OH} = 13.5 Vdc)		15	-1.4	–	-1.2	-3.5		-1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3		1.1	2.25		0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6		3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15		±0.1		±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15		±1.0		±0.00001	±1.0	–	±14.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–				5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0		5.0		0.050	5.0	–	150	µAdc
(Per Package)		10		10		0.100	10		300	
		15		20		0.150	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0		50		0.050	50		375	µAdc
(Per Package)		10		100		0.100	100		750	
		15		200		0.150	200	–	1500	
Total Supply Current** ‡ (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (1.98 µA/kHz) f + I_{DD}							µAdc
		10	I_T = (3.96 µA/kHz) f + I_{DD}							
		15	I_T = (5.86 µA/kHz) f + I_{DD}							
Three State Leakage Current (AL Device)	I_{TL}	15		±0.1		±0.00001	±0.1		±3.0	µAdc
Three State Leakage Current (CL/CP Device)	I_{TL}	15		±1.0		±0.00001	±1.0		±7.5	µAdc

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device
T_{high} = +125°C for AL Device, +85°C for CL/CP Device

#Noise immunity specified for worst case input combination

Noise Margin for both "1" and "0" level		
	1.0 Vdc min @ V_{DD}	5.0 Vdc
	2.0 Vdc min @ V_{DD}	10 Vdc
	2.5 Vdc min @ V_{DD}	15 Vdc

‡To calculate total supply current at loads other than 50 pF

$$I_T(C_L) = I_T(50\ pF) + 4 \times 10^{-3} (C_L - 50) V_{DD} f$$

where I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.

**The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Figure	Symbol	V_{DD}	Min	Typ	Max	Unit
Output Rise Time	1	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns			5.0	–	180	360	
t_{TLH} = (1.5 ns/pF) C_L + 25 ns			10	–	90	180	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns			15	–	65	130	
Output Fall Time	1	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns			5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns			10	–	50	100	
t_{THL} = (0.55 ns/pF) C_L + 9.5 ns			15	–	40	80	
Read Cycle Time	1, 2	$t_{cyc(R)}$	5.0	–	2000	6000	ns
			10	–	750	2200	
			15	–	500	1650	
Write Cycle Time	3, 4	$t_{cyc(W)}$	5.0	–	1200	3600	ns
			10	–	750	2200	
			15	–	500	1650	
Address to $\overline{\text{Strobe}}$ Setup Time	1, 3	$t_{su(A\text{-}\overline{ST})}$	5.0	1500	500	–	ns
			10	450	150	–	
			15	350	120	–	
$\overline{\text{Strobe}}$ to Address Hold Time	1, 3	$t_{h(\overline{ST}\text{-}A)}$	5.0	150	50	–	ns
			10	100	0	–	
			15	75	0	–	
Address to $\overline{\text{Chip Enable}}$ Serup Time	2, 4	$t_{su(A\text{-}\overline{CE})}$	5.0	1800	600	–	ns
			10	600	200	–	
			15	450	150	–	
$\overline{\text{Chip Enable}}$ to Address Hold Time	2, 4	$t_{h(\overline{CE}\text{-}A)}$	5.0	450	150	–	ns
			10	300	100	–	
			15	225	75	–	
$\overline{\text{Strobe}}$ or $\overline{\text{Chip Enable}}$ Pulse Width When Reading	1, 2	$t_{WL(R)}$	5.0	1800	450		ns
			10	450	150		
			15	350	100		
$\overline{\text{Strobe}}$ or $\overline{\text{Chip Enable}}$ Pulse Width When Writing	3, 4	$t_{WL(W)}$	5.0	3600	1200		ns
			10	1800	600		
			15	1350	400	–	
Read Setup Time	1	$t_{su(R)}$	5.0	0	-100	–	ns
			10	0	-40	–	
			15	0	-30	–	
Read Hold Time	1	$t_{h(R)}$	5.0	540	180	–	ns
			10	240	60	–	
			15	180	45	–	
Data Setup Time	3, 4	$t_{su(D)}$	5.0	1800	600	–	ns
			10	600	200	–	
			15	450	150		
Data Hold Time	3, 4	$t_{h(D)}$	5.0	600	200	–	ns
			10	150	50	–	
			15	120	30	–	

*The formula given is for the typical characteristics only.

(continued)

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C) (continued)

Characteristic	Figure	Symbol	V_{DD}	Min	Typ	Max	Unit
Write Enable Setup Time	3, 4	$t_{su(\overline{WE})}$	5.0	720	240	–	ns
			10	240	80	–	
			15	180	55	–	
Write Enable Hold Time	3, 4	$t_{h(\overline{WE})}$	5.0	150	50	–	ns
			10	60	20	–	
			15	45	15	–	
Read Access Time from Strobe	1, 3	$t_{acc(R-\overline{ST})}$	5.0	–	2000	6000	ns
			10	–	700	2100	
			15	–	350	1600	
Read Access Time from Chip Enable	2	$t_{acc(R-\overline{CE})}$	5.0	–	2100	6300	ns
			10	–	750	2250	
			15	–	400	1700	
Output Enable/Disable Delay from Chip Enable or Write Enable	2, 4	$t_{R(\overline{CE})}$, $t_{R(\overline{WE})}$	5.0	–	400	1200	ns
			10	–	200	600	
			15	–	150	450	
Three-State Enable/Disable Output Delay	2	$t_{(\overline{T})}$	5.0	–	400	1200	ns
			10	–	160	480	
			15	–	120	360	
Latch to Output Propagation Delay	1	$t_{\overline{LE}}$	5.0	–	500	1500	ns
			10	–	200	600	
			15	–	150	450	

*The formula given is for the typical characteristics only

LOGIC DIAGRAM

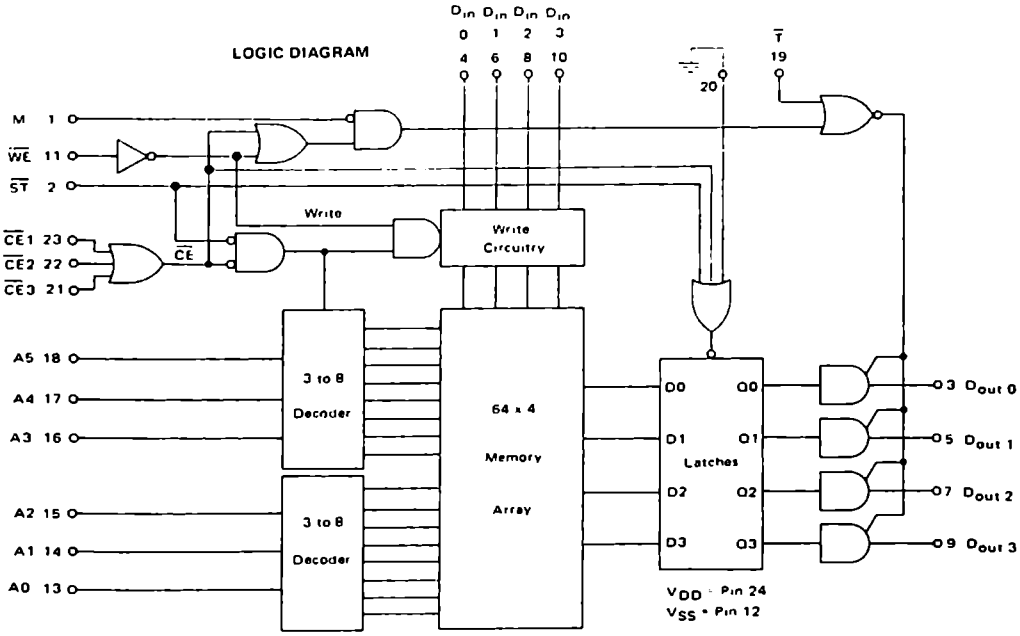
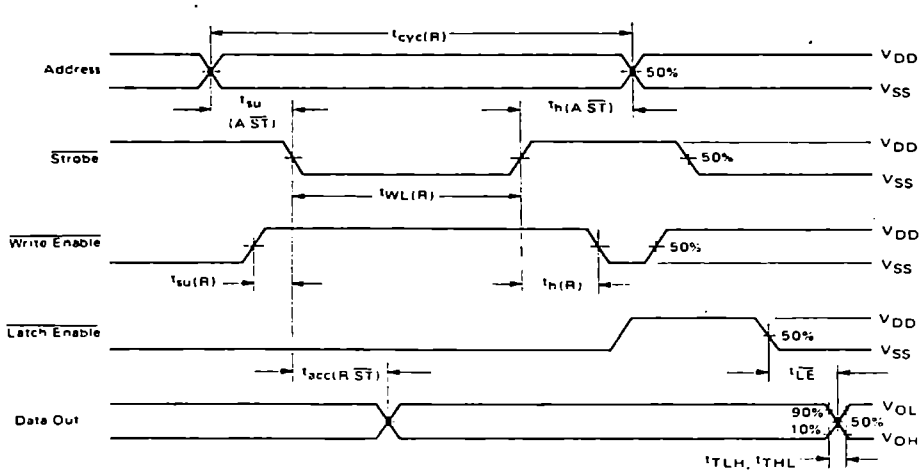
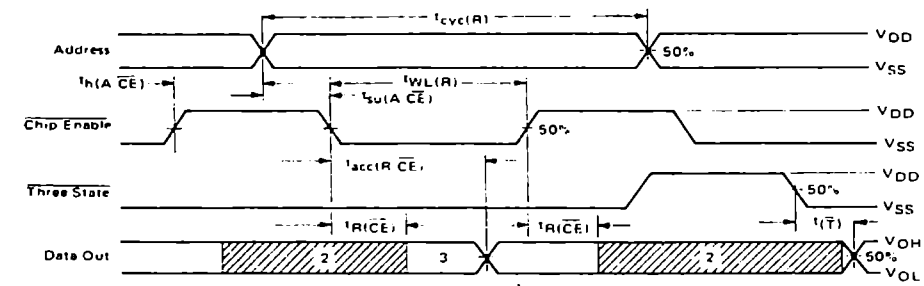


FIGURE 1 – READ CYCLE WAVEFORMS UTILIZING STROBE TO ACCESS MEMORY



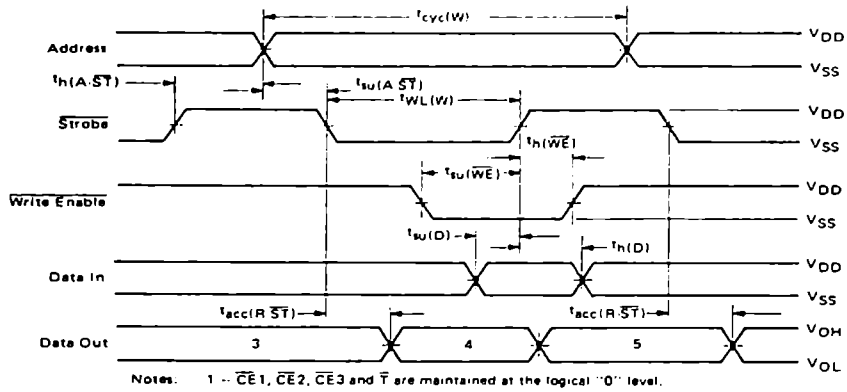
Notes 1 $\overline{CE}1$, $\overline{CE}2$, $\overline{CE}3$ and $\overline{T}$ are low, M is high.
2 $\overline{WE}$ may be held high during the complete read cycle.

FIGURE 2 – READ CYCLE WAVEFORMS UTILIZING CHIP ENABLE TO ACCESS MEMORY



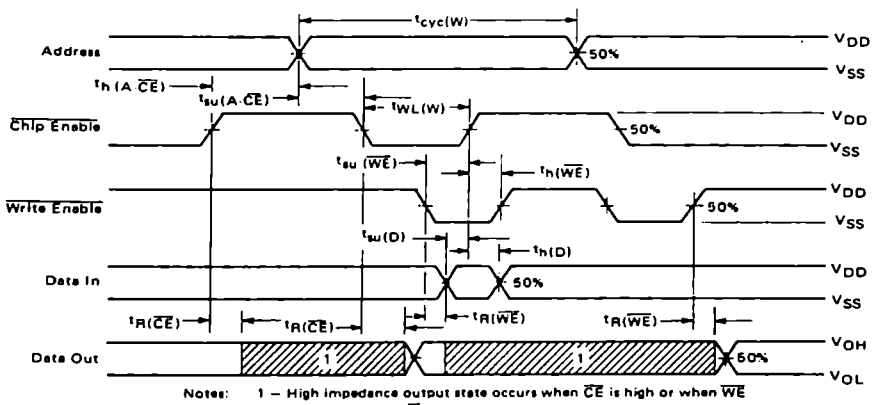
Notes 1 Unused $\overline{CE}$, $\overline{ST}$, M and $\overline{T}$ are low and $\overline{WE}$ is high.
2 High impedance output state occurs when any $\overline{CE}$ is high and M is low, or when $\overline{T}$ is high.
3 The output displays data from the previous state.
4 $t_{WL(R)} + t_{acc(R\overline{CE})max}$

FIGURE 3 – WRITE CYCLE WAVEFORMS UTILIZING STROBE



Notes: 1 – $\overline{CE}1$, $\overline{CE}2$, $\overline{CE}3$ and $\overline{T}$ are maintained at the logical "0" level.
2 – M is maintained at the logical "1" level.
3 – The output displays the contents of the previous state.
4 – The output displays the contents of the presently addressed location as in a read modify write cycle.
5 – The output displays the data that was written into addressed location.

FIGURE 4 – WRITE CYCLE WAVEFORM UTILIZING CHIP ENABLE



Notes: 1 – High impedance output state occurs when $\overline{CE}$ is high or when $\overline{WE}$ is low, for M and $\overline{T}$ maintained in the low state.
2 – Unused $\overline{CE}$'s, $\overline{ST}$, M and $\overline{T}$ are maintained at the logical "0" level.

TRUTH TABLE

Function	$\overline{CE}$ 1	CE 2	$\overline{CE}$ 3	T	$\overline{LE}$	M	$\overline{ST}$	$\overline{WE}$	D_{in}	D_{out}	Comments
Address Changing Valid	X	X	X	X	X	X	1	X	X	R/A	D_{out} will be active if all $\overline{CE}$ = 0, 1 = 0 and $\overline{WE}$ = 1 and M = 1 and T = 0
	X	X	*	X	X	X	X	X	X	R/A	
	X	*	X	X	X	X	X	X	X	R/A	
	*	X	X	X	X	X	X	X	X	R/A	
Address Changing Not Valid	0	0	0	X	X	X	0	X	X	R/A	D_{out} will be set next T = 0 and $\overline{WE}$ = 1 and M = 1 and T = 0
D_{out} Disabled (in high impedance state)	X	X	1	X	X	0	X	X	X	R	Disables write circuitry
	X	1	X	X	X	0	X	X	X	R	
	*	X	X	X	X	0	X	X	X	R	
	X	X	X	*	X	X	X	X	X	R	T = 1 always disables D_{out}
	X	X	X	X	X	0	X	0	X	R	M = 0 and write operation disables D_{out}
D_{out} Enabled (in active state)	0	0	0	0	X	X	X	1	X	A	Read operation, D_{out} active
	X	X	X	0	X	1	X	X	X	A	Read or write, D_{out} active
Read And Load Memory (simultaneously)	0	0	0	X	0	X	0	X	X	R/A	If $\overline{WE}$ = 0, D_{in} = D_{out}
Data Retention	X	X	X	X	X	X	X	X	X	R/A	
	X	X	X	X	X	X	X	X	X	R/A	
	1	X	X	X	X	X	X	X	X	R/A	
	X	X	X	X	X	X	1	X	X	R/A	
	X	X	X	X	X	1	X	X	0	R/A	
Write Into Memory	0	0	0	X	X	X	0	0	X	R/A	
Write Disabled	X	X	X	X	X	X	X	X	X	R/A	
	X	1	X	X	X	X	X	X	X	R/A	
	X	X	X	X	X	X	X	X	X	R/A	
	X	X	X	X	X	X	1	X	X	R/A	
	X	X	X	X	X	X	X	1	X	R/A	
Output Latch Enabled	0	0	0	X	0	X	0	X	X	R/A	
Output Latch Disabled	X	X	1	X	X	X	X	X	X	R/A	
	X	1	X	X	X	X	X	X	X	R/A	
	1	X	X	X	X	X	X	X	X	R/A	
	X	X	X	X	1	X	X	X	X	R/A	
	X	X	X	X	X	X	1	X	X	R/A	

R = High-impedance state of D_{out}

A = Active (normal state, V_{DD} or V_{SS})

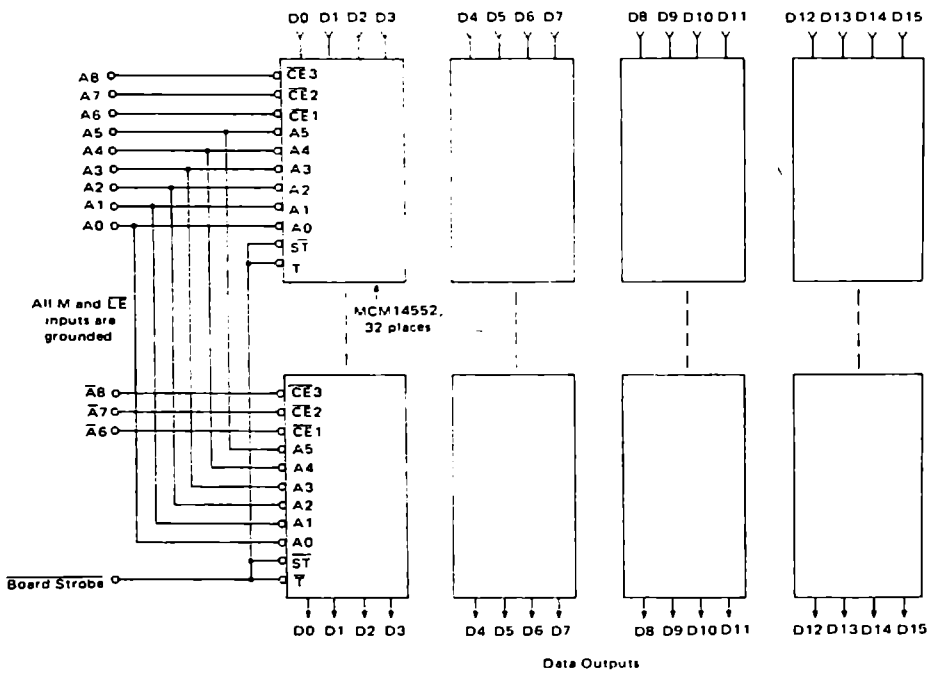
R/A = R or A, depending upon conditions of the other control inputs

X = Don't Care (can be high or low, but not floating)

1 = A or R, but not V_{DD}

0 = Active (normal V_{SS})

FIGURE 5 – 512 WORD x 16 BIT MEMORY BOARD



MOTOROLA

MCM5101
MCM51L01

256 × 4 BIT STATIC RAM

The MCM5101 family of CMOS RAMs offers ultra-low power and fully static operation with a single 5-volt supply. These CMOS 1024-bit devices are organized in 256 words by 4 bits. Separate data inputs and data outputs permit maximum flexibility in bus-oriented systems. Data retention at a power supply as low as 2.0 volts over temperature readily allows design into applications using battery backup for nonvolatility. The MCM5101 is fully static and does not require clocking in standby mode.

The MCM5101 is fabricated using the Motorola advanced ion-implanted, silicon-gate technology for high performance and high reliability.

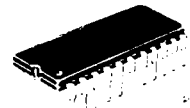
- Low Standby Power
- Fast Access Time
- Single −5.0 Volt Supply
- Fully TTL Compatible — All Inputs and Outputs
- Three-State Output
- Fully Static Operation
- Data Retention to 2.0 Volts
- Direct Replacement for
  - Intel 5101 Series
  - AMI S5101 Series
  - Hitachi HM435101 Series
- Pin Replacement for Harris HM6501 Series

CMOS

(COMPLEMENTARY MOS)

1024-BIT STATIC RANDOM ACCESS MEMORY

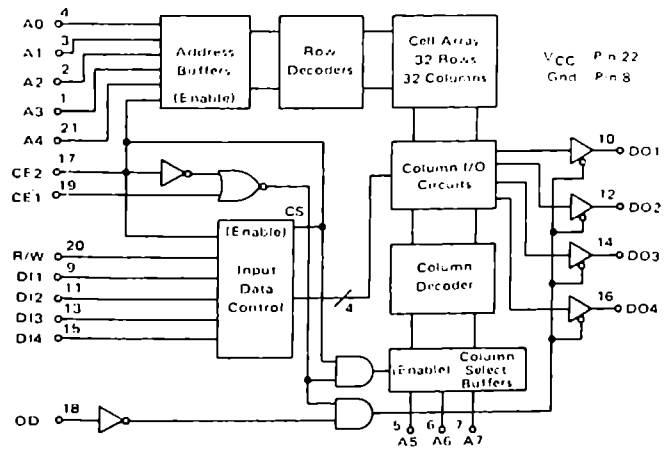
C SUFFIX
CERDIP PACKAGE
CASE 715-07



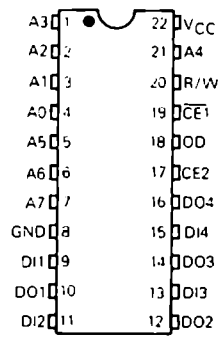
P SUFFIX
PLASTIC PACKAGE
CASE 709-09

Type Number	Typical Current @2 V (μA)	Typical Current @ 5 V (μA)	Max Access (ns)
MCM51L01C45, P45	0.14	0.2	450
MCM51L01C65, P65	0.14	0.2	650
MCM5101C65, P65	0.70	1.0	650
MCM5101C80, P80	-	10	800

BLOCK DIAGRAM



PIN ASSIGNMENT



TRUTH TABLE

$\overline{CE1}$	CE2	OD	R/W	D_{in}	Output	Mode
H	X	X	X	X	High-Z	Not Selected
X	L	X	X	X	High-Z	Not Selected
X	X	H	H	X	High-Z	Output Disabled
L	H	H	L	X	High-Z	Write
L	H	L	L	X	D_{in}	Write
L	H	L	H	X	D_{out}	Read

DS9828/9-80

MAXIMUM RATINGS (Voltages referenced to V_{SS} Pin 8)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{CC}	−0.5 to +7.0	V
Voltage on Any Pin	V_{in}	−0.3 to V_{CC}+0.3	V
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC} V_{SS}	4.75 0	5.0 0	5.25 0	V
Logic 1 Voltage, All Inputs	V_{IH}	2.2	—	V_{CC}+0.3	V
Logic 0 Voltage, All Inputs	V_{IL}	−0.3	—	0.65	V

DC CHRACTERISTICS

Characteristic	Symbol	MCM51L01-45 MCM51L01-65			MCM5101-65			MCM5101-80			Unit
		Min	Typ(1)	Max	Min	Typ(1)	Max	Min	Typ(1)	Max	
Input Current	I_{in}(2)	—	5.0	1	—	5.0	—	—	5.0	—	nA
Input High Voltage	V_{IH}	2.2	—	V_{CC}+0.3	2.2	—	V_{CC}+0.3	2.2	—	V_{CC}+0.3	V
Input Low Voltage	V_{IL}	−0.3	—	0.65	−0.3	—	0.65	−0.3	—	0.65	V
Output High Voltage (I_{OH} = −1.0 mA)	V_{OH}	2.4	—	—	2.4	—	—	2.4	—	—	V
Output Low Voltage (I_{OL} = 2.0 mA)	V_{OL}	—	—	0.4	—	—	0.4	—	—	0.4	V
Output Leakage Current (CE1 = 2.2 V, V_{OL} = 0 V to V_{CC})	I_{LO}(2)	—	—	±1.0	—	—	±1.0	—		±2.0	μA
Operating Current (V_{in} = V_{CC}, except CE1 ≤ 0.65 V, outputs open)	I_{CC1}	—	9.0	22	—	9.0	22	—	11	25	mA
Operating Current (V_{in} = 2.2 V, Except CE1 ≤ 0.65 V, outputs open)	I_{CC2}	—	13	27	—	13	27	—	15	30	mA
Standby Current (CE2 ≤ 0.2 V, V_{in} = 0 V or V_{CC})	I_{CCL}(2)(4)	—	—	10	—	—	200	—	—	500	μA

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, V_{CC} = 5 V periodically sampled rather than 100% tested)

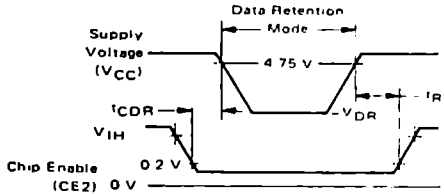
Characteristic	Symbol	Typ	Max	Unit
Input Capacitance (V_{in} = 0 V)	C_{in}	4.0	8.0	pF
Output Capacitance (V_{out} = 0 V)	C_{out}	8.0	12.0	pF

LOW V_{CC} DATA RETENTION CHARACTERISTICS (Excluding MCM5101-80)

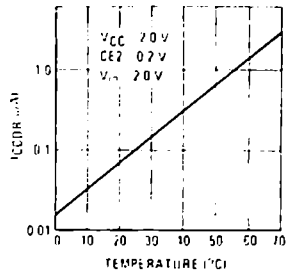
Parameter	Test Conditions		Symbol	Min	Typ(1)	Max	Unit
V_{CC} for Data Retention	CE2 ≤ 0.2 V		V_{DR}	2.0	—	—	V
MCM51L01-45, -65 Data Retention Current		V_{DR} = 2.0 V	I_{CCDR1}	—	0.14	10	μA
MCM5101-65 Data Retention Current		V_{DR} = 2.0 V	I_{CCDR2}	—	0.70	200	μA
Chip Deselect to Data Retention Time			t_{CDR}	0	—	—	ns
Operation Recover Time			t_R	t_{RC}(3)	—	—	ns

Notes:
1. Typical values are T_A = 25°C and nominal supply voltage
2. Current through all inputs and outputs included in I_{CCL} measurement
3. t_{RC} = Read Cycle Time
4. Low current state is for CE2 = 0 only

LOW V_{CC} DATA RETENTION WAVEFORM



TYPICAL I_{CCDR} vs TEMPERATURE



AC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature unless otherwise noted)

Input Pulse Levels	−0.65 V to 2.2 V	Output Load	1 TTL Gate and C_L = 100 pF
Input Rise and Fall Times	20 ns	Timing Measurement Reference Level	1.5 V

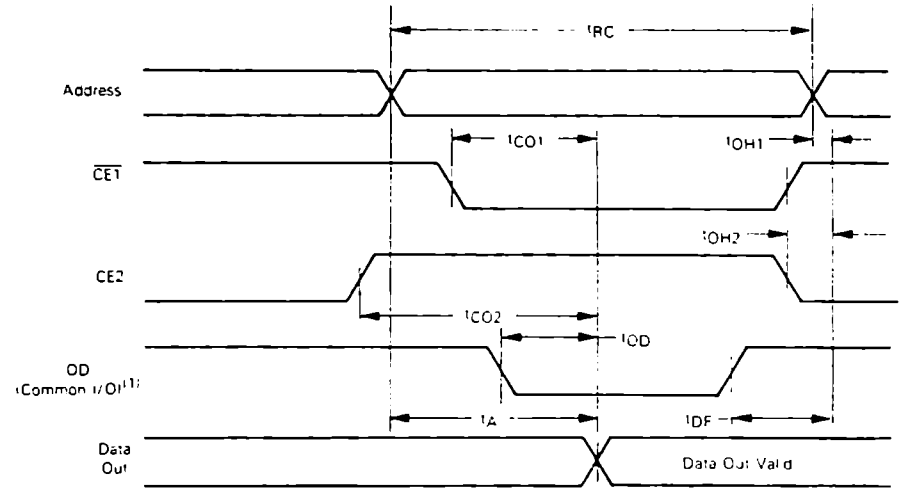
READ CYCLE

Parameter	Symbol	MCM51L01-45		MCM51L01-65 MCM5101-65		MCM5101-80		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle	t_{RC}	450	–	650	–	800	–	ns
Access Time	t_A	–	450	–	650	–	800	ns
Chip Enable (CE1) to Output	t_{CO1}	–	400	–	600	–	800	ns
Chip Enable (CE2) to Output	t_{CO2}	–	500	–	700	–	850	ns
Output Disable to Output	t_{OD}	–	250	–	350	–	450	ns
Data Output to High Z State	t_{DF}	0	130	0	150	0	200	ns
Previous Read Data Valid with Respect to Address Change	t_{OH1}	0	–	0	–	0	–	ns
Previous Read Data Valid with Respect to Chip Enable	t_{OH2}	0	–	0	–	0	–	ns

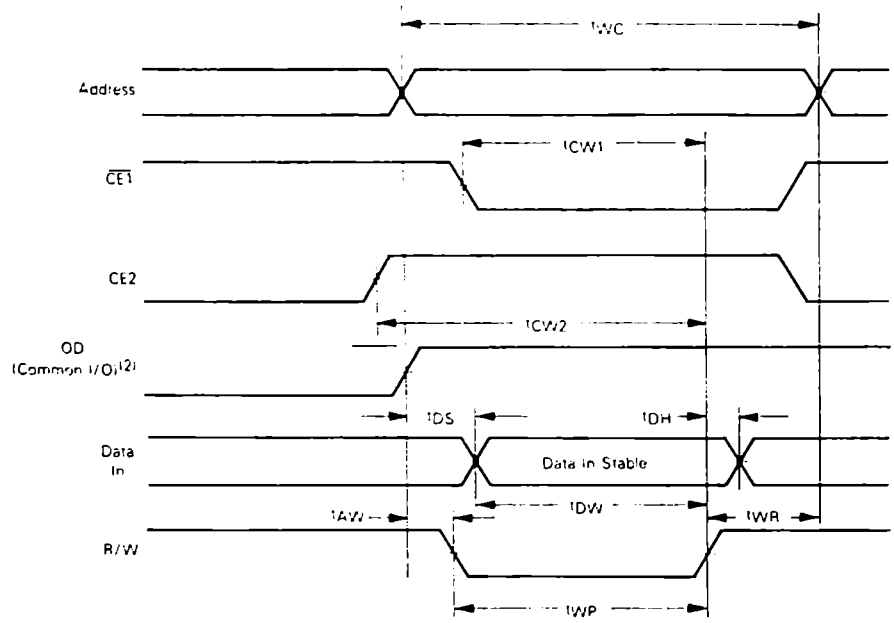
WRITE CYCLE

Parameter	Symbol	MCM51L01-45		MCM51L01-65 MCM5101-65		MCM5101-80		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle	t_{WC}	450	–	650	–	800	–	ns
Write Delay	t_{AW}	130	–	150	–	200	–	ns
Chip Enable (CE1) to Write	t_{CW1}	350	–	550	–	650	–	ns
Chip Enable (CE2) to Write	t_{CW2}	350	–	550	–	650	–	ns
Data Setup	t_{DW}	250	–	400	–	450	–	ns
Data Hold	t_{DH}	50	–	100	–	100	–	ns
Write Pulse	t_{WP}	250	–	400	–	450	–	ns
Write Recovery	t_{WR}	50	–	50	–	100	–	ns
Output Disable Setup	t_{DS}	130	–	150	–	200	–	ns

READ CYCLE TIMING



WRITE CYCLE TIMING



Notes
1. OD may be tied low for separate I/O operation
2. During the write cycle, OD is "high" for common I/O and "don't care" for separate I/O operation

MOTOROLA

MCM6508
MCM6518

1024 × 1 BIT STATIC RANDOM ACCESS MEMORY

The MCM6508 and MCM6518 are fully static 1024 × 1 RAMs fabricated using CMOS silicon gate technology. They offer low power operation from a single +5 V supply with data retention to 2.0 V. The 16-pin MCM6508 has a single active low chip enable. The MCM6518 has two select lines, in addition to the chip enable. Both part types latch addresses with chip enable. The MCM6518 is especially suitable for multiplexed bus microprocessors like the MC146805.

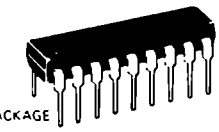
- Low Standby and Operating Power
- Single ±10% 5 V Supply
- Data Retention to 2.0 V
- Fast Access Time
- Address Latches
- Three-State Outputs
- Fully TTL Compatible Inputs/Outputs
- Fully Static Operation
- Direct Replacement For
  Harris HM6508/HM6518
  Intersil IM6508/IM6518

CMOS

(COMPLEMENTARY MOS)

1024 X 1 BIT STATIC RANDOM ACCESS MEMORY

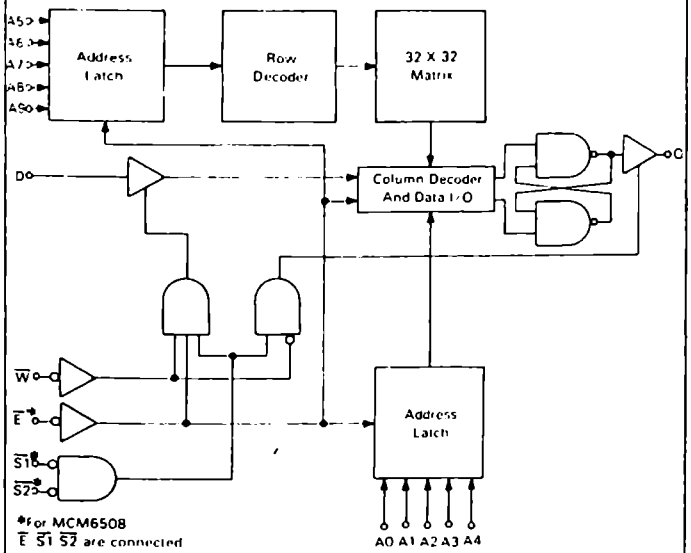
C SUFFIX
FRIT SEAL CERAMIC PACKAGE
CASE 620-06



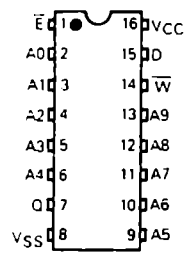
C SUFFIX
FRIT SEAL CERAMIC PACKAGE
CASE 726-02

Type Number	Package Suffixes	Typical Current 2 V	Typical Current 5 V	Maximum Access Time	Operating Temperature Range
MCM6508-25/MCM6518-25	C/P	0.1 μA	0.1 μA	250 ns	0 to 70°C
MCM6508-30/MCM6518-30	C/P	1 μA	1 μA	300 ns	0 to 70°C
MCM6508-46/MCM6518-46	C/P	1 μA	1 μA	460 ns	0 to 70°C

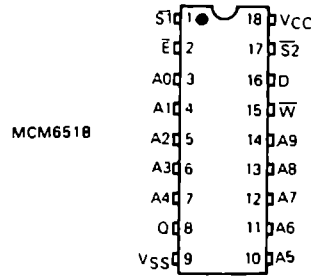
MCM6508 AND MCM6518 FUNCTIONAL BLOCK DIAGRAM



PIN ASSIGNMENTS



MCM6508



MCM6518

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields, however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit.

DS9829/10-80

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{CC}	-0.5 to 7.0	V
Voltage on Any Pin	V_{in}	-0.3 to V_{CC} + 0.3	V
Operating Temperature Range	T_A	0 to 70	°C
Storage Temperature Range	T_{stg}	-65 to 150	°C

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted)

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC} V_{SS}	4.5 0	5.0 0	5.5 0	V
Logic 1 Voltage, All Inputs	V_{IH}	V_{CC} - 2.0	–	V_{CC}	V
Logic 0 Voltage, All Inputs	V_{IL}	-0.3	–	0.8	V

DC CHARACTERISTICS

Characteristic	Symbol	MCM6508-25 MCM6518-25			MCM6508-30, -46 MCM6518-30, -46			Unit
		Min	Typ[1]	Max	Min	Typ[1]	Max	
Input Current	I_{in}	–	5.0	–	–	5.0	–	nA
Output High Voltage (I_{OH} = -1.0 mA)	V_{OH}	2.4	–	–	2.4	–		V
Output Low Voltage (I_{OL} = 2.0 mA)	V_{OL}	–	–	0.4	–	–	0.4	V
Output Leakage Current (See Note 1) (V_o = 0 V to V_{CC})	I_{OL}	–	–	±10	–	–	±10	µA
Standby Current (V_{IH} = $\overline{E}$ = S_1 = $\overline{S_2}$ = V_{CC})	I_{DDSB}		0.1	10.0	–	1.0	100	µA
Data Retention Current (V_{DD} = 2.0 V, V_{IH} = $\overline{E}$ = S_1 = $\overline{S_2}$)	I_{DDDR}	–	0.1	10.0	–	1.0	100	µA
Operating Current (t_{ELEH} = 1 µs)	I_{DDOP}	–	1.5		–	1.5	–	mA

Note:
1. Typical values are T_A = 25°C and nominal supply voltage.

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, V_{CC} = +5 V, periodically sampled rather than 100% tested)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance (V_{in} = 0 V)	C_{in}	4.0	8.0	pF
Output Capacitance (V_{out} = 0 V)	C_{out}	8.0	12.0	pF

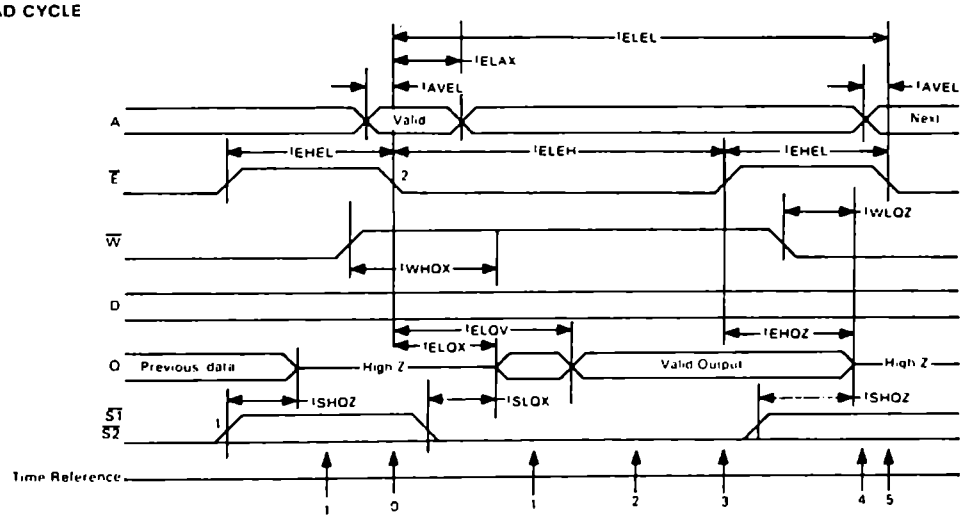
AC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted)

Input Pulse Levels	0.8 V to V_{CC} - 2.0 V	Output Load	1 TTL Gate and C_L = 50 pF
Input Rise and Fall Times	20 ns	Timing Measurement Reference Level	1.5 V

Parameter	Symbol	MCM6508-25 MCM6518-25		MCM6508-30 MCM6518-30		MCM6508-46 MCM6518-46		Units
		Min	Max	Min	Max	Min	Max	
Read or Write Cycle Time	t_{ELEL}	350	–	450	–	730	–	ns
Enable Pulse Width, Low	t_{ELEH}	250	–	300	–	460	–	ns
Enable Pulse Width, High	t_{EHEL}	100	–	150	–	270	–	ns
Enable Access Time	t_{ELQV}	–	250	–	300	–	460	ns
Address Setup	t_{AVEL}	0	–	7	–	15	–	ns
Address Hold	t_{ELAX}	50	–	70	–	130	–	ns
Data Setup	t_{DVWH}	110	–	130	–	270	–	ns
Data Hold	t_{WHDX}	0	–	0	–	0	–	ns
Write Pulse Width	t_{WLWH}	130	–	160	–	270	–	ns
Write Enable to Output Disable	t_{WLQZ}	–	160	–	180	–	285	ns
Output Disable (6508 Only)	t_{EHQZ}	–	160	–	180	–	285	ns
Output Disable (6518 Only)	t_{SHQZ}	–	160	–	180	–	285	ns
Write Disable to Output Enable	t_{WHQX}	–	160	–	180	–	285	ns
Output Enable (6508 Only)	t_{ELQX}	–	160	–	180	–	285	ns
Output Enable (6518 Only)	t_{SLQX}	–	160	–	180	–	285	ns
Select to Write Pulse Setup	t_{WLSH}	130	–	160	–	270	–	ns
Select to Write Pulse Hold	t_{SLWH}	130	–	160	–	270	–	ns
Enable to Write Pulse Setup	t_{WLEH}	130	–	160	–	270	–	ns
Enable to Write Pulse Hold	t_{ELWH}	130	–	160	–	270	–	ns

READ CYCLE



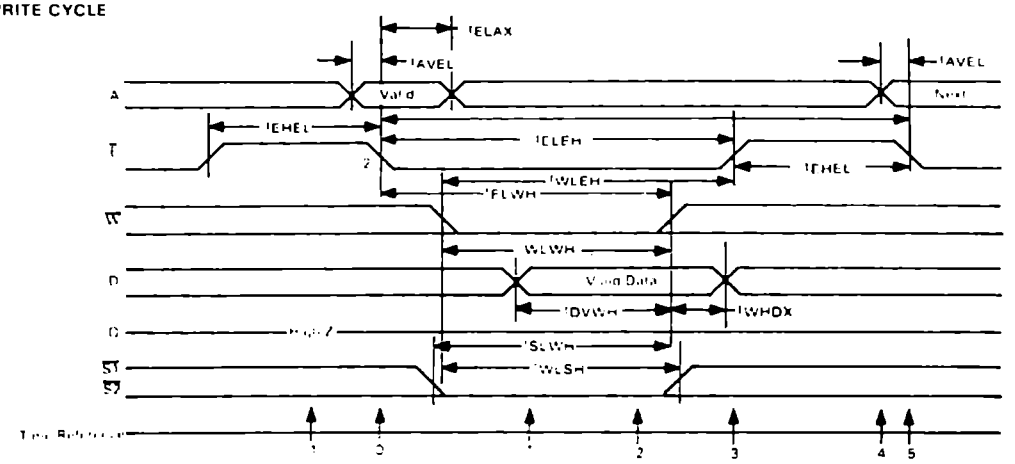
TRUTH TABLE

Time Reference	Inputs					Output	Function
	$\overline{E}$	$\overline{S}$	$\overline{W}$	A	D	Q	
-1	H	H	X	X	X	Z	Disabled
0	↘	X	H	V	X	Z	Address Latched
1	L	L	H	X	X	X	Output Enabled
2	L	L	H	X	X	V	Output Valid
3	↗	L	H	X	X	V	Output Latched
4	H	H	X	X	X	Z	Disabled (Same As -1)
5	↘	X	H	V	X	Z	Next Cycle (Same As 0)

Notes:

1. MCM6518 selected only if both $\overline{S1}$ and $\overline{S2}$ are low and deselected if either $\overline{S1}$ or $\overline{S2}$ is high. $\overline{S1}$ and $\overline{S2}$ are connected to $\overline{E}$ on MCM6508.
2. The address within the memory will change only on falling $\overline{E}$.

WRITE CYCLE



TRUTH TABLE

Time Reference	Inputs					Output	Function
	$\overline{E}$	$\overline{S}$	$\overline{W}$	A	D	Q	
-1	H	X	X	X	X	Z	Disabled
0	↘	X	X	V	X	Z	Address Latched
1	L	L	↘	X	V	Z	Write Mode
2	L	↘	L	X	V	Z	Data Written
3	↘	X	X	X	X	Z	Write Completed
4	H	X	X	X	X	Z	Disabled (Same As -1)
5	↘	X	X	V	X	Z	Next Cycle (Same As 0)

Notes

MOTOROLA

MCM65116

Product Preview

2048 × 8-BIT STATIC RANDOM ACCESS MEMORY

The MCM65116 is a 16,384-bit Static Random Access Memory organized as 2048 words by 8-bits, fabricated using Motorola's high-performance silicon-gate complementary metal oxide semiconductor (HCMOS) technology. It uses a design approach which provides the simple timing features associated with fully static memories and the reduced power associated with CMOS memories. This means low standby power without the need for clocks, nor reduced data rates due to cycle times that exceed access time.

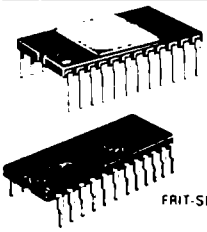
Chip Enable ($\overline{E}$) controls the power-down feature. It is not a clock but rather a chip control that affects power consumption. In less than a cycle time after chip enable ($\overline{E}$) goes high, the part automatically reduces its power requirements and remains in this low-power standby as long as the chip enable ($\overline{E}$) remains high. The automatic power-down feature causes no performance degradation.

The MCM65116 is in a 24-pin dual-in-line package with the industry standard pinout and is pinout compatible with the industry standard 16K EPROM/ROM.

- 2048 Words by 8-Bit Organization
- HCMOS Technology
- Single +5 V Supply
- Fully Static, No Clock or Timing Strobe Required
- Industry Standard 24-Pin Package
- Maximum Access Time
  - MCM65116-12 – 120 ns
  - MCM65116-15 – 150 ns
  - MCM65116-20 – 200 ns
- Power Dissipation
  - 80 mA Maximum (Active)
  - 15 mA Maximum (Standby)
- Fully TTL Compatible
- Automatic Power-Down
- Pinout Compatible with Industry Standard 2716 16K EPROM and Mask Programmable ROM

CMOS
(COMPLEMENTARY MOS)

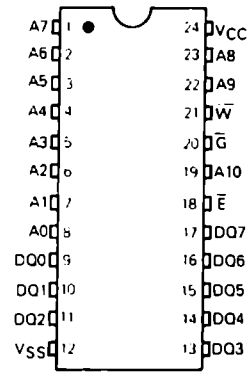
2,048 × 8 BIT STATIC RANDOM ACCESS MEMORY



L SUFFIX
CERAMIC PACKAGE
CASE 716

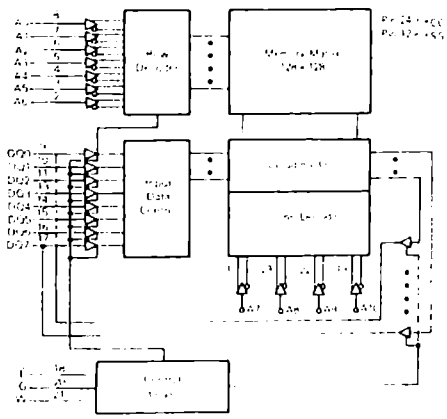
C SUFFIX
FRIT-SEAL CERAMIC PACKAGE
CASE 623

PIN ASSIGNMENTS



PIN NAMES	
A0-A10	Address Input
DQ0-DQ7	Data Input/Output
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
$\overline{E}$	Chip Enable
V_{CC}	Power (+5 V)
V_{SS}	Ground

BLOCK DIAGRAM



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NP330/11-80

MOTOROLA

MCM65147

Product Preview

4096-BIT STATIC RANDOM ACCESS MEMORY

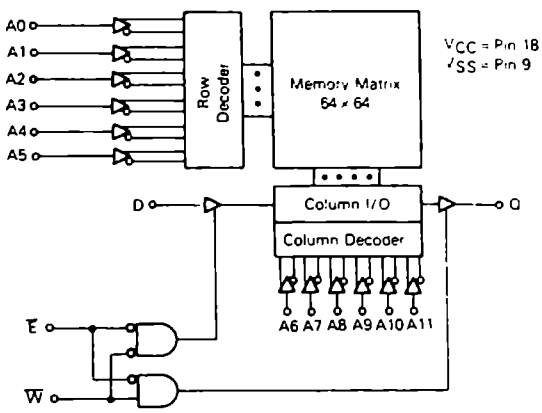
The MCM65147 is a 4096-bit static Random Access Memory organized as 4096 words by 1-bit, fabricated using Motorola's high performance CMOS silicon gate technology (HCMOS). It uses a design approach which provides the simple timing features associated with fully static memories and the reduced power associated with CMOS memories. This means low power without the need for clocks, nor reduced data rates due to cycle times that exceed access times.

Chip enable ($\overline{E}$) controls the power-down feature. It is not a clock, but rather a chip control that affects power consumption. After $\overline{E}$ goes high, initiating deselect mode, the part automatically reduces its power requirements and remains in this low-power standby mode as long as $\overline{E}$ remains high.

The MCM65147 is in an 18-pin dual in-line package with the industry standard pinout. It is TTL compatible in all respects. The data out has the same polarity as the input data. A data input and a separate three-state output provide flexibility and allow easy OR-ties.

- Single +5 V Supply
- Fully Static Memory — No Clock or Timing Strobe Required
- Automatic Power Down
- Low Power Dissipation
  - 75 mW Typical (Active)
  - 500 µW Typical (Standby)
- Directly TTL Compatible — All Inputs and Output
- Separate Data Input and Three-State Output
- Equal Access and Cycle Time
- Maximum Access Time
  - MCM65147-55 = 55 ns
  - MCM65147-70 = 70 ns
- High Density 18-Pin Package

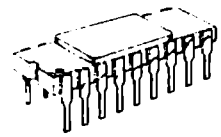
BLOCK DIAGRAM



CMOS

(COMPLIMENTARY MOS)

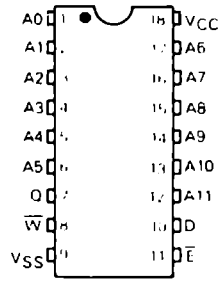
4,096 × 1 BIT
STATIC RANDOM
ACCESS MEMORY



L SUFFIX
CERAMIC PACKAGE
CASE 680

C SUFFIX
FRIT SEAL CERAMIC PACKAGE
CASE 726

PIN ASSIGNMENTS



PIN NAMES	
A0-A11	Address
$\overline{E}$	Chip Enable
D	Data In
Q	Data Out
$\overline{W}$	Write
V_{CC}	Power (+5 V)
V_{SS}	Ground

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NP328/11-80

MOTOROLA

MCM65148

Product Preview

4096-BIT STATIC RANDOM ACCESS MEMORY

The MCM65148 is a 4096-bit Random Access Memory organized as 1024 words by 4-bits, fabricated using Motorola's high-performance silicon-gate complementary metal oxide semiconductor (HCMOS) technology. For ease of use, the device operates from a single power supply, is directly compatible with TTL and requires no clocks or refreshing because of its fully static design. Data access is particularly simple, since address setup times are not required. The output data has the same polarity as the input data.

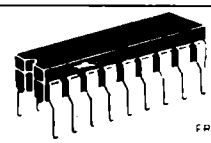
The MCM65148 is designed for memory applications where simple interfacing is the design objective. The MCM65148 is assembled in an 18-pin dual-in-line package with the industry standard pinout. A chip enable ($\overline{E}$) lead allows easy selection of an individual package when the three-state outputs are OR-tied.

- 1024 Words by 4-Bit Organization
- HCMOS Technology
- Single +5 V Supply
- No Clock or Timing Strobe Required
- Industry Standard 18-Pin Configuration
- Maximum Access Time
  - MCM65148-70 – 70 ns
  - MCM65148-85 – 85 ns
- Automatic Power Down
- Power Dissipation
  - 200 mW Typical (Active)
  - 100 µW Typical (Standby)
- Fully TTL Compatible
- Common Data Inputs and Outputs
- Three-State Outputs for OR-Ties

CMOS

(COMPLEMENTARY MOS)

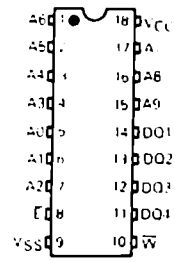
4096-BIT STATIC RANDOM ACCESS MEMORY



C SUFFIX

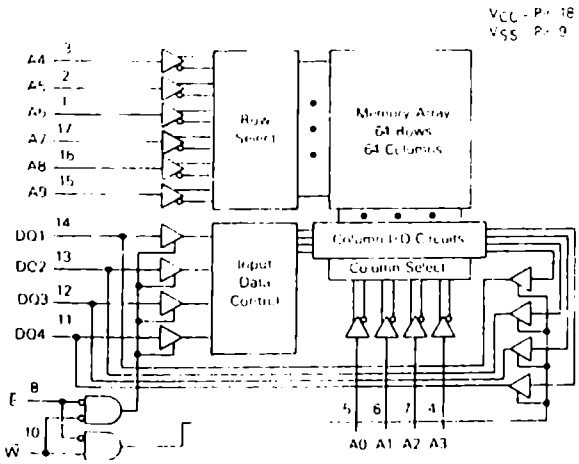
L SUFFIX

PIN ASSIGNMENT



PIN NAMES	
A0-A9	Address Input
$\overline{W}$	Write Enable
$\overline{E}$	Chip Select
DQ1-DQ4	Data Input/Output
V_{CC}	Power (+5 V)
V_{SS}	Ground

BLOCK DIAGRAM



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NP331/11-80

MOTOROLA

MCM14524

1024-BIT READ ONLY MEMORY

The MCM14524 is a complementary MOS mask programmable Read Only Memory (ROM). This device is ordered as a factory special with its unique pattern specified by the user.

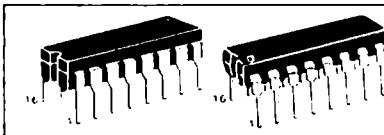
This ROM is organized in a 256 x 4-bit pattern. The contents of a specified address (< A0, A1, A2, A3, A4, A5, A6, A7 >) will appear at the four data outputs (B0, B1, B2, B3) following the negative going edge of the clock. When the clock goes high, the data present at the output will be latched. The memory Enable may be taken low asynchronously, forcing the data outputs low and resetting the output latches. This device finds application wherever low power or high noise immunity is a design consideration.

- Diode Protection on All Inputs
- Noise Immunity - 45% of V_{DD} typical
- Quiescent Current – 10 nA/package typical @ 5 Vdc
- Single Supply Operation – Either Positive or Negative
- Memory Enable Allows Expansion
- Output Latches Provide a Useful Storage Register
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load to Two HTL Loads Over the Rated Temperature Range

CMOS LSI

(LOW POWER COMPLEMENTARY MOS)

1024-BIT
(256 x 4)
READ ONLY MEMORY



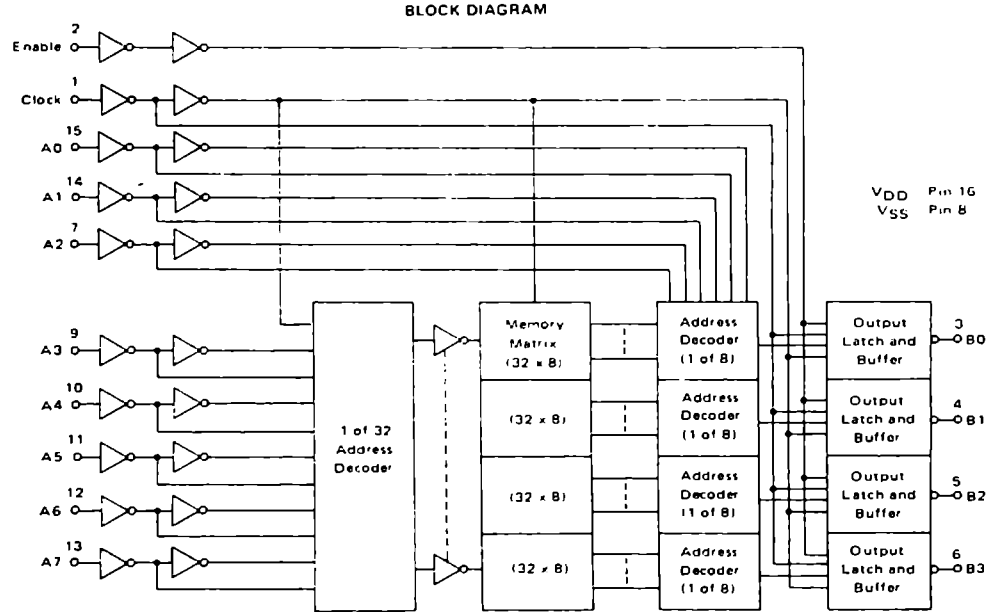
L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14xxx — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

BLOCK DIAGRAM



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}		Vdc
Input Voltage, All Inputs			Vdc
DC Current Drain per Pin		10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A		°C
Storage Temperature Range	T_{stg}		°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high impedance circuit.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage — "0" Level	V_{OL}	5.0	–	0.01	–	0	0.01	–	0.05	Vdc
		10	–	0.01	–	0	0.01	–	0.05	
		15	–	0.01	–	0	0.01	–	0.05	
"1" Level	V_{OH}	5.0	4.99	–	4.99	5.0	–	4.95	–	Vdc
		10	9.99	–	9.99	10	–	9.95	–	
		15	14.99	–	14.99	15	–	14.95	–	
Noise Immunity	V_{NIL}									Vdc
(V_{out} = 0.8 Vdc)		5.0	1.5	–	1.5	2.25	–	1.4	–	
(V_{out} = 1.0 Vdc)		10	3.0	–	3.0	4.50	–	2.9	–	
(V_{out} = 1.5 Vdc)		15	3.75	–	3.75	6.75	–	3.75	–	
(V_{out} = 0.8 Vdc)	V_{NIH}	5.0	1.4	–	1.5	2.25	–	1.5	–	Vdc
(V_{out} = 1.0 Vdc)		10	2.9	–	3.0	4.50	–	3.0	–	
(V_{out} = 1.5 Vdc)		15	3.65	–	3.75	6.75	–	3.75	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) — Source		5.0	-1.2	–	-1.0	-1.7	–	-0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	0.25	–	0.2	0.36	–	0.14	–	
(V_{OH} = 9.5 Vdc)		10	0.62	–	0.5	0.9	–	0.35	–	
(V_{OH} = 13.5 Vdc)		15	1.8	–	1.5	3.5	–	1.1	–	
(V_{OL} = 0.4 Vdc) — Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) — Source		5.0	1.0	–	0.8	1.7	–	0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	0.2	–	0.16	0.36	–	0.12	–	
(V_{OH} = 9.5 Vdc)		10	0.5	–	0.4	0.9	–	0.3	–	
(V_{OH} = 13.5 Vdc)		15	1.4	–	1.1	3.5	–	1.0	–	
(V_{OL} = 0.4 Vdc) — Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	0.1	–	0.00001	0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±1.0	–	0.00001	±1.0	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	–	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	0.010	5.0	–	150	µAdc
(Per Package)		10	–	10	–	0.020	10	–	300	
		15	–	20	–	0.030	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	50	–	0.010	50	–	375	µAdc
(Per Package)		10	–	100	–	0.020	100	–	750	
		15	–	200	–	0.030	200	–	1500	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (1.6 µA/kHz) f + I_{DD}							µAdc
		10	I_T = (3.2 µA/kHz) f + I_{DD}							
		15	I_T = (4.8 µA/kHz) f + I_{DD}							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst case input combination.
†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 1 \times 10^{-3} (C_L - 50) V_{DD} f$
where I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

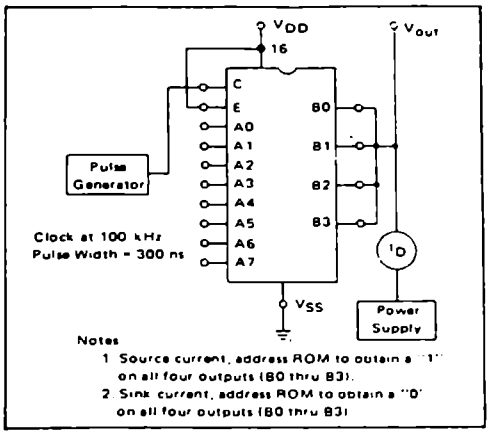
SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH}, t_{THL} = (3.0 ns/pF) C_L + 30 ns		5.0	–	180	360	
t_{TLH}, t_{THL} = (1.5 ns/pF) C_L + 15 ns		10	–	90	180	
t_{TLH}, t_{THL} = (1.1 ns/pF) C_L + 10 ns		15	–	65	130	
Output Fall Time	t_{THL}					ns
t_{TLH}, t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{TLH}, t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{TLH}, t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Clock Read Access Delay Time	t_{accC}					ns
t_{accC} = (1.7 ns/pF) C_L + 1265 ns		5.0	–	1350	4000	
t_{accC} = (0.66 ns/pF) C_L + 517 ns		10	–	550	1600	
t_{accC} = (0.5 ns/pF) C_L + 325 ns		15	–	350	1200	
Enable Access Delay Time	t_{accEn}					ns
t_{accEn} = (1.7 ns/pF) C_L + 160 ns		5.0	–	245	615	
t_{accEn} = (0.66 ns/pF) C_L + 77 ns		10	–	110	265	
t_{accEn} = (0.5 ns/pF) C_L + 50 ns		15	–	75	190	
Clock Pulse Width*	t_{WH}	5.0	450	150	–	ns
		10	165	55	–	
		15	125	35	–	
	t_{WL}	5.0	3600	1200	–	ns
		10	1425	475	–	
		15	1070	300	–	
Maximum Low Clock Pulse Width #	t_{WL}	5.0	2.0	10	–	ms
		10	0.9	3.0	–	
		15	0.1	0.3	–	
Address Setup Time	$t_{su(A)}$	5.0	0	0	–	ns
		10	0	0	–	
		15	0	0	–	
Address Hold Time	$t_{h(A)}$	5.0	0	0	–	ns
		10	0	0	–	
		15	0	0	–	
Clock to Enable Setup Time	$t_{su(cl)}$	5.0	4275	1425	–	ns
		10	1725	575	–	
		15	1295	400	–	
Clock to Enable Hold Time	$t_{h(cl)}$	5.0	150	0	–	ns
		10	75	0	–	
		15	55	0	–	

*The clock can remain high indefinitely with the data remaining latched.

#If clock stays low too long, the dynamically stored data will leak off and will have to be recalled

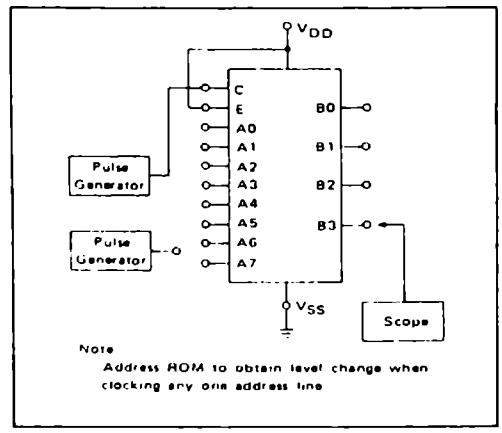
FIGURE 1 – OUTPUT DRIVE CURRENT TEST CIRCUIT



Notes

1. Source current, address ROM to obtain a "1" on all four outputs (B0 thru B3).
2. Sink current, address ROM to obtain a "0" on all four outputs (B0 thru B3).

FIGURE 2 – SWITCHING TIME TEST CIRCUIT (Refer to timing diagram)

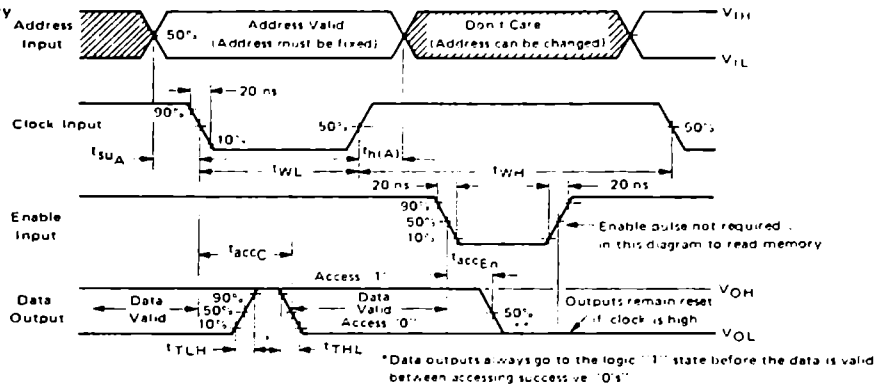


Note

Address ROM to obtain level change when clocking any one address line

MEMORY READ CYCLE TIMING DIAGRAMS

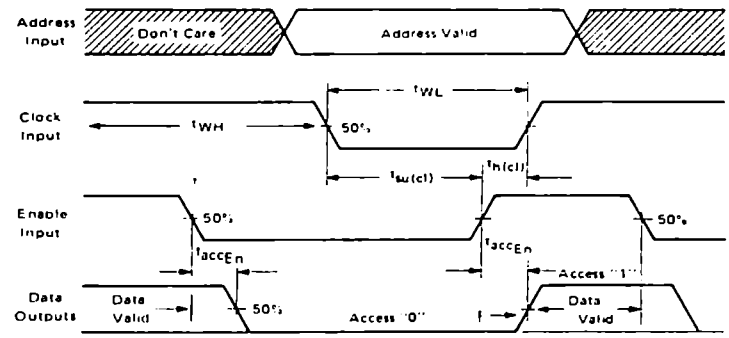
a) Using Clock to Read Memory



*Data outputs always go to the logic "1" state before the data is valid between accessing successive "0"s.

**Outputs forced to "0" by Enable

b) Using the Enable to Read Memory



† In this mode of operation, the negative going edge of Enable should occur on or before the clock negative edge

‡ The data outputs are valid without the logic "1" pulse occurring during the access cycle as shown in a) above.

CUSTOM PROGRAMMING

By the programming of a single photomask for the MCM14524, the customer may specify the content of the memory.

Address Inputs

Words are numbered 0 through 255 and are addressed using sequential addressing of Address leads A0 through A7 with A0 as the least significant digit.

Logic "0" is defined as a "low" Address input (V_{IL}).
Logic "1" is defined as a "high" Address input (V_{IH}).

WORD \ ADDRESS	A7	A6	A5	A4	A3	A2	A1	A0
Word 0	0	0	0	0	0	0	0	0
Word 1	0	0	0	0	0	0	0	1
Word 2	0	0	0	0	0	0	1	0
Word 3	0	0	0	0	0	0	1	1
. .	.	.	.	.	.	.	.	.
. .	.	.	.	.	.	.	.	.
Word 255	1	1	1	1	1	1	1	1

TRUTH TABLE

CLOCK	ENABLE	B0	B1	B2	B3
V_{DD} ⎍ V_{SS}	1	⟨Address⟩	⟨Address⟩	⟨Address⟩	⟨Address⟩
V_{SS} ⎍ V_{DD}	1	OUTPUT DATA LATCHES			
X	0	0	0	0	0

X = Don't Care

*Indicates contents of specified Address will appear at outputs as stated above.

BINARY TO HEXADECIMAL CONVERSION TABLE

BINARY WORD DESIRED	CARD CHARACTER
0 0 0 0	0
0 0 0 1	1
0 0 1 0	2
0 0 1 1	3
0 1 0 0	4
0 1 0 1	5
0 1 1 0	6
0 1 1 1	7
1 0 0 0	8
1 0 0 1	9
1 0 1 0	A
1 0 1 1	B
1 1 0 0	C
1 1 0 1	D
1 1 1 0	E
1 1 1 1	F

Two methods may be used to transmit the custom memory pattern to Motorola

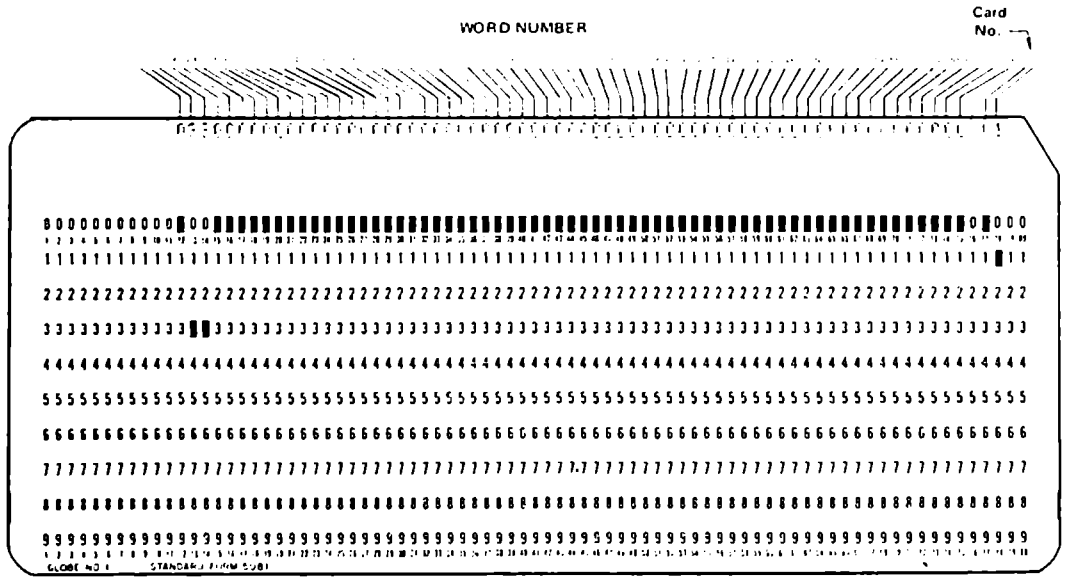
METHOD A. PUNCHED COMPUTER CARDS

A binary coded decimal equivalent of each desired output may be punched in standard computer cards (four cards are required for all 256 words) in numerical (word number) order. 64 words per card are punched in columns 12 thru 75 using the Binary to Hexadecimal conversion table. Columns 77 and 78 are used to number the cards, which must be in numerical order. Please use characters as shown in the table when punching computer cards

ROM SAMPLE WORD PROGRAMMING FOR PUNCHED CARD

WORD NUMBER	ADDRESS INPUTS								SAMPLE WORD OUTPUTS				CARD CHARACTER
	A7	A6	A5	A4	A3	A2	A1	A0	B3	B2	B1	B0	
0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1	0	0	1	1	3
2	0	0	0	0	0	0	1	0	0	0	1	1	3
3	0	0	0	0	0	0	1	1	0	0	0	0	0
.	.	.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.	.	.
255	1	1	1	1	1	1	1	1	1	0	1	0	A

Shown in columns 12 - 15 on card below.



METHOD B: TRUTH TABLE

For customers who do not have access to punch cards, Motorola will accept Truth Tables. When filling out the table, use the 0 to F hexidecimal character in column "C".

CUSTOM PROGRAM for the MCM14524 Read Only Memory

WORD	C
0	
1	
2	
3	
4	
5	
6	
7	
8	
9	
10	
11	
12	
13	
14	
15	
16	
17	
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35	
36	
37	
38	
39	
40	
41	
42	
43	
44	
45	
46	
47	
48	
49	
50	

WORD	C
51	
52	
53	
54	
55	
56	
57	
58	
59	
60	
61	
62	
63	
64	
65	
66	
67	
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87	
88	
89	
90	
91	
92	
93	
94	
95	
96	
97	
98	
99	
100	
101	

WORD	C
102	
103	
104	
105	
106	
107	
108	
109	
110	
111	
112	
113	
114	
115	
116	
117	
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138	
139	
140	
141	
142	
143	
144	
145	
146	
147	
148	
149	
150	
151	
152	

WORD	C
153	
154	
155	
156	
157	
158	
159	
160	
161	
162	
163	
164	
165	
166	
167	
168	
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189	
190	
191	
192	
193	
194	
195	
196	
197	
198	
199	
200	
201	
202	
203	

WORD	C
204	
205	
206	
207	
208	
209	
210	
211	
212	
213	
214	
215	
216	
217	
218	
219	
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245	
246	
247	
248	
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250	
251	
252	
253	
254	
255	

MOTOROLA

MCM65516

Advance Information

2048 × 8 BIT READ ONLY MEMORY

The MCM65516 is a complementary MOS mask programmable byte organized read only memory (ROM). The MCM65516 is organized as 2048 bytes of 8 bits, designed for use in multiplex bus systems. It is fabricated using Motorola's silicon gate CMOS technology, which offers low-power operation from a single 5.0 volt supply.

The memory is compatible with CMOS microprocessors that share address and data lines. Compatibility is enhanced by pins 13, 14, 16, and 17 which give the user the versatility of selecting the active levels of each. Pin 17 allows the user to choose active high, active low or a third option of programming which is termed the "MOTEL" mode. If this mode is selected by the user, it provides direct compatibility with either the Motorola MC146805E2 or Intel 8085 type microprocessor series. In the MOTEL operation the ROM can accept either polarity signal on the data strobe input as long as the signal toggles during the cycle. This unique operational feature makes the ROM an extremely versatile part.

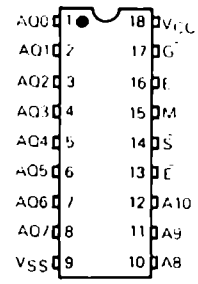
- 2K × 8 CMOS ROM
- 3 to 6 Volt Supply
- Access Time
  - 430 ns (5 V) MCM65516-43
  - 550 ns (5 V) MCM65516-55
- Low Power Dissipation
  - 30 mA Maximum (Active)
  - 50 µA Maximum (Standby)
- Multiplex Bus Directly Compatible With All CMOS Microprocessors (MC146805E2, NSC800)
- Pins 13, 14, 16, and 17 are Mask Programmable
- MOTEL Mask Option Also Insures Direct Compatibility with NMOS Microprocessors Like MC6803, MC6801, 8085, and 8086
- Standard 18 Pin Package

CMOS
(COMPLEMENTARY MOS)

2048 × 8 BIT
MULTIPLEXED BUS
READ ONLY MEMORY

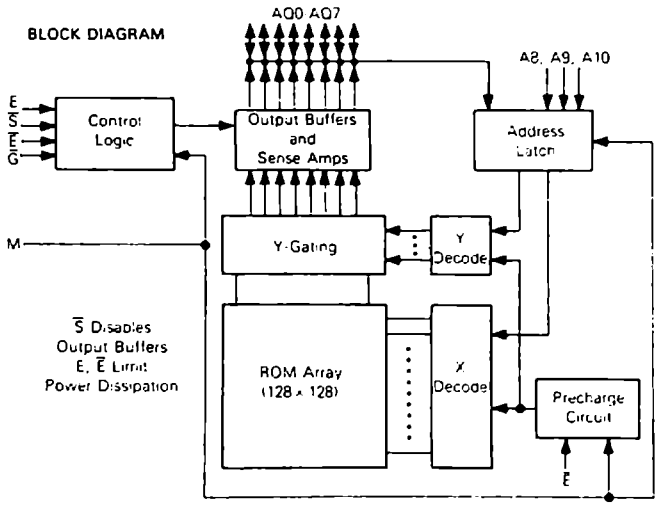
L SUFFIX
CERAMIC PACKAGE
CASE 650-06

PIN ASSIGNMENTS



PIN NAMES	
AQ0-AQ7	Address/Data Output
A8-A10	Address
M	Multiplex Address Strobe
E	Chip Enable
S	Chip Select
G	Data Strobe (Output Enable)

BLOCK DIAGRAM



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields, however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

ADI854/9 60

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	V
Input Voltage	V_{in}	−0.3 to +7.0	V
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted.)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Nom	Max	Unit
Supply Voltage (V_{CC} must be applied at least 100 µs before proper device operation is achieved)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	V_{CC} − 2.0	–	5.5	V
Input Low Voltage	V_{IL}	−0.3	–	0.8	V

RECOMMENDED OPERATING CHARACTERISTICS

Characteristic	Symbol	MCM65516-43		MCM65516-55		Unit	Test Condition
		Min	Max	Min	Max		
Output High Voltage (Source Current = −1.6 mA)	V_{OH}	V_{CC} − 0.4 V	–	V_{CC} − 0.4 V	–	V	
Output Low Voltage (Sink Current = +1.6 mA)	V_{OL}	–	0.4	–	0.4	V	
Supply Current (Operating)	I_{CC1}	–	30	–	30	mA	C_L = 130 pF, V_{in} = V_{IH} to V_{IL}, t_{cyc} = 1.0 µs
Supply Current (DC Active)	I_{CC2}	–	100	–	100	µA	V_{in} = V_{CC} to GND
Standby Current	I_{SB}	–	50	–	75	µA	V_{in} = V_{CC} to GND
Input Leakage	I_{in}	−10	+10	−10	+10	µA	
Output Leakage	I_{OL}	−10	+10	−10	+10	µA	

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, periodically sampled rather than 100% tested.)

Characteristic	Symbol	Max	Unit
Input Capacitance	C_{in}	5	pF
Output Capacitance	C_{out}	12.5	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

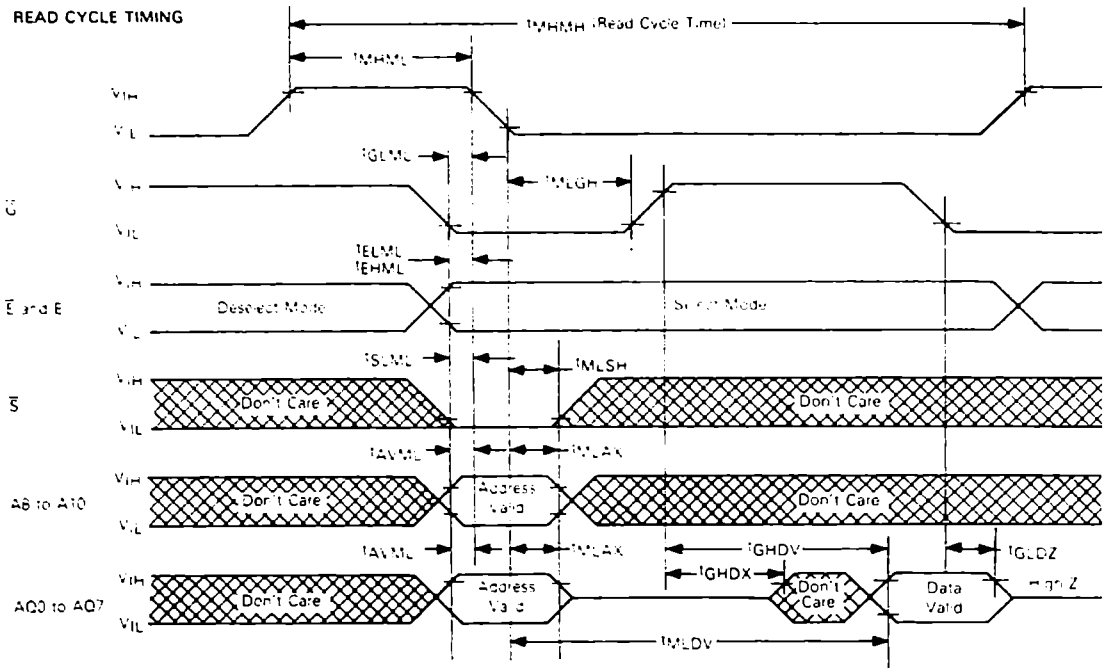
(Full operating voltage and temperature range unless otherwise noted.)

READ CYCLE

C_L = 130 pF

Parameter	Symbol	MCM65516-43		MCM65516-55		Unit
		Min	Max	Min	Max	
Address Strobe Access Time	t_{MLDV}	–	430	–	550	ns
Read Cycle Time	t_{MHMH}	580	–	725	–	ns
Multiplex Address Strobe High to Multiplex Address Strobe Low (Pulse Width)	t_{MHML}	150	–	175	–	ns
Data Strobe Low to Multiplex Address Strobe Low	t_{GLML}	50	–	50	–	ns
Multiplex Address Strobe Low to Data Strobe High	t_{MLGH}	100	–	160	–	ns
Address Valid to Multiplex Address Strobe Low	t_{AVML}	50	–	50	–	ns
Chip Select Low to Multiplex Address Strobe Low	t_{SLML}	50	–	50	–	ns
Multiplex Address Strobe Low to Chip Select High	t_{MLSH}	50	–	80	–	ns
Chip Enable Low/High to Multiplex Address Strobe Low	t_{ELML} t_{EHML}	50 50	– –	50 50	– –	ns
Multiplex Address Strobe Low to Address Don't Care	t_{MLAX}	50	–	80	–	ns
Data Strobe High to Data Valid	t_{GHDV}	175	–	200	–	ns
Data Strobe Low to High-Z	t_{GLDZ}	–	160	–	160	ns
Data Strobe High to Address Don't Care	t_{GHDX}	20	–	20	–	ns

READ CYCLE TIMING



FUNCTIONAL DESCRIPTION

The 2K × 8 bit CMOS ROM (MCM65516) shares address and data lines and, therefore, is compatible with the majority of CMOS microprocessors in the industry. The package size is reduced from 24 pins for standard NMOS ROMs to 18 pins because of the multiplexed bus approach. The savings in package size and external bus lines adds up to tighter board packing density which is handy for battery powered hand carried CMOS systems. This ROM is designed with the intention of having very low active as well as standby currents. The active power dissipation of 150 mW (at V_{CC} = 5 V, freq = 1 MHz) and standby power of 250 µW (at V_{CC} = 5 V) add up to low power for battery operation. The typical access time of the ROM is 280 ns making it acceptable for operation with today's existing CMOS microprocessors.

An example of this operation is shown in Figure 1. Shown is a typical connection with either the Motorola MC146805E2 CMOS microprocessor (M6800 series) or the National NSC800 which is an 8085 or Z80 based system. The main difference between the systems is that the data strobe (DS) on the MC146805E2 and the read bar ($\overline{RD}$) on the 8085 both control the output of data from the ROM but are of opposite polarity. The Motorola 2K × 8 ROM can accept either polarity signal on the data strobe input as long as the signal toggles during the cycle. This is termed the MOTEL mode of operation. This unique operational feature makes the ROM an extremely versatile part. Further operational features are explained in the following section.

Operational Features

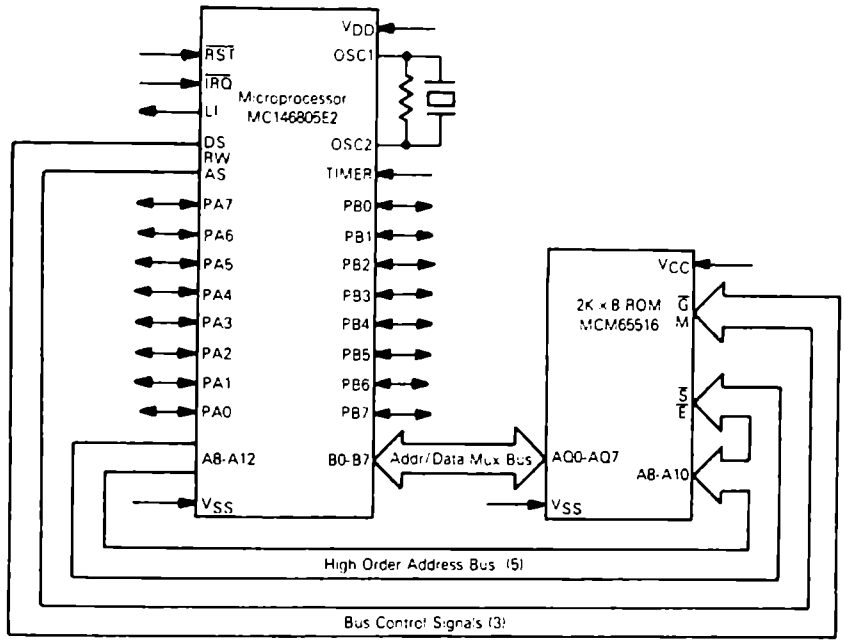
In order to operate in a multiplexed bus sytem the ROM latches, for one cycle, the address and chip select input information on the trailing edge of address strobe (M) so the address signals can be taken off the bus.

Since they are latched, the address and chip select signals have a setup and hold time referenced to the negative edge of address strobe. Address strobe has a minimum pulse width requirement since the circuit is internally precharged during this time and is setup for the next cycle on the trailing edge of address strobe. Access time is measured from the negative edge of address strobe.

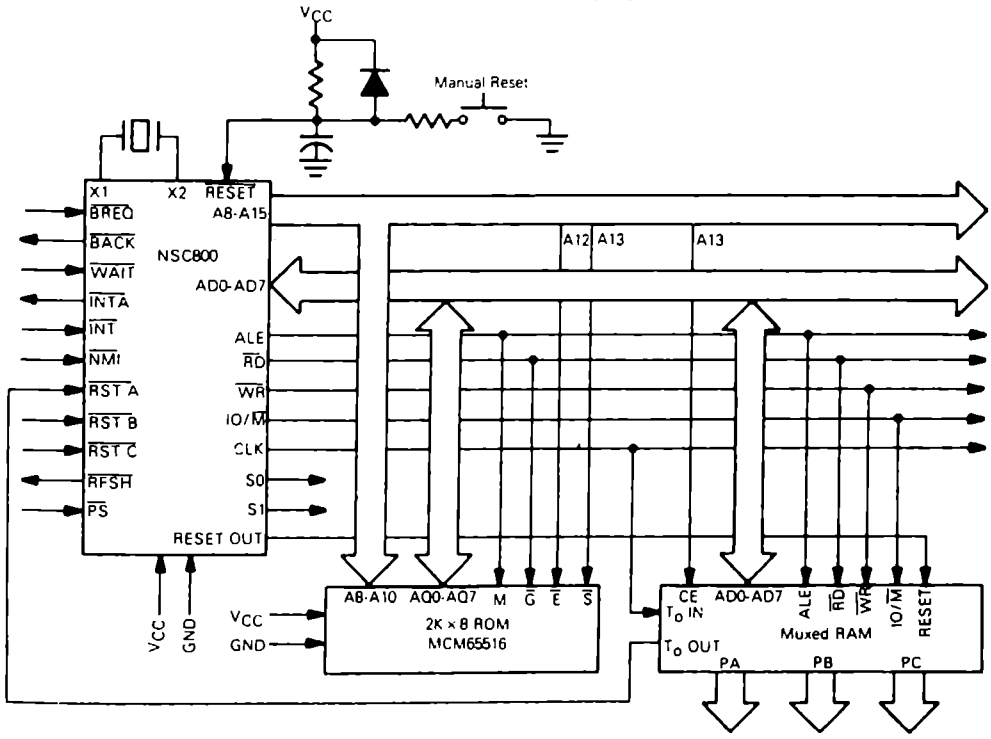
The part is equipped with a data strobe input (G) which controls the output of data onto the bus lines after the addresses are off the bus. The data strobe has three potential modes of operation which are programmable with the ROM array. The first mode is termed the MOTEL mode of operation. In this mode, the circuit can work with either the Motorola or Intel type microprocessor series. The difference between the two series for a ROM peripheral is only the polarity of the data strobe signal. Therefore, in the MOTEL mode the ROM recognizes the state of the data strobe signal at the trailing edge of address strobe (requires a setup and hold time), latches the state into the circuit after address strobe, and turns on the data outputs when an opposite polarity signal appears on the data strobe input. In this manner the data strobe input can work with either polarity signal but that signal must toggle during a cycle to output data on the bus lines. If the data strobe remains at a d.c. level the outputs will remain off. The data strobe input has two other programmable modes of operation and those are the standard static select modes (high or low) where a d.c. input not synchronous with the address strobe will turn the outputs on or off.

The chip enable and chip select inputs are all programmable with the ROM array to either a high or low select. The chip select acts as an additional address and is latched on the address strobe trailing edge. On deselect the chip select merely turns off the output drivers acting as an output disable. It does not power down the chip. The chip enable inputs, however, do put the chip in a power down standby mode but they are not latched with address strobe and must be maintained in a d.c. state for a full cycle.

FIGURE 1
TYPICAL MINIMUM SYSTEM – MOTOROLA



TYPICAL SYSTEM – NATIONAL



CUSTOM PROGRAMMING

By the programming of a single photomask for the MCM65516 the customer may specify the content of the memory and the method of enabling the outputs, or selection of the "MOTEL" option (Pin 17).

Information on the general options of the MCM65516 should be submitted on an Organizational Data form such as that shown in the below figure

Information for custom memory content may be sent to Motorola in one of two forms (shown in order of preference).

1 Magnetic Tape
9 track, 800 bpi, odd parity written in EBCDIC character code Motorola's R O M S. format.
2 EPROMs
One 16K (MCM2716, or TMS2716)

FORMAT FOR PROGRAMMING GENERAL OPTIONS

ORGANIZATIONAL DATA MOS READ ONLY MEMORY

Customer

Company _____

Part No. _____

Originator _____

Phone No _____

Motorola Use Only

Quote _____

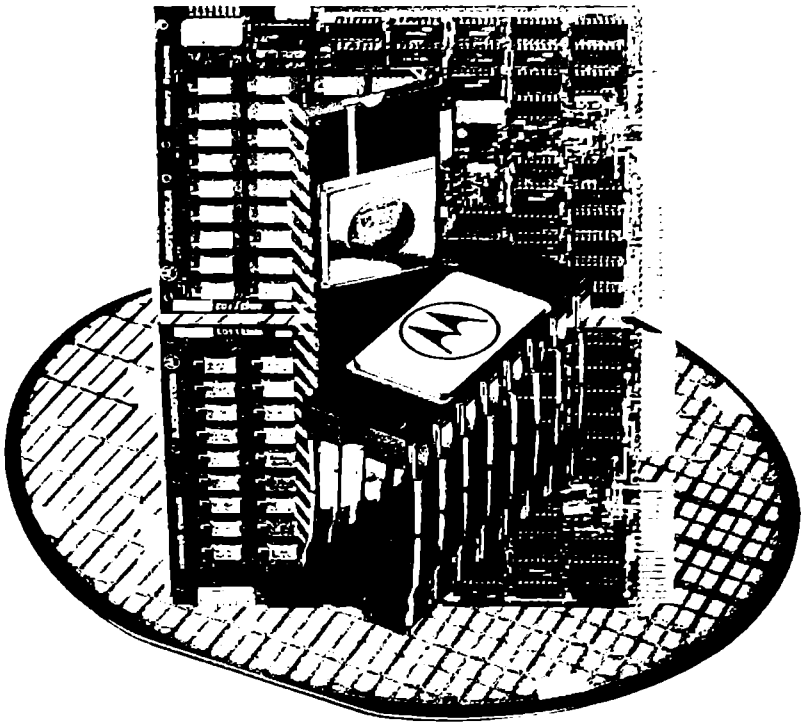
Part No _____

Specif. No. _____

Programmable Pin Options

	13	14	16	17
Active High	☐	☐	☐	☐
Active Low	☐	☐	☐	☐

MOTEL ☐



Bipolar Memories
TTL, MECL-RAM, PROM

MOTOROLA

MCM93415

1024-BIT RANDOM ACCESS MEMORY

The MCM93415 is a 1024-bit Read-Write RAM organized 1024 words by 1 bit.

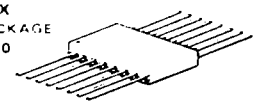
The MCM93415 is designed for buffer control storage and high performance main memory applications, and has a typical access time of 35 ns.

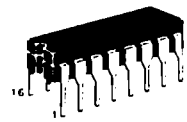
The MCM93415 has full decoding on chip, separate data input and data output lines, and an active low chip select. The device is fully compatible with standard DTL and TTL logic families and features an uncommitted collector output for ease of memory expansion.

- Uncommitted Collector Output
- TTL Inputs and Output
- Non-Inverting Data Output
- High Speed –
  - Access Time – 35 ns Typical
  - Chip Select – 15 ns Typical
- Power Dissipation Decreases with Increasing Temperature
- Power Dissipation 0.5 mW/Bit Typical
- Organized 1024 Words X 1 Bit

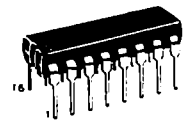
TTL
1024 X 1 BIT
RANDOM ACCESS MEMORY

F SUFFIX
CERAMIC PACKAGE
CASE 650



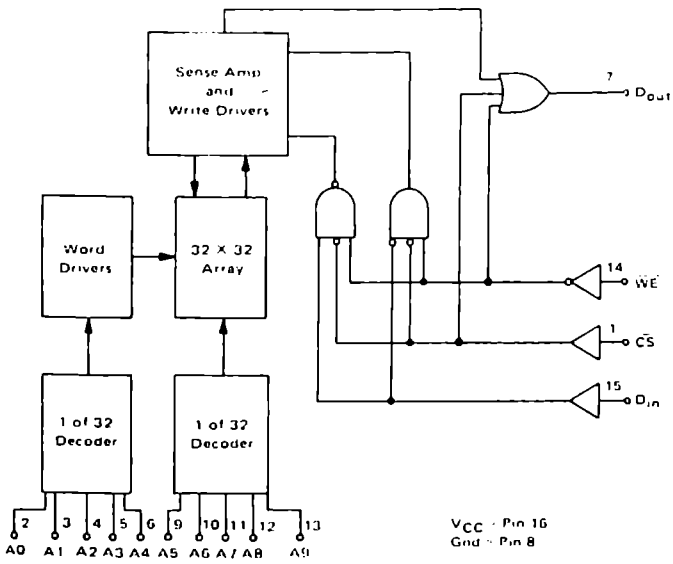


D SUFFIX
CERAMIC PACKAGE
CASE 620

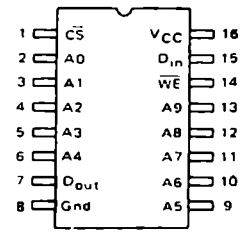


P SUFFIX
PLASTIC PACKAGE
CASE 648

BLOCK DIAGRAM


Sense Amp and Write Drivers
Word Drivers
32 X 32 Array
1 of 32 Decoder
1 of 32 Decoder
7 Dout
14 WE
1 CS
15 Din
2 3 4 5 6 9 10 11 12 13
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9
VCC = Pin 16
Gnd = Pin 8

PIN ASSIGNMENT



Pin Designation

$\overline{CS}$	Chip Select
A0 – A9	Address Inputs
$\overline{WE}$	Write Enable
D_{in}	Data Input
D_{out}	Data Output

FUNCTIONAL DESCRIPTION

The MCM93415 is a fully decoded 1024-bit Random Access Memory organized 1024 words by one bit. Bit selection is achieved by means of a 10-bit address, A0 to A9.

The Chip Select input provides for memory array expansion. For large memories, the fast chip select access time permits the decoding of Chip Select ($\overline{CS}$) from the address without affecting system performance.

The read and write operations are controlled by the state of the active low Write Enable ($\overline{WE}$, Pin 14). With $\overline{WE}$ held low and the chip selected, the data at D_{in} is written into the addressed location. To read, $\overline{WE}$ is held high and the chip selected. Data in the specified location is presented at D_{out} and is non-inverted.

Uncommitted collector outputs are provided to allow wired-OR applications. In any application an external pull-up resistor of R_L value must be used to provide a high at the output when it is off. Any R_L value within the range specified below may be used.

$$\frac{V_{CC(Min)}}{I_{OL} - FO(1.6)} \cdot R_L \cdot \frac{V_{CC(Min)} - V_{OH}}{n(I_{CEX}) + FO(0.04)}$$

R_L is in kΩ
n = number of wired-OR outputs tied together
FO = number of TTL Unit Loads (UL) driven
I_{CEX} = Memory Output Leakage Current
V_{OH} = Required Output High Level at Output Node
I_{OL} = Output Low Current

The minimum R_L value is limited by output current sinking ability. The maximum R_L value is determined by the output and input leakage current which must be supplied to hold the output at V_{OH}. One Unit Load = 40 µA High/1.6 mA Low.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Storage Temperature	
Ceramic Package (D and F Suffix)	-55°C to +165°C
Plastic Package (P Suffix)	-55°C to +125°C
Operating Junction Temperature, T_J	
Ceramic Package (D and F Suffix)	+165°C
Plastic Package (P Suffix)	+125°C
V_{CC} Pin Potential to Ground Pin	-0.5 V to +7.0 V
Input Voltage (dc)	-0.5 V to +5.5 V
Voltage Applied to Outputs (Output High)	-0.5 V to +5.5 V
Output Current (dc) (Output Low)	+20 mA
Input Current (dc)	-12 mA to +5.0 mA

TRUTH TABLE

Inputs			Output	
$\overline{CS}$	$\overline{WE}$	D_{in}	Open Collector	Mode
H	X	X	H	Not Selected
L	L	L	H	Write "0"
L	L	H	H	Write "1"
L	H	X	D_{out}	Read

H = High Voltage Level
L = Low Voltage Level
X = Don't Care (High or Low)

NOTE 1: Device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.

GUARANTEED OPERATING RANGES (Note 2)

Part Number	Supply Voltage (V_{CC})			Ambient Temperature (T_A)
	Min	Nom	Max	
MCM93415DC, PC	4.75 V	5.0 V	5.25 V	0°C to +75°C
MCM93415FM, DM	4.50 V	5.0 V	5.50 V	-55°C to +125°C

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted)

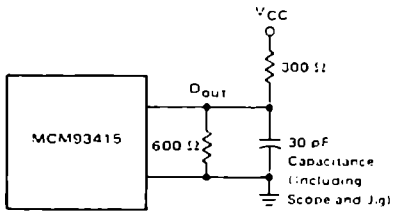
Symbol	Characteristic	Limits		Unit	Conditions	
		Min	Max			
V_{OL}	Output Low Voltage		0.45	Vdc	V_{CC} = Min, I_{OL} = 16 mA	
V_{IH}	Input High Voltage	2.1		Vdc	Guaranteed Input High Voltage for All Inputs	
V_{IL}	Input Low Voltage		0.8	Vdc	Guaranteed Input Low Voltage for All Inputs	
I_{IL}	Input Low Current		-400	µAdc	V_{CC} = Max, V_{in} = 0.4 V	
I_{IH}	Input High Current		40	µAdc	V_{CC} = Max, V_{in} = 4.5 V	
			1.0	mAdc	V_{CC} = Max, V_{in} = 5.25 V	
I_{CEX}	Output Leakage Current		100	µAdc	V_{CC} = Max, V_{out} = 4.5 V	
V_{CD}	Input Diode Clamp Voltage		-1.5	Vdc	V_{CC} = Max, I_{in} = -10 mA	
I_{CC}	Power Supply Current		130	mAdc	T_A = Max	V_{CC} = Max, All Inputs Grounded
			155	mAdc	T_A = 0°C	
			170	mAdc	T_A = Min	

AC OPERATING CONDITIONS AND CHARACTERISTICS

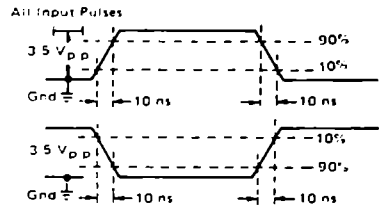
(Full operating voltage and temperature unless otherwise noted)

AC TEST LOAD AND WAVEFORM

Loading Condition



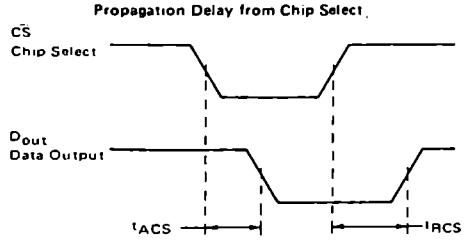
Input Pulses



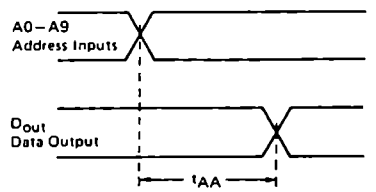
Symbol	Characteristic (Notes 2, 3)	MCM93415DC,PC Min	MCM93415DC,PC Max	MCM93415DM,FM Min	MCM93415DM,FM Max	Unit	Conditions
READ MODE	DELAY TIMES					ns	
t_{ACS}	Chip Select Time		35		45		See Test Circuit
t_{RCS}	Chip Select Recovery Time		35		50		and Waveforms
t_{AA}	Address Access Time		45		60		
WRITE MODE	DELAY TIMES					ns	
t_{WS}	Write Disable Time		35		45		See Test Circuit
t_{WR}	Write Recovery Time		40		50		and Waveforms
	INPUT TIMING REQUIREMENTS					ns	
t_W	Write Pulse Width (to guarantee write)	30		40			See Test Circuit
t_{WSD}	Data Setup Time Prior to Write	5		5			and Waveforms
t_{WHD}	Data Hold Time After Write	5		5			
t_{WSA}	Address Setup Time (at t_W Min)	10		15			
t_{WHA}	Address Hold Time	10		10			
t_{WSCS}	Chip Select Setup Time	5		5			
t_{WHCS}	Chip Select Hold Time	5		5			

READ OPERATION TIMING DIAGRAM

Propagation Delay from Chip Select

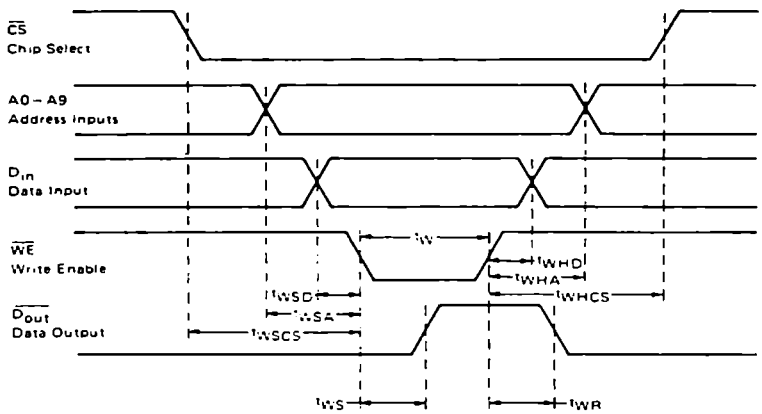


Propagation Delay from Address Inputs



(All Time Measurements Referenced to 1.5 V)

WRITE CYCLE TIMING



(All Time Measurements Referenced to 1.5 V)

NOTE 2. DC and AC specifications limits guaranteed with 500 linear feet per minute blown air. Contact your Motorola Sales Representative if extended temperature or modified operating conditions are desired.

Package	θ_{JA} (Junction to Ambient)		θ_{JC} (Junction to Case)
	Blown	Still	
D Suffix	50°C/W	85°C/W	15°C/W
F Suffix	55°C/W	90°C/W	15°C/W
P Suffix	65°C/W	100°C/W	25°C/W

NOTE 3. The AC limits are guaranteed to be the worst case bit in the memory.

MOTOROLA

MCM93425

1024-BIT RANDOM ACCESS MEMORY

The MCM93425 is a 1024-bit Read/Write RAM, organized 1024 words by 1 bit.

The MCM93425 is designed for high performance main memory and control storage applications and has a typical address time of 35 ns.

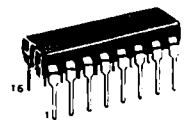
The MCM93425 has full decoding on-chip, separate data input and data output lines, and an active low-chip select and write enable. The device is fully compatible with standard DTL and TTL logic families. A three-state output is provided to drive bus-organized systems and/or highly capacitive loads.

- Three-State Output
- TTL Inputs and Output
- Non-Inverting Data Output
- High Speed –
  - Access Time – 35 ns Typical
  - Chip Select – 15 ns Typical
- Power Dissipation – 0.5 mW/Bit Typical
- Power Dissipation Decreases With Increasing Temperature

TTL
1024 X 1 BIT
RANDOM ACCESS MEMORY

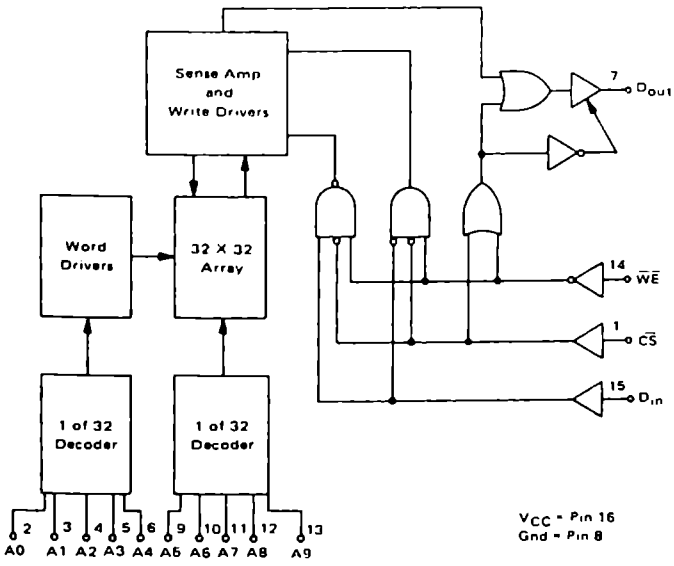
F SUFFIX
CERAMIC PACKAGE
CASE 650

D SUFFIX
CERAMIC PACKAGE
CASE 620



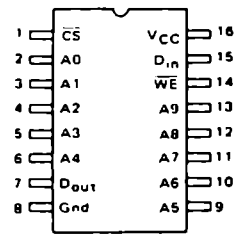
P SUFFIX
PLASTIC PACKAGE
CASE 648

BLOCK DIAGRAM



NOTE: Logic driving sense amp/write drivers depicts negative only write used on C4m

PIN ASSIGNMENT



Pin Description

$\overline{CS}$	Chip Select
A0 - A9	Address Inputs
$\overline{WE}$	Write Enable
D_{in}	Data Input
D_{out}	Data Output

FUNCTIONAL DESCRIPTION

The MCM93425 is a fully decoded 1024-bit Random Access Memory organized 1024 words by one bit. Word selection is achieved by means of a 10-bit address, A0–A9.

The Chip Select ($\overline{CS}$) input provides for memory array expansion. For large memories, the fast chip select time permits the decoding of chip select from the address without increasing address access time.

The read and write operations are controlled by the state of the active low Write Enable ($\overline{WE}$, Pin 14). With $\overline{WE}$ and $\overline{CS}$ held low, the data at D_{in} is written into the addressed location. To read, $\overline{WE}$ is held high and $\overline{CS}$ held low. Data in the specified location is presented at D_{out} and is non-inverted.

The three-state output provides drive capability for higher speeds with capacitive load systems. The third state (high impedance) allows bus organized systems where multiple outputs are connected to a common bus.

During writing, the output is held in the high-impedance state.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Storage Temperature	
Ceramic Package (D and F Suffix)	−55°C to +165°C
Plastic Package (P Suffix)	−55°C to +125°C
Operating Junction Temperature, T_J	
Ceramic Package (D and F Suffix)	+165°C
Plastic Package (P Suffix)	+125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
Input Voltage (dc)	−0.5 V to +5.5 V
Voltage Applied to Outputs (Output High)	−0.5 V to +5.5 V
Output Current (dc) (Output Low)	+20 mA
Input Current (dc)	−12 mA to +5.0 mA

NOTE 1: Device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.

TRUTH TABLE

Inputs			Output	
$\overline{CS}$	$\overline{WE}$	D_{in}	D_{out}	Mode
H	X	X	High Z	Not Selected
L	L	L	High Z	Write "0"
L	L	H	High Z	Write "1"
L	H	X	D_{out}	Read

H = High Voltage Level
L = Low Voltage Level
X = Don't Care (High or Low)

GUARANTEED OPERATING RANGES (Notes 2 and 3)

Part Number	Supply Voltage (V_{CC})			Ambient Temperature (T_A)
	Min	Nom	Max	
MCM93425DC, PC	4.75 V	5.0 V	5.25 V	0°C to +75°C
MCM93425FM, DM	4.50 V	5.0 V	5.50 V	−55°C to +125°C

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted)

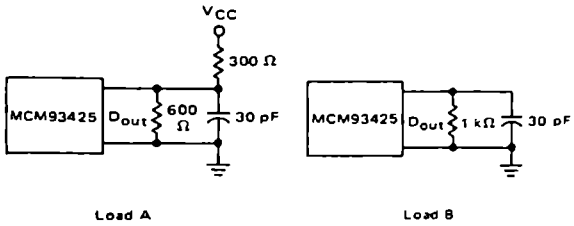
Symbol	Characteristic		Limits Min	Limits Max	Units	Conditions	
V_{OL}	Output Low Voltage			0.45	Vdc	V_{CC} Min, I_{OL} = 16 mA	
V_{IH}	Input High Voltage		2.1		Vdc	Guaranteed Input High Voltage for all Inputs	
V_{IL}	Input Low Voltage			0.8	Vdc	Guaranteed Input Low Voltage for all Inputs	
I_{IL}	Input Low Current			−400	μAdc	V_{CC} = Max, V_{in} = 0.4 V	
I_{IH}	Input High Current			40	μAdc	V_{CC} Max, V_{in} = 4.5 V	
				1.0	mAdc	V_{CC} Max, V_{in} = 5.25 V	
I_{off}	Output Current (High Z)			50	μAdc	V_{CC} Max, V_{out} = 2.4 V	
				−50		V_{CC} Max, V_{out} = 0.5 V	
I_{OS}	Output Current Short Circuit to Ground			−100	mAdc	V_{CC} Max	
V_{OH}	Output High Voltage	MCM93425DC, PC	2.4		Vdc	I_{OH} = −10.3 mA, V_{CC} = 5.0 V ±5%	
		MCM93425FM, DM	2.4		Vdc	I_{OH} = −5.2 mA	
V_{CD}	Input Diode Clamp Voltage			−1.5	Vdc	V_{CC} Max, I_{in} = −10 mA	
I_{CC}	Power Supply Current			130	mAdc	T_A = Max	V_{CC} Max, All Inputs Grounded
				155	mAdc	T_A = 0°C	
				170	mAdc	T_A = Min	

AC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature unless otherwise noted)

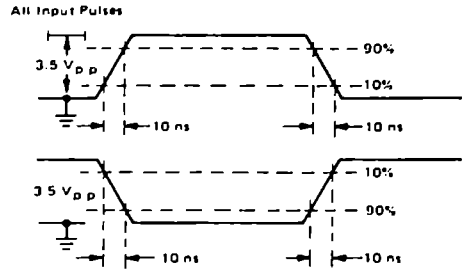
AC TEST LOAD AND WAVEFORMS

Loading Conditions



Load A Load B

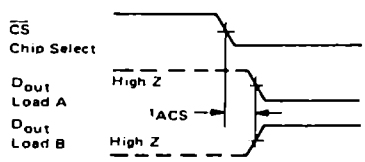
Input Pulses



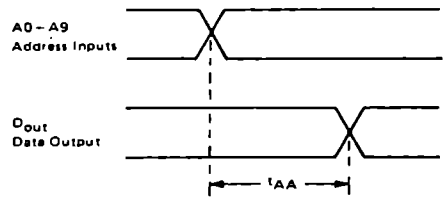
Symbol	Characteristic (Notes 2, 4)	MCM93425DC, PC Min	MCM93425DC, PC Max	MCM93425DM, FM Min	MCM93425DM, FM Max	Units	Conditions
READ MODE	DELAY TIMES					ns	
t_{ACS}	Chip Select Time		35		45		See Test Circuit
t_{ZRCS}	Chip Select to High Z		35		50		and Waveforms
t_{AA}	Address Access Time		45		60		
WRITE MODE	DELAY TIMES					ns	
t_{ZWS}	Write Disable to High Z		35		45		See Test Circuit
t_{WR}	Write Recovery Time		40		50		and Waveforms
	INPUT TIMING REQUIREMENTS					ns	
t_W	Write Pulse Width (to guarantee write)	30		40			See Test Circuit
t_{WSD}	Data Setup Time Prior to Write	5		5			and Waveforms
t_{WHD}	Data Hold Time After Write	5		5			
t_{WSA}	Address Setup Time (at t_W = Min)	10		15			
t_{WHA}	Address Hold Time	10		10			
t_{WSCS}	Chip Select Setup Time	5		5			
t_{WHCS}	Chip Select Hold Time	5		5			

READ OPERATION TIMING DIAGRAM

Propagation Delay from Chip Select

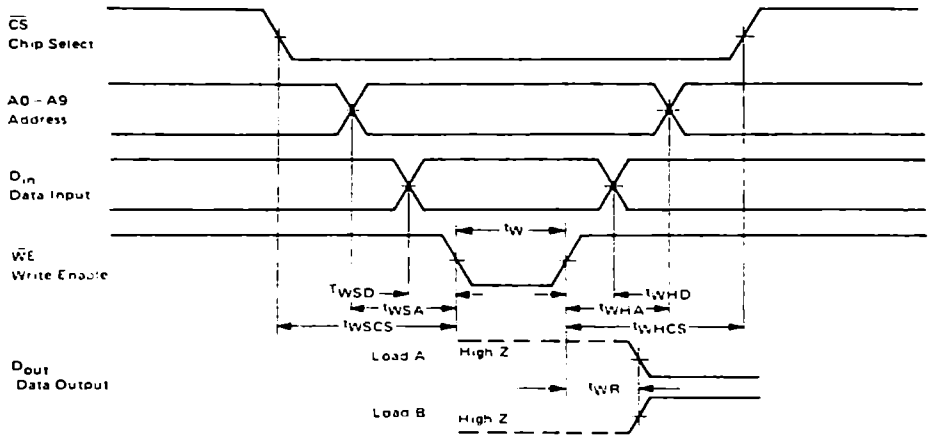


Propagation Delay from Address Inut



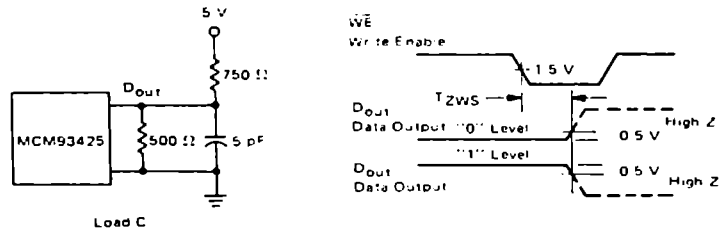
(All time measurements referenced to 1.5 V)

WRITE CYCLE TIMING

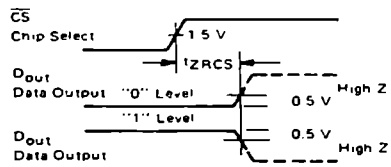


(All above measurements reference to 1.5 V)

WRITE ENABLE TO HIGH Z DELAY



Propagation Delay from Chip Select to High Z



(All t_{ZXX} parameters are measured at a delta of 0.5 V from the logic level and using Load C)

NOTE 2: DC and AC specifications limits guaranteed with 500 linear feet per minute blown air. Contact your Motorola Sales Representative if extended temperature or modified operating conditions are desired.

Package	θ_{JA} (Junction to Ambient)		θ_{JC} (Junction to Case)
	Blown	Still	
D Suffix	50°C/W	85°C/W	15°C/W
F Suffix	55°C/W	90°C/W	15°C/W
P Suffix	65°C/W	100°C/W	25°C/W

NOTE 3: Output short circuit conditions must not exceed 1 second duration.

NOTE 4: The maximum address access time is guaranteed to be the worst case bit in the memory.

MOTOROLA

MCM7680
MCM7681

8192-BIT PROGRAMMABLE READ ONLY MEMORY

The MCM7680/81 together with the MCM7620/21, MCM7640/43 comprise a complete, compatible family having common dc electrical characteristics and identical programming requirements. They are fully decoded, high-speed, field-programmable ROMs and are available in commonly used organizations, with both open-collector and three-state outputs. All bits are manufactured storing a logical "1" (outputs high), and can be selectively programmed for logical "0" (outputs low).

The field-programmable PROM can be custom-programmed to any pattern using a simple programming procedure. Schottky bipolar circuitry provides fast access time, and features temperature and voltage compensation to minimize access time variations.

Pinouts are compatible to industry-standard PROMs and ROMs. In addition, the MCM7680 and 81 are pin compatible replacement for the 512 × 8 with pin 2 connected as A9 on the 1024 × 8.

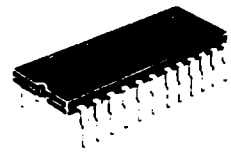
In addition to the conventional storage array, extra test rows and columns are included to assure high programmability, and guarantee parametric and ac performance. Fuses in these test rows and columns are blown prior to shipment.

- Common dc Electrical Characteristics and Programming Procedure
- Simple, High-Speed Programming Procedure (0.1 second per 1024 Bits, Typical)
- Expandable – Open-Collector or Three-State Outputs and Chip Enable Inputs
- Inputs and Outputs TTL-Compatible
  Low Input Current – 250 μA Logic "0", 40 μA Logic "1"
  Full Output Drive – 16 mA Sink, 2.0 mA Source
- Fast Access Time – Guaranteed for Worst-Case N^2 Sequencing, Over Commercial and Military Temperature Ranges
- Pin-Compatible with Industry-Standard PROMs and ROMs

MTTL

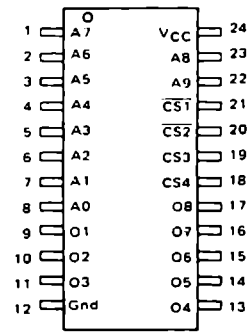
8192-BIT PROGRAMMABLE READ ONLY MEMORIES

MCM7680 – 1024 × 8 – Open-Collector
MCM7681 – 1024 × 8 – Three-State



CERAMIC PACKAGE
CASE 623

PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Supply Voltage (operating)	V_{CC}	+7.0	Vdc
Input Voltage	V_{in}	+5.5	Vdc
Output Voltage (operating)	V_{OH}	+7.0	Vdc
Supply Current	I_{CC}	650	mAdc
Input Current	I_{in}	-20	mAdc
Output Sink Current	I_o	100	mAdc
Operating Temperature Range MCM76xxDM MCM76xxDC	T_A	 -55 to +125 0 to +70	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C
Maximum Junction Temperature	T_J	+175	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability. (While programming, follow the programming specifications.)

DC OPERATING CONDITIONS AND CHARACTERISTICS

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Symbol	Min	Nom	Max	Unit
Supply Voltage	V_{CC}				Vdc
MCM76xxDM		4.50	5.0	5.50	
MCM76xxDC		4.75	5.0	5.25	
Input High Voltage	V_{IH}	2.0	–	–	Vdc
Input Low Voltage	V_{IL}	–	–	0.8	Vdc

DC CHARACTERISTICS

			Open-Collector Output			Three-State Output			
Symbol	Parameter	Test Conditions	Min	Typ	Max	Min	Typ	Max	Unit
I_{RA}, I_{RE}	Address/Enable "1"	V_{IH} = V_{CC} Max	–	–	40	–	–	40	µAdc
I_{FA}, I_{FE}	Input Current "0"	V_{IL} = 0.45 V	–	-0.1	-0.25	–	-0.1	-0.25	mAdc
V_{OH}	Output Voltage "1"	I_{OH} = -2.0 mA, V_{CC} = V_{CC} Min	N/A	–	–	2.4	3.4	–	Vdc
V_{OL}	"0"	I_{OL} = +16 mA, V_{CC} = V_{CC} Min	–	0.35	0.45	–	0.35	0.45	Vdc
I_{OHE}	Output Disabled "1"	V_{OH}, V_{CC} = V_{CC} Max	–	–	100	–	–	100	µAdc
I_{OLE}	Current "0"	V_{OL} = +0.3 V, V_{CC} = V_{CC} Max	–	–	N/A	–	–	-100	µAdc
I_{OH}	Output Leakage "1"	V_{OH}, V_{CC} = V_{CC} Max	–	–	100		–	N/A	µAdc
V_{CL}	Input Clamp Voltage	I_{in} = -10 mA	–	–	-1.5	–	–	-1.5	Vdc
I_{OS}	Output Short Circuit Current	V_{CC} = V_{CC} Max, V_{out} = 0.0 V One Output Only for 1 s Max	N/A	–	N/A	15	–	70	mAdc
I_{CC}	Power Supply Current	V_{CC} = V_{CC} Max							
	MCM7680/MCM7681DC	All Inputs Grounded	–	110	150	–	110	150	mAdc
	MCM7680/MCM7681DM		–	110	170	–	110	170	mAdc

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, periodically sampled rather than 100% tested.)

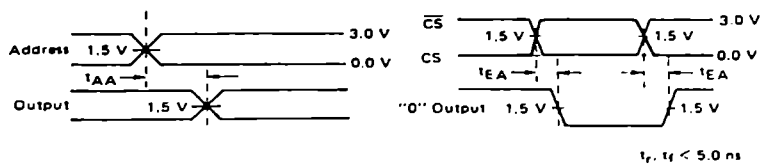
Characteristic	Symbol	Typ	Unit
Input Capacitance	C_{in}	8.0	pF
Output Capacitance	C_{out}	8.0	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

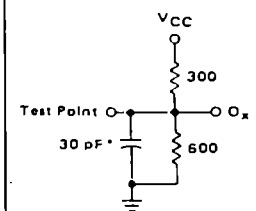
(Full operating voltage and temperature unless otherwise noted)

		0 to +70°C		-55 to +125°C		
Characteristic	Symbol	Typ	Max	Typ	Max	Unit
Address to Output Access Time	t_{AA}	45	70	45	85	ns
Chip Enable Access Time	t_{EA}					ns
MCM7680/81		30	40	30	50	

TIMING DIAGRAM



AC TEST LOAD



PROGRAMMING

The PROMs are manufactured with all bits/outputs Logical "1" (Output High). Any desired bit/output can be programmed to a Logical "0" (Output Low) by following the simple procedure shown below. One may build his own programmer to satisfy the sepcifications described in Table 1, or buy any of the commercially available programmers which meet these specifications. These PROMs can be programmed automatically or by the manual procedure shown below.

PROGRAMMING PROCEDURE

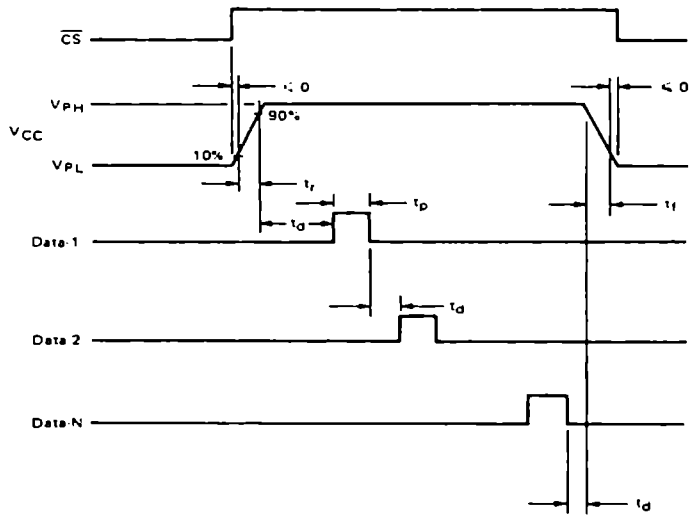
1. Address the PROM with the binary address of the selected word to be programmed. Address inputs are TTL-compatible. An open circuit should not be used to address the PROM.
2. Disable the chip by applying inputs highs (V_{IH}) to the $\overline{CS}$ inputs. CS inputs must remain at V_{IH} for program and verify. The chip select is TTL-compatible. An open circuit should not be used to disable the chip.
3. Disable the programming circuitry by applying an Output Voltage Disable of less than V_{OPD} to the output of the PROM. The output may be left open to achieve the disable.
4. Raise V_{CC} to V_{PH} with rise time equal to t_r.
5. After a delay equal to or greater than t_d, apply a pulse with amplitude of V_{OPE} and duration of t_p to the output selected for programming. Note that the PROM is supplied with fuses intact generating an output high. Programming a fuse will cause the output to go low in the verify mode.
6. Other bits in the same word may be programmed while the V_{CC} input is raised to V_{PH} by applying output enable pulses to each output which is to be programmed. The output enable pulses must be separated by a minimum interval of t_d.
7. Lower V_{CC} to 4.5 Volts following a delay of t_d from the last programming enable pulse applied to an output.
8. Enable the PROM for verification by applying a logic "0" (V_{IL}) to the $\overline{CS}$ inputs.
9. If any bit does not verify as programmed, repeat Steps 2 through 8 until the bit has received a total of 1.0 ms of programming time. Bits which do not program within 1.0 ms may be considered programming rejects. Multiple pulses of durations shorter than 1.0 ms may be used to enhance programming speed.
10. Repeat Steps 1 through 9 for all other bits to be programmed in the PROM.
11. Programming rejects returned to the factory must be accompanied by data giving address with desired and actual output data of a location in which a programming failure has occurred.

TABLE 1
PROGRAMMING SPECIFICATIONS

Symbol	Parameter	Min	Typ	Max	Unit
V_{IH}	Address Input	2.4	5.0	5.0	V
V_{IL}	Voltage(1)	0.0	0.4	0.8	V
V_{PH}	Programming/Verify	11.75	12.0	12.25	V
V_{PL}	Voltage to V_{CC}	4.5	4.5	5.5	V
I_{CCP}	Programming Voltage Current Limit Programming (V_{CC})	600	600	650	mA
t_r	Voltage Rise and	1	1	10	µs
t_f	Fall Time	1	1	10	µs
t_d	Programming Delay	10	10	100	µs
t_p	Programming Pulse Width	100	–	1000	µs
DC	Programming Duty Cycle	–	50	90	%
	Output Voltage				
V_{OPE}	Enable	10.0	10.5	11.0	V
V_{OPD}	Disable(2)	4.5	5.0	5.5	V
I_{OPE}	Output Voltage Enable Current	2	4	10	mA
T_C	Case Temperature	–	25	75	°C

(1) Address and chip select should not be left open for V_{IH}.
(2) Disable condition will be met with output open circuit.

FIGURE 1 – TYPICAL PROGRAMMING WAVEFORMS



MOTOROLA

MCM7684
MCM7685

Advance Information

8192-BIT PROGRAMMABLE READ ONLY MEMORY

The MCM7684/85 together with the MCM7620/21/40/41/42/43/80/81 comprise a complete, compatible family having common dc electrical characteristics and identical programming requirements. They are fully decoded, high-speed, field-programmable ROMs and are available in commonly used organizations, with both open-collector and three-state outputs. All bits are manufactured storing a logical "1" (outputs high), and can be selectively programmed for logical "0" (outputs low).

The field-programmable PROM can be custom-programmed to any pattern using a simple programming procedure. Schottky bipolar circuitry provides fast access time, and features temperature and voltage compensation to minimize access time variations.

Pinouts are compatible to industry-standard PROMs and ROMs. In addition, the MCM7684 and 85 are pin compatible replacement for the 1024 X 4 with pin 8 connected as A10 on the 2048 X 4.

In addition to the conventional storage array, extra test rows and columns are included to assure high programmability, and guarantee parametric and ac performance. Fuses in these test rows and columns are blown prior to shipment.

- Common dc Electrical Characteristics and Programming Procedure
- Simple, High-Speed Programming Procedure (0.1 second per 1024 Bits, Typical)
- Expandable – Open-Collector or Three-State Outputs and Chip Enable Input
- Inputs and Outputs TTL-Compatible
  Low Input Current – 250 μA Logic "0", 40 μA Logic "1"
  Full Output Drive – 16 mA Sink, 2.0 mA Source
- Fast Access Time – Guaranteed for Worst-Case N^2 Sequencing, Over Commercial and Military Temperature Ranges
- Pin-Compatible with Industry-Standard PROMs and ROMs

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Supply Voltage (operating)	V_{CC}	+7.0	Vdc
Input Voltage	V_{in}	+5.5	Vdc
Output Voltage (operating)	V_{OH}	+7.0	Vdc
Supply Current	I_{CC}	650	mAdc
Input Current	I_{in}	-20	mAdc
Output Sink Current	I_o	100	mAdc
Operating Temperature Range MCM76xxDM MCM76xxDC	T_A	 -55 to +125 0 to +70	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C
Maximum Junction Temperature	T_J	+175	°C

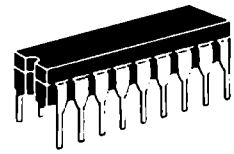
NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability. (While programming, follow the programming specifications.)

This is advance information and specifications are subject to change without notice.

MTTL

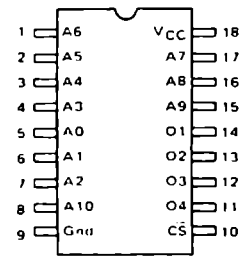
8192-BIT PROGRAMMABLE READ ONLY MEMORIES

MCM7684 – 2048 X 4 – Open-Collector
MCM7685 – 2048 X 4 – Three-State



D SUFFIX
CERAMIC PACKAGE
CASE 726

PIN ASSIGNMENT



DC OPERATING CONDITIONS AND CHARACTERISTICS

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Symbol	Min	Nom	Max	Unit
Supply Voltage	V_{CC}				Vdc
MCM76xxDM		4.50	5.0	5.50	
MCM76xxDC		4.75	5.0	5.25	
Input High Voltage	V_{IH}	2.0	–	–	Vdc
Input Low Voltage	V_{IL}	–	–	0.8	Vdc

DC CHARACTERISTICS

(Over Recommended Operating Temperature Range)

				Open-Collector Output			Three-State Output			
Symbol	Parameter		Test Conditions	Min	Typ	Max	Min	Typ	Max	Unit
I_{RA}, I_{RE}	Address/Enable	"1"	V_{IH} = V_{CC} Max	–	–	40	–	–	40	µAdc
I_{EA}, I_{FE}	Input Current	"0"	V_{IL} = 0.45 V	–	-0.1	-0.25	–	-0.1	-0.25	mAdc
V_{OH}	Output Voltage	"1"	I_{OH} = -2.0 mA, V_{CC} Min	N/A	–	–	2.4	3.4	–	Vdc
V_{OL}		"0"	I_{OL} = +16 mA, V_{CC} Min	–	0.35	0.45	–	0.35	0.45	Vdc
I_{OHZ}	Output Disabled	"1"	V_{OH}, V_{CC} Max	–	–	100	–	–	100	µAdc
I_{OLZ}	Current	"0"	V_{OL} = +0.3 V, V_{CC} Max	–	–	N/A	–	–	-100	µAdc
I_{OH}	Output Leakage	"1"	V_{OH}, V_{CC} Max	–	–	100	–	–	N/A	µAdc
V_{IC}	Input Clamp Voltage		I_{in} = -10 mA	–	–	-1.5	–	–	-1.5	Vdc
I_{OS}	Output Short Circuit Current		V_{CC} Max, V_{out} = 0.0 V One Output Only for 1 s Max	N/A	–	N/A	15	–	70	mAdc
I_{CC}	Power Supply Current		V_{CC} Max							
	MCM7684/MCM7685 DC		All Inputs Grounded	–	80	120	–	80	120	mAdc
	MCM7684/MCM7685 DM			–	80	140	–	80	140	mAdc

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, periodically sampled rather than 100% tested.)

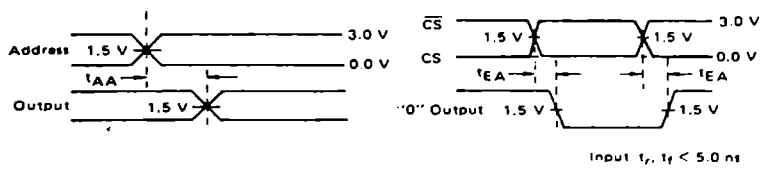
Characteristic	Symbol	Typ	Unit
Input Capacitance	C_{in}	8.0	pF
Output Capacitance	C_{out}	8.0	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

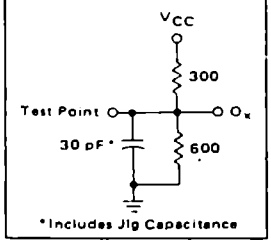
(Full operating voltage and temperature unless otherwise noted)

		0 to +70°C		-55 to +125°C		
Characteristic	Symbol	Typ	Max	Typ	Max	Unit
Address to Output Access Time	t_{AA}	45	70	45	85	ns
Chip Enable Access Time	t_{EA}	15	25	15	30	ns

TIMING DIAGRAM



AC TEST LOAD



PROGRAMMING

The PROMs are manufactured with all bits/outputs Logical "1" (Output High). Any desired bit/output can be programmed to a Logical "0" (Output Low) by following the simple procedure shown below. One may build his own programmer to satisfy the sepcifications described in Table 1, or buy any of the commercially available programmers which meet these specifications. These PROMs can be programmed automatically or by the manual procedure shown below.

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1. Address the PROM with the binary address of the selected word to be programmed. Address inputs are TTL-compatible. An open circuit should not be used to address the PROM.
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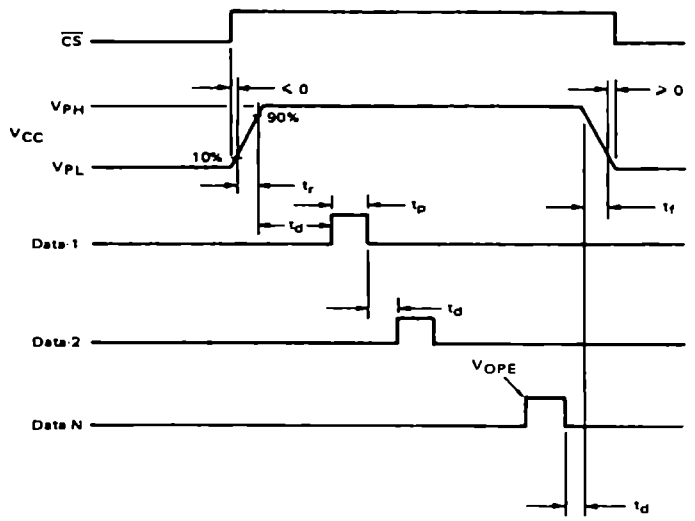
3. Disable the programming circuitry by applying an Output Voltage Disable of less than V_{OPD} to the output of the PROM. The output may be left open to achieve the disable.
4. Raise V_{CC} to V_{PH} with rise time equal to t_r.
5. After a delay equal to or greater than t_d, apply a pulse with amplitude of V_{OPE} and duration of t_p to the output selected for programming. Note that the PROM is supplied with fuses intact generating an output high. Programming a fuse will cause the output to go low in the verify mode.
6. Other bits in the same word may be programmed while the V_{CC} input is raised to V_{PH} by applying output enable pulses to each output which is to be programmed. The output enable pulses must be separated by a minimum interval of t_d.
7. Lower V_{CC} to 4.5 Volts following a delay of t_d from the last programming enable pulse applied to an output.
8. Enable the PROM for verification by applying a logic "0" (V_{IL}) to the $\overline{CS}$ inputs.
9. If any bit does not verify as programmed, repeat Steps 2 through 8 until the bit has received a total of 1.0 ms of programming time. Bits which do not program within 1.0 ms may be considered programming rejects. Multiple pulses of durations shorter than 1.0 ms may be used to enhance programming speed.
10. Repeat Steps 1 through 9 for all other bits to be programmed in the PROM.
11. Programming rejects returned to the factory must be accompanied by data giving address with desired and actual output data of a location in which a programming failure has occurred.

TABLE 1
PROGRAMMING SPECIFICATIONS

Symbol	Parameter	Min	Typ	Max	Unit
V_{IH}	Address Input	2.4	5.0	5.0	V
V_{IL}	Voltage(1)	0.0	0.4	0.8	V
V_{PH}	Programming/Verify	11.75	12.0	12.25	V
V_{PL}	Voltage to V_{CC}	4.5	4.5	5.5	V
I_{CCP}	Programming Voltage Current Limit Programming (V_{CC})	600	600	650	mA
t_r	Voltage Rise and	1	1	10	µs
t_f	Fall Time	1	1	10	µs
t_d	Programming Delay	10	10	100	µs
t_p	Programming Pulse Width	100	–	1000	µs
DC	Programming Duty Cycle	–	50	90	%
	Output Voltage				
V_{OPE}	Enable	10.0	10.5	11.0	V
V_{OPD}	Disable(2)	4.5	5.0	5.5	V
I_{OPE}	Output Voltage Enable Current	2	4	10	mA
T_C	Case Temperature	–	25	75	°C

(1) Address and chip select should not be left open for V_{IH}.
(2) Disable condition will be met with output open circuit.

FIGURE 1 – TYPICAL PROGRAMMING WAVEFORMS



MECL MEMORIES
GENERAL INFORMATION

Complete information is available in the MECL Data Book. Contact your sales representative or authorized distributor for information.

TABLE 1 – LIMITS BEYOND WHICH DEVICE LIFE MAY BE IMPAIRED

Characteristic	Symbol	Rating	Unit
Supply Voltage	V_{EE}	-8.0 to 0	V
Input Voltage (V_{CC} = 0)	V_{in}	0 to V_{EE}	V
Output Source Current – Continuous Surge	I_{out}	50 100	mA
Junction Temperature – Ceramic Package① Plastic Package	T_J	165 150	°C
Storage Temperature	T_{stg}	-55 to +150	°C

① Maximum T_J may be exceeded ($\leq 250^{\circ}C$) for short periods of time ($\leq$ 240 hours) without significant reduction in device life.

TABLE 2 – LIMITS BEYOND WHICH PERFORMANCE MAY BE DEGRADED

Characteristic	Symbol	Rating	Unit
Supply Voltage (V_{CC} = 0)②	V_{EE}	-4.94 to -5.46	V
Output Drive – MCM10100 Series MCM10500 Series	–	50 Ω to -2.0 V 100 Ω to -2.0 V	Ω
Operating Temperature Range③ MCM10100 Series MCM10500 Series	T_A	 0 to 75 -55 to +125	°C

② Functionality only. Data sheet limits are specified for -5.19 to -5.21 V.
③ With airflow ≥ 500 lfpm.

TABLE 3 – DC TEST PARAMETERS

Each MECL 10,000 series device has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 linear feet per minute is maintained. V_{EE} = −5.2 V ± 0.010 V.

Forcing Function	Parameter	−55°C	0°C	25°C		75°C	125°C
		MCM10500*	MCM10100**	MCM10100**	MCM10500*	MCM10100**	MCM10500*
V_{IHmax}	V_{OHmax}	−0.880	−0.840	−0.810	−0.780	−0.720	−0.630
	V_{OHmin}	−1.080	−1.000	−0.960	−0.930	−0.900	−0.825
	V_{OHAmin}	−1.100	−1.020	−0.980	−0.950	−0.920	−0.845
V_{IHAmin}		−1.255	−1.145	−1.105	−1.105	−1.045	−1.000
V_{ILAmin}		−1.510	−1.490	−1.475	−1.475	−1.450	−1.400
	V_{OLAmin}	−1.635	−1.645	−1.630	−1.600	−1.605	−1.525
	V_{OLAmax}	−1.655	−1.665	−1.650	−1.620	−1.625	−1.545
V_{ILmin}	V_{OLmin}	−1.920	−1.870	−1.850	−1.850	−1.830	−1.820
V_{ILmin}	I_{INLmin}	0.5	0.5	0.5	0.5	0.3	0.3

*Driving 100 Ω to −2.0 V.
**Driving 50 Ω to −2.0 V.

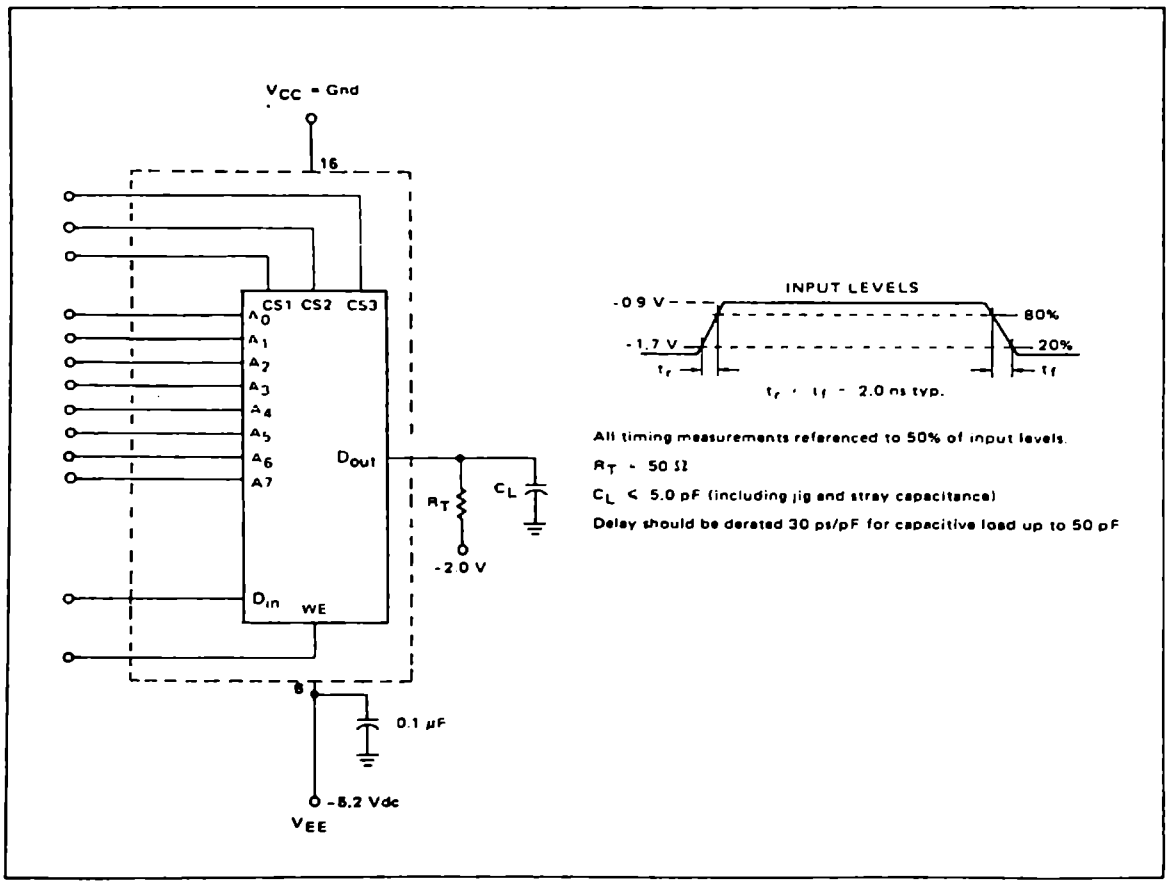


FIGURE 1 – SWITCHING TIME TEST CIRCUIT

FIGURE 2 -- CHIP SELECT ACCESS TIME WAVEFORM

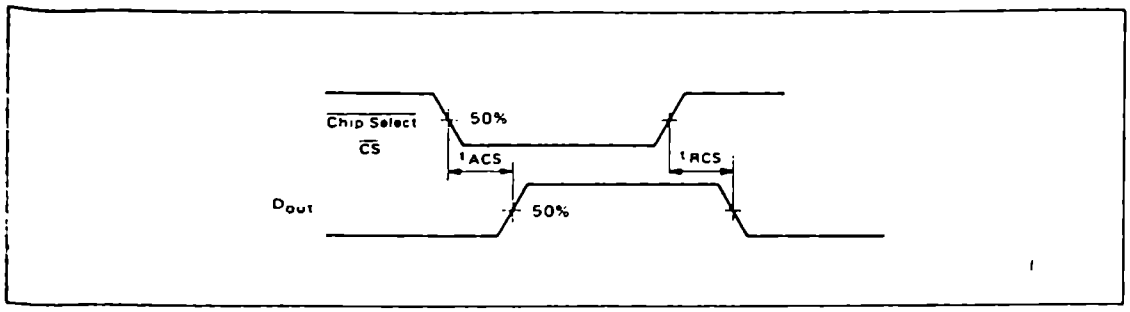


FIGURE 3 – ADDRESS ACCESS TIME WAVEFORM

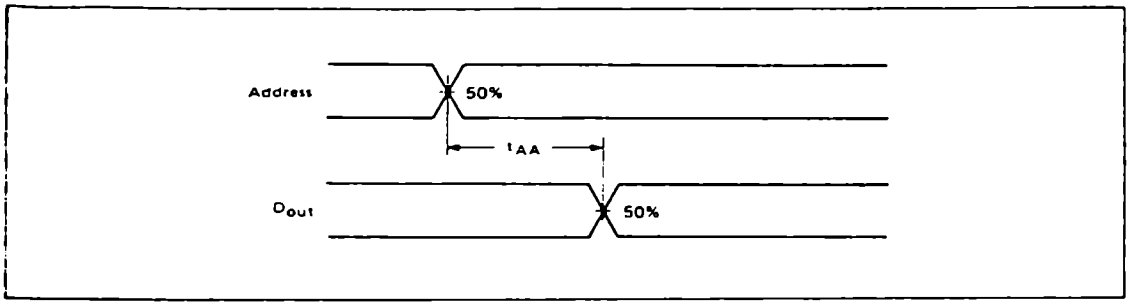
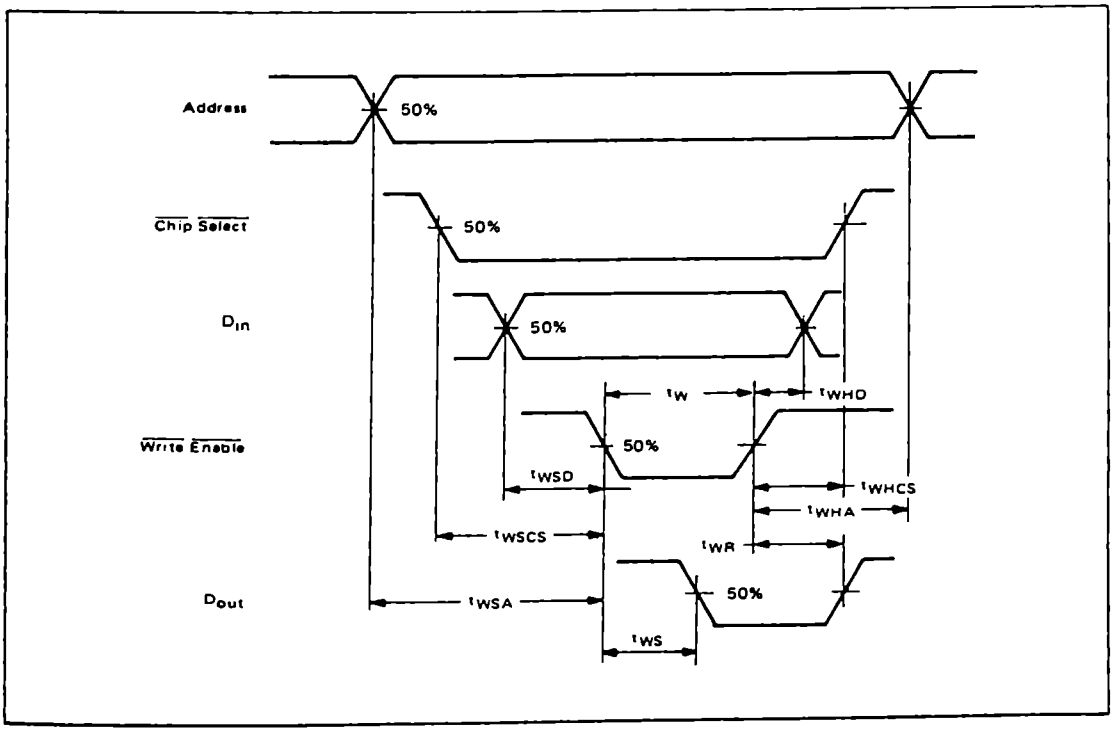


FIGURE 4 – SETUP AND HOLD WAVEFORMS (WRITE MODE)



8 x 2 MULTIPORT REGISTER FILE (RAM)

The MCM10143 is an 8 word by 2 bit multiport register file (RAM) capable of reading two locations and writing one location simultaneously. Two sets of eight latches are used for data storage in this LSI circuit.

WRITE

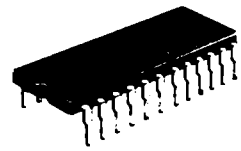
The word to be written is selected by addresses A_0–A_2. Each bit of the word has a separate write enable to allow more flexibility in system design. A write occurs on the positive transition of the clock. Data is enabled by having the write enables at a low level when the clock makes the transition. To inhibit a bit from being written, the bit enable must be at a high level when the clock goes low and not change until the clock goes high. Operation of the clock and the bit enables can be reversed. While the clock is low a positive transition of the bit enable will write that bit into the address selected by A_0–A_2.

READ

When the clock is high any two words may be read out simultaneously, as selected by addresses B_0–B_2 and C_0–C_2, including the word written during the preceding half clock cycle. When the clock goes low the addressed data is stored in the slaves. Level changes on the read address lines have no effect on the output until the clock again goes high. Read out is accomplished at any time by enabling output gates ($\overline{OB}_0$–$\overline{OB}_1$), ($\overline{OC}_0$–$\overline{OC}_1$).

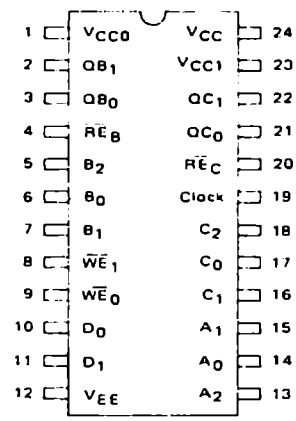
t_{pd}:
- Clock to Data out – 5 ns (typ) (Read Selected)
- Address to Data out – 10 ns (typ) (Clock High)
- $\overline{\text{Read Enable}}$ to Data out – 2.8 ns (typ) (Clock high, Addresses present)

P_D – 610 mW/pkg (typ no load)



L SUFFIX
CERAMIC PACKAGE
CASE 623

PIN ASSIGNMENT



TRUTH TABLE

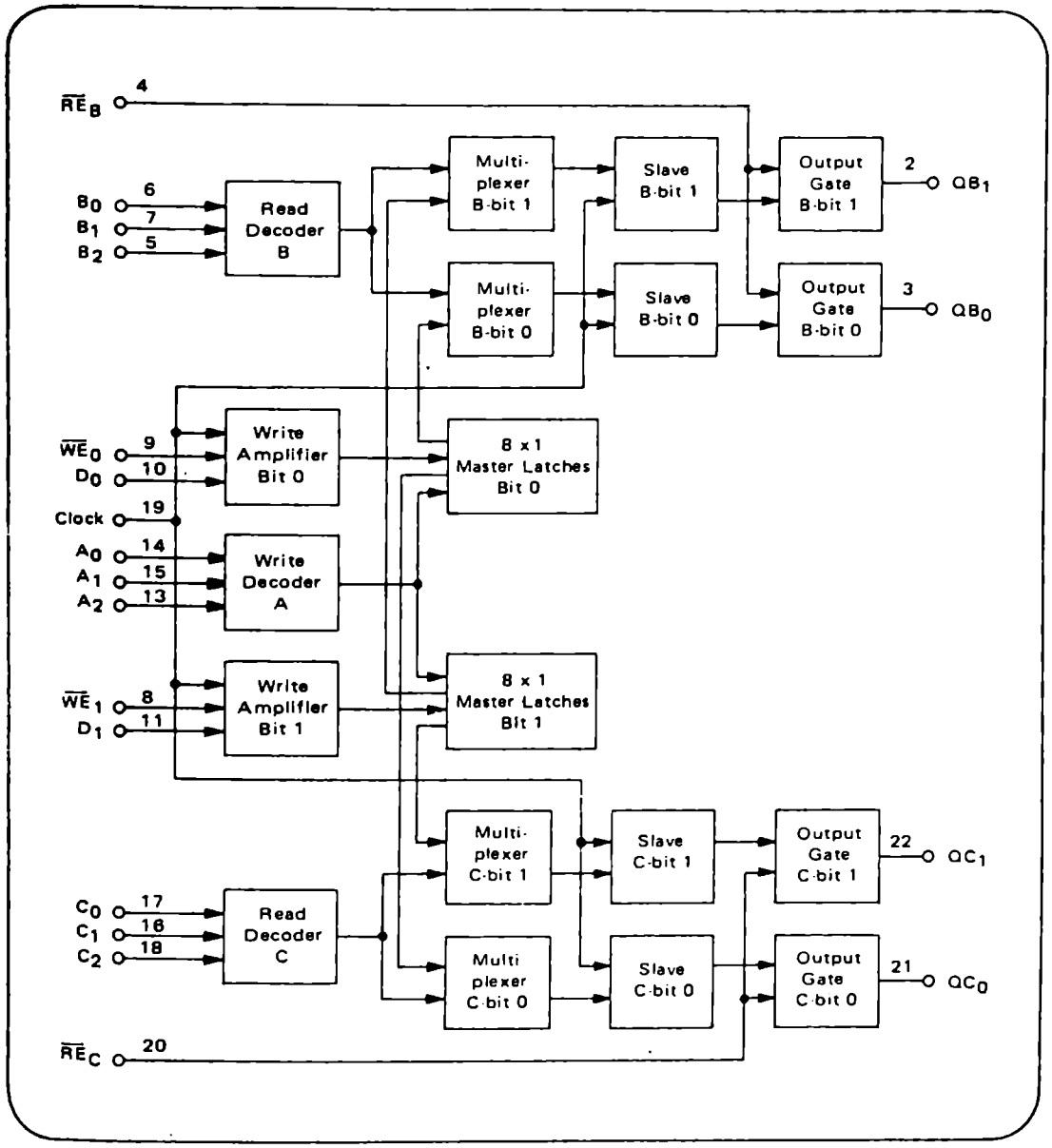
*MODE	INPUT							OUTPUT			
	**Clock	$\overline{WE}_0$	$\overline{WE}_1$	D_0	D_1	$\overline{RE}_B$	$\overline{RE}_C$	$\overline{OB}_0$	$\overline{OB}_1$	$\overline{OC}_0$	$\overline{OC}_1$
Write	L→H	L	L	H	H	H	H	L	L	L	L
Read	H	◇	◇	◇	◇	L	L	H	H	H	H
Read	H→L	◇	◇	◇	◇	L	L	H	H	H	H
Read	L→H→L	H	H	◇	◇	L	L	H	H	H	H
Write	L→H	L	L	L	H	H	H	L	L	L	L
Read	H	◇	◇	◇	◇	L	L	L	H	L	H

**Note Clock occurs sequentially through Truth Table

*Note A0 A2, B0 B2, and C0 C2 are all set to same address location throughout Table

◇ Don't Care

BLOCK DIAGRAM

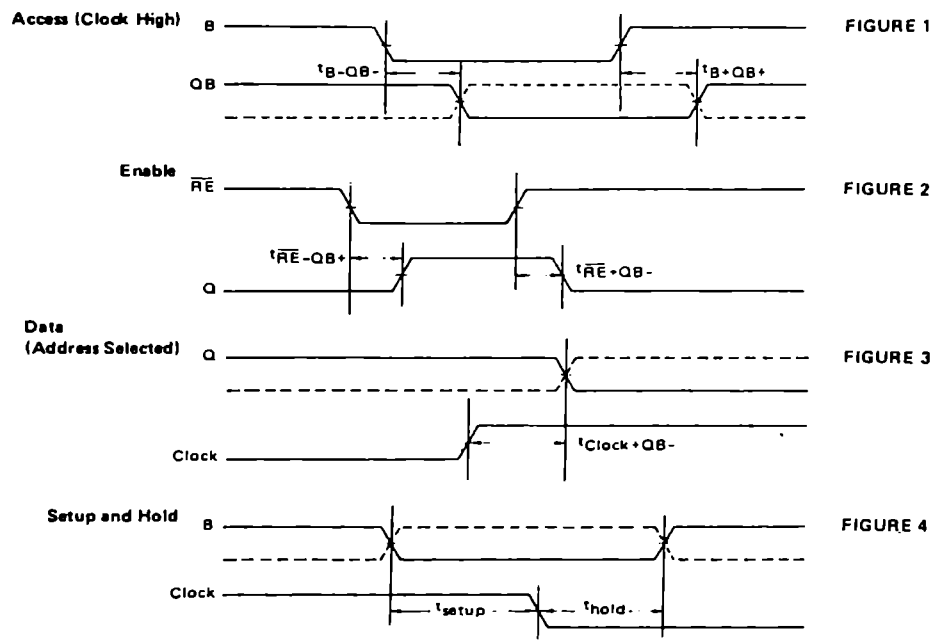


ELECTRICAL CHARACTERISTICS

Characteristics	Symbol	0°C		+25°C			+75°C		Unit
		Min	Max	Min	Typ	Max	Min	Max	
Power Supply Drain Current	I_E	–	150	–	118	150	–	150	mAdc
Input Current	I_{inH}								μAdc
Pins 10, 11, 19		–	245	–	–	245	–	245	
All other pins		–	200	–	–	200	–	200	
Switching Times ①									ns
Read Mode									
Address Input	$t_{B\pm QB\pm}$	4.0	15.3	4.5	10	14.5	4.5	15.5	
$\overline{\text{Read Enable}}$	$t_{\overline{RE}-QB+}$	1.1	5.3	1.2	3.5	5.0	1.2	5.5	
Data	$t_{Clock+QB-}$	1.7	7.3	2.0	5.0	7.0	2.0	7.6	
Setup									
Address	$t_{setup(B-Clock-)}$	–	–	8.5	5.5	–	–	–	
Hold									
Address	$t_{hold(Clock-B+)}$	–	–	-1.5	-4.5	–	–	–	
Write Mode									
Setup									
$\overline{\text{Write Enable}}$	$t_{setup(\overline{WE}-Clock+)}$	–	–	7.0	4.0	–	–	–	
	$t_{setup(\overline{WE}+Clock-)}$	–	–	1.0	-2.0	–	–	–	
Address	$t_{setup(A-Clock+)}$	–	–	8.0	5.0	–	–	–	
Data	$t_{setup(D-Clock+)}$	–	–	5.0	2.0	–	–	–	
Hold									
$\overline{\text{Write Enable}}$	$t_{hold(Clock+\overline{WE}+)}$	–	–	5.5	2.5	–	–	–	
	$t_{hold(Clock+\overline{WE}-)}$	–	–	1.0	-2.0	–	–	–	
Address	$t_{hold(Clock+A+)}$	–	–	1.0	-3.0	–	–	–	
Data	$t_{hold(Clock+D+)}$	–	–	1.0	-2.0	–	–	–	
Write Pulse Width	$PW_{\overline{WE}}$	–	–	8.0	5.0	–	–	–	
Rise Time, Fall Time (20% to 80%)	t_r, t_f	1.1	4.2	1.1	2.5	4.0	1.1	4.5	

①AC timing figures do not show all the necessary presetting conditions.

READ TIMING DIAGRAMS



WRITE TIMING DIAGRAM

Enable Setup

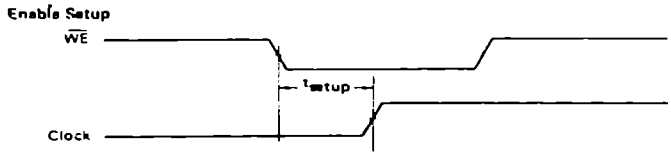


FIGURE 5

Enable Hold

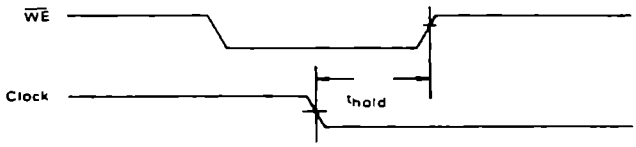


FIGURE 6

Disable

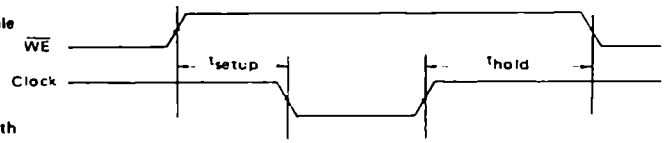


FIGURE 7

Pulse Width

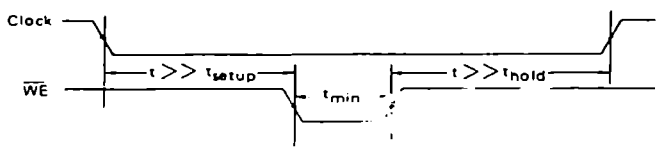


FIGURE 8

Address

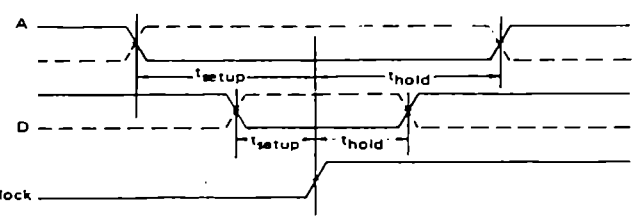
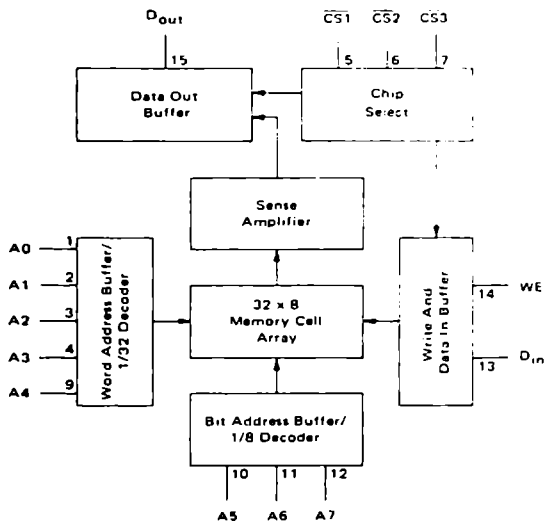


FIGURE 9

MCM10144/MCM10544

256 X 1-BIT RANDOM ACCESS MEMORY



The MCM10144/10544 is a 256 word X 1-bit RAM. Bit selection is achieved by means of an 8-bit address A0 through A7.

The active-low chip select allows memory expansion up to 2048 words. The fast chip select access time allows memory expansion without affecting system performance.

The operating mode of the RAM ($\overline{CS}$ inputs low) is controlled by the $\overline{WE}$ input. With $\overline{WE}$ low the chip is in the write mode—the output is low and the data present at D_{in} is stored at the selected address. With $\overline{WE}$ high the chip is in the read mode—the data state at the selected memory location is presented non-inverted at D_{out}.

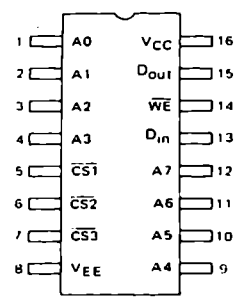
- Typical Address Access Time = 17 ns
- Typical Chip Select Access Time = 4.0 ns
- 50 kΩ Input Pulldown Resistors on Chip Select
- Power Dissipation (470 mW typ @ 25°C) Decreases with Increasing Temperature
- Pin-for-Pin Replacement for F10410

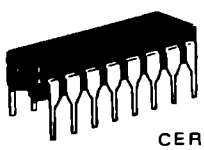
TRUTH TABLE

MODE	INPUT			OUTPUT
	$\overline{CS}$*	$\overline{WE}$	D_{in}	D_{out}
Write "0"	L	L	L	L
Write "1"	L	L	H	L
Read	L	H	Ø	Q
Disabled	H	Ø	Ø	L

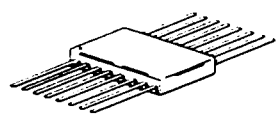
*$\overline{CS} = \overline{CS1} + \overline{CS2} + \overline{CS3}$ Ø = Don't Care

PIN ASSIGNMENT





L SUFFIX
CERAMIC PACKAGE
CASE 620



F SUFFIX
CERAMIC PACKAGE
CASE 650

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	−55°C		0°C		+25°C		+75°C		+125°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_{EE}	–	140	–	135	–	130	–	125	–	125	mAdc
Input Current High	I_{inH}	–	375	–	220	–	220	–	220	–	220	μAdc

-55°C and +125°C test values apply to MC105xx devices only.

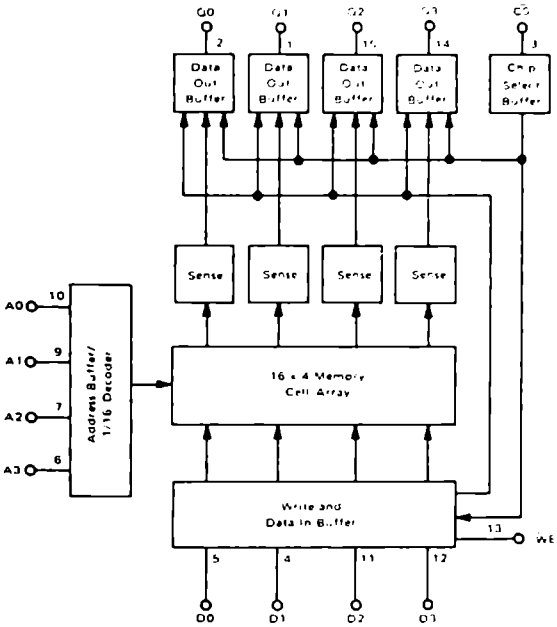
SWITCHING CHARACTERISTICS (Note 1)

Characteristics	Symbol	MCM10144 T_A = 0 to +75°C, V_{EE} = −5.2 Vdc ± 5%		MCM10544 T_A = −55 to +125°C, V_{EE} = −5.2 Vdc ± 5%		Unit	Conditions
		Min	Max	Min	Max		
Read Mode						ns	Measured from 50% of
Chip Select Access Time	t_{ACS}	2.0	10	2.0	10		input to 50% of output.
Chip Select Recovery Time	t_{RCS}	2.0	10	2.0	10		See Note 2.
Address Access Time	t_{AA}	7.0	26	7.0	26		
Write Mode						ns	t_{WSA} = 8.0 ns
Write Pulse Width	t_W	25	–	25	–		Measured at 50% of
Data Setup Time Prior to Write	t_{WSD}	2.0	–	2.0	–		input to 50% of output.
Data Hold Time After Write	t_{WHD}	2.0	–	2.0	–		t_W = 25 ns.
Address Setup Time Prior to Write	t_{WSA}	8.0	–	8.0	–		
Address Hold Time After Write	t_{WHA}	2.0	–	0.0	–		
Chip Select Setup Time Prior to Write	t_{WSCS}	2.0	–	2.0	–		
Chip Select Hold Time After Write	t_{WHCS}	2.0	–	2.0	–		
Write Disable Time	t_{WS}	2.5	10	2.5	10		
Write Recovery Time	t_{WR}	2.5	10	2.5	10		
Rise and Fall Time	t_r, t_f					ns	Measured between 20% and 80% points.
Address to Output		1.5	7.0	1.5	7.0		
$\overline{CS}$ or $\overline{WE}$ to Output		1.5	5.0	1.5	5.0		
Capacitance						pF	Measured with a pulse
Input Capacitance	C_{in}	–	5.0	–	5.0		technique.
Output Capacitance	C_{out}	–	8.0	–	8.0		

NOTES: 1. Test circuit characteristics: R_T = 50 Ω, MCM10144; 100 Ω, MCM10544. $C_L \leq 5.0$ pF (including jig and stray capacitance). Delay should be derated 30 ps/pF for capacitive load up to 50 pF.
2. The maximum Address Access Time is guaranteed to be the Worst-Case Bit in the Memory.
3. For proper use of MECL Memories in a system environment, consult MECL System Design Handbook.

MCM10145/MCM10545

16 X 4-BIT REGISTER FILE (RAM)



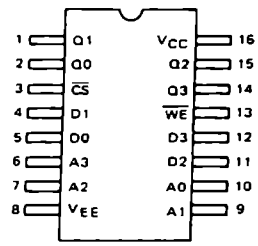
The MCM10145/10545 is a 16 word X 4 bit RAM. Bit selection is achieved by means of a 4-bit address A0 through A3.

The active-low chip select allows memory expansion up to 32 words. The fast chip select access time allows memory expansion without affecting system performance.

The operating mode of the RAM ($\overline{CS}$ input low) is controlled by the $\overline{WE}$ input. With $\overline{WE}$ low the chip is in the write mode—the output is low and the data present at D_n is stored at the selected address. With $\overline{WE}$ high the chip is in the read mode—the data state at the selected memory location is presented non-inverted at Q_n.

- Typical Address Access Time = 10 ns
- Typical Chip Select Access Time = 4.5 ns
- 50 kΩ Pulldown Resistors on All Inputs
- Power Dissipation (470 mW typ @ 25°C)
  Decreases with Increasing Temperature

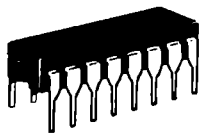
PIN ASSIGNMENT



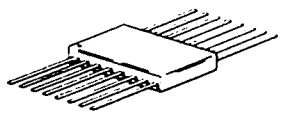
TRUTH TABLE

MODE	INPUT			OUTPUT
	$\overline{CS}$	$\overline{WE}$	D_n	Q_n
Write "0"	L	L	L	L
Write "1"	L	L	H	L
Read	L	H	ø	Q
Disabled	H	ø	ø	L

ø = Don't Care.

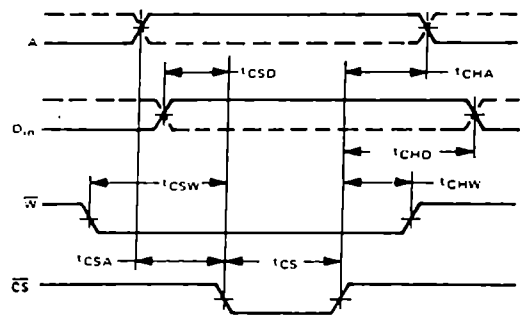


L SUFFIX
CERAMIC PACKAGE
CASE 620



F SUFFIX
CERAMIC PACKAGE
CASE 650

FIGURE 1 – CHIP ENABLE STROBE MODE



ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	−55°C Min	−55°C Max	0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	+125°C Min	+125°C Max	Unit
Power Supply Drain Current	I_{EE}	–	135	–	130	–	125	–	120	–	120	mAdc
Input Current High	I_{inH}	–	375	–	220	–	220	–	220	–	220	μAdc

−55°C and +125°C test values apply to MC105xx devices only.

SWITCHING CHARACTERISTICS (Note 1)

Characteristics	Symbol	MCM10145 T_A = 0 to +75°C, V_{EE} = −5.2 Vdc ± 5% Min	MCM10145 Max	MCM10545 T_A = −55 to +125°C, V_{EE} = −5.2 Vdc ± 5% Min	MCM10545 Max	Unit	Conditions
Read Mode						ns	Measured from 50% of
Chip Select Access Time	t_{ACS}	2.0	8.0	2.0	10		input to 50% of output.
Chip Select Recovery Time	t_{RCS}	2.0	8.0	2.0	10		See Note 2.
Address Access Time	t_{AA}	4.0	15	4.0	18		
Write Mode						ns	t_{WSA} = 5 ns
Write Pulse Width	t_W	8.0	–	8.0	–		Measured at 50% of
Data Setup Time Prior to Write	t_{WSD}	0	–	0	–		input to 50% of output.
Data Hold Time After Write	t_{WHD}	3.0	–	4.0	–		t_W = 8 ns.
Address Setup Time Prior to Write	t_{WSA}	5.0	–	5.0	–		
Address Hold Time After Write	t_{WHA}	1.0	–	3.0	–		
Chip Select Setup Time Prior to Write	t_{WSCS}	0	–	5.0	–		
Chip Select Hold Time After Write	t_{WHCS}	0	–	0	–		
Write Disable Time	t_{WS}	2.0	8.0	2.0	10		
Write Recovery Time	t_{WR}	2.0	8.0	2.0	10		
Chip Enable Strobe Mode						ns	Guaranteed but not
Data Setup Prior to Chip Select	t_{CSD}	0	–	–	–		tested on standard
Write Enable Setup Prior to Chip Select	t_{CSW}	0	–	–	–		product. See Figure 1.
Address Setup Prior to Chip Select	t_{CSA}	0	–	–	–		
Data Hold Time After Chip Select	t_{CHD}	2.0	–	–	–		
Write Enable Hold Time After Chip Select	t_{CHW}	0	–	–	–		
Address Hold Time After Chip Select	t_{CHA}	4.0	–	–	–		
Chip Select Minimum Pulse Width	t_{CS}	18	–	–	–		
Rise and Fall Time	t_r, t_f					ns	Measured between 20%
Address to Output		1.5	7.0	1.5	7.0		and 80% points.
$\overline{CS}$ to Output		1.5	5.0	1.5	5.0		
Capacitance						pF	Measured with a pulse
Input Capacitance	C_{in}	–	6.0	–	6.0		technique.
Output Capacitance	C_{out}	–	8.0	–	8.0		

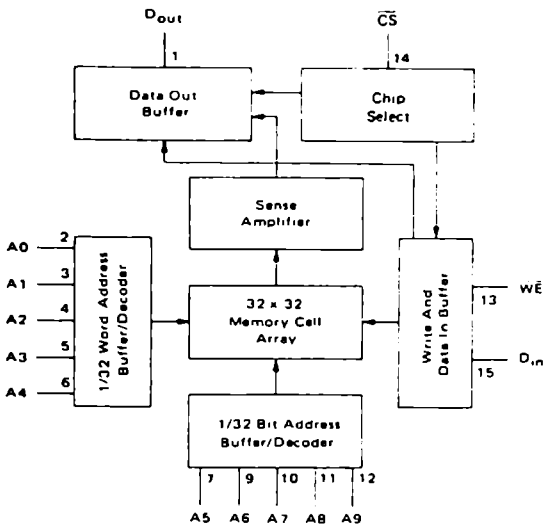
NOTES: 1. Test circuit characteristics: R_T = 50 Ω, MCM10145; 100 Ω, MCM10545. $C_L \leq$ 5.0 pF (including jig and Stray Capacitance). Delay should be derated 30 ps/pF for capacitive loads up to 50 pF.

2. The maximum Address Access Time is guaranteed to be the worst-case bit in the memory.

3. For proper use of MECL Memories in a system environment, consult MECL System Design Handbook.

MCM10146/MCM10546

1024 X 1-BIT RANDOM ACCESS MEMORY



The MCM10146/10546 is a 1024 X 1-bit RAM. Bit selection is achieved by means of a 10-bit address, A0 to A9.

The active-low chip select is provided for memory expansion up to 2048 words.

The operating mode of the RAM ($\overline{CS}$ input low) is controlled by the $\overline{WE}$ input. With $\overline{WE}$ low, the chip is in the write mode, the output, D_{out}, is low and the data state present at D_{in} is stored at the selected address. With $\overline{WE}$ high, the chip is in the read mode and the data stored at the selected memory location will be presented non-inverted at D_{out}. (See Truth Table.)

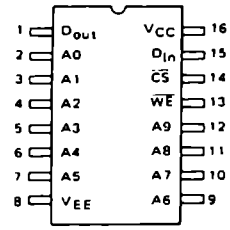
- Pin-for-Pin Compatible with the 10415
- Power Dissipation (520 mW typ @ 25°C) Decreases with Increasing Temperature
- Typical Address Access of 24 ns
- Typical Chip Select Access of 4.0 ns
- 50 kΩ Pulldown Resistor on Chip Select Input

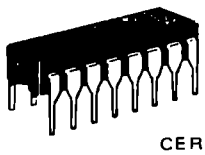
TRUTH TABLE

MODE	INPUT			OUTPUT
	$\overline{CS}$	$\overline{WE}$	D_{in}	D_{out}
Write "0"	L	L	L	L
Write "1"	L	L	H	L
Read	L	H	Ø	Q
Disabled	H	Ø	Ø	L

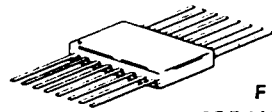
Ø = Don't Care

PIN ASSIGNMENT





L SUFFIX
CERAMIC PACKAGE
CASE 620



F SUFFIX
CERAMIC PACKAGE
CASE 650-03

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	-55°C		0°C		+25°C		+75°C		+125°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_{EE}	–	155	–	150	–	145	–	125	–	125	mAdc
Input Current High	I_{inH}	–.	375	–	220	–	220	–	220	–	220	μAdc
Logic "0" Output Voltage	V_{OL}	-1.970	-1.655	-1.920	-1.665	-1.900	-1.650	-1.880	-1.625	-1.870	-1.545	Vdc

NOTE: -55°C and +125°C test values apply to MCM105XX only.

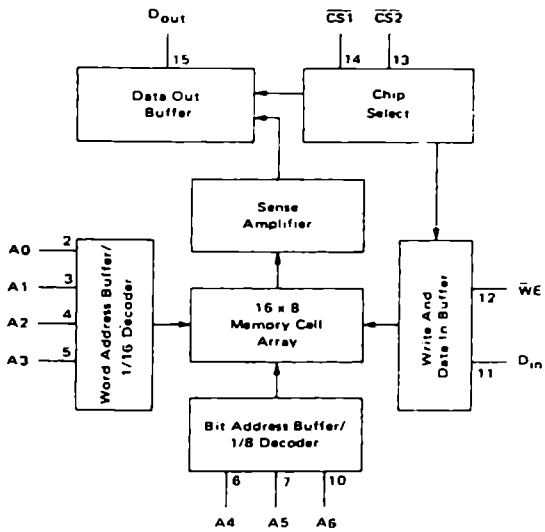
SWITCHING CHARACTERISTICS (Note 1)

Characteristics	Symbol	MCM10146 T_A = 0 to +75°C, V_{EE} = -5.2 Vdc ± 5%		MCM10546 T_A = -55 to +125°C, V_{EE} = -5.2 Vdc ± 5%		Unit	Conditions
		Min	Max	Min	Max		
Read Mode						ns	Measured at 50% of input to 50% of output. See Note 2.
Chip Select Access Time	t_{ACS}	2.0	7.0	2.0	8.0		
Chip Select Recovery Time	t_{RCS}	2.0	7.0	2.0	8.0		
Address Access Time	t_{AA}	8.0	29	8.0	40		
Write Mode						ns	t_{WSA} = 8.0 ns. Measured at 50% of input to 50% of output. t_W = 25 ns
Write Pulse Width (To guarantee writing)	t_W	25	–	25	–		
Data Setup Time Prior to Write	t_{WSD}	5.0	–	5.0	–		
Data Hold Time After Write	t_{WHD}	5.0	–	5.0	–		
Address Setup Time Prior to Write	t_{WSA}	8.0	–	10	–		
Address Hold Time After Write	t_{WHA}	2.0	–	8.0	–		
Chip Select Setup Time Prior to Write	t_{WSCS}	5.0	–	5.0	–		
Chip Select Hold Time After Write	t_{WHCS}	5.0	–	5.0	–		
Write Disable Time	t_{WS}	2.8	7.0	2.8	12		
Write Recovery Time	t_{WR}	2.8	7.0	2.8	12		
Rise and Fall Time	t_r, t_f					ns	Measured between 20% and 80% points.
$\overline{CS}$ or $\overline{WE}$ to Output		1.5	4.0	1.5	4.0		
Address to Output		1.5	8.0	1.5	8.0		
Capacitance						pF	Measured with a pulse technique.
Input Capacitance	C_{in}	–	5.0	–	5.0		
Output Capacitance	C_{out}	–	8.0	–	8.0		

NOTES: 1. Test circuit characteristics: R_T = 50 Ω, MCM10146; 100 Ω, MCM10546. C_L ≤ 5.0 pf including jig and stray capacitance. For Capacitance Loading ≤ 50 pF, delay should be derated by 30 ps/pF.
2. The maximum Address Access Time is guaranteed to be the Worst-Case Bit in the Memory.
3. For proper use of MECL Memories in a system environment, consult MECL System Design Handbook.

MCM10147/MCM10547

128 X 1-BIT RANDOM ACCESS MEMORY



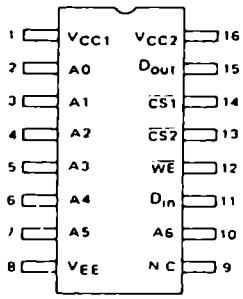
The MCM1047/10547 is a fast 128-word X 1-bit RAM. Bit selection is achieved by means of a 7-bit address, A0 through A6.

The active-low chip selects and fast chip select access time allow easy memory expansion up to 512 words without affecting system performance.

The operating mode ($\overline{CS}$ inputs low) is controlled by the $\overline{WE}$ input. With $\overline{WE}$ low the chip is in the write mode—the output is low and the data present at D_{in} is stored at the selected address. With $\overline{WE}$ high the chip is in the read mode—the data state at the selected memory location is presented non-inverted at D_{out}.

- Typical Address Access Time of 10 ns
- Typical Chip Select Access Time of 4.0 ns
- 50 kΩ Input Pulldown Resistors on All Inputs
- Power Dissipation (420 mW typ @ 25°C) Decreases with Increasing Temperature
- Similar to F10405

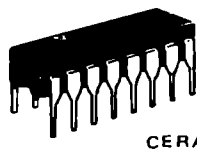
PIN ASSIGNMENT



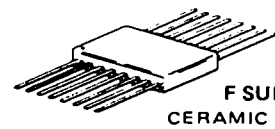
TRUTH TABLE

MODE	INPUT			OUTPUT
	$\overline{CS}$*	$\overline{WE}$	D_{in}	D_{out}
Write "0"	L	L	L	L
Write "1"	L	L	H	L
Read	L	H	ø	Q
Disabled	H	ø	ø	L

*$\overline{CS} = \overline{CS1} + \overline{CS2}$ ø = Don't Care



L SUFFIX
CERAMIC PACKAGE
CASE 620



F SUFFIX
CERAMIC PACKAGE
CASE 650

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	−55°C		0°C		+25°C		+75°C		+125°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_{EE}	–	115	–	105	–	100	–	95	–	95	mAdc
Input Current High	I_{inH}	–	375	–	220	–	220	–	220	–	220	μAdc

−55°C and +125°C test values apply to MC105xx devices only.

SWITCHING CHARACTERISTICS (Note 1)

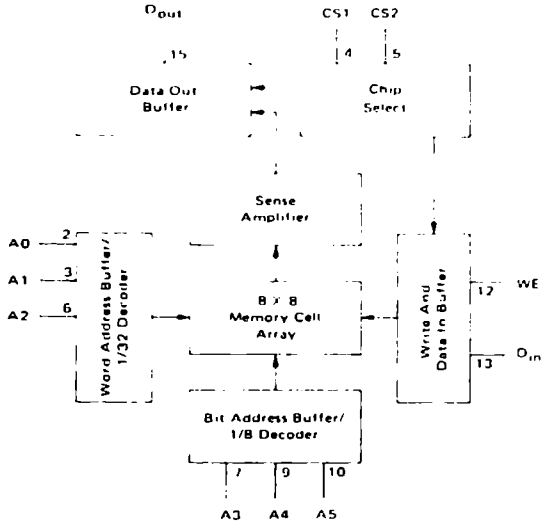
Characteristics	Symbol	MCM10147 T_A = 0 to +75°C, V_{EE} = −5.2 Vdc ±5%		MCM10547 T_A = −55 to +125°C, V_{EE} = −5.2 Vdc ±5%		Unit	Conditions
		Min	Max	Min	Max		
Read Mode						ns	Measured from 50% of input to 50% of output. See Note 2.
Chip Select Access Time	t_{ACS}	2.0	8.0	•	•		
Chip Select Recovery Time	t_{RCS}	2.0	8.0	•	•		
Address Access Time	t_{AA}	5.0	15	•	•		
Write Mode						ns	t_{WSA} = 4.0 ns Measured at 50% of input to 50% of output. t_W = 8.0 ns.
Write Pulse Width	t_W	8.0	–	•	–		
Data Setup Time Prior to Write	t_{WSD}	1.0	–	•	–		
Data Hold Time After Write	t_{WHD}	3.0	–	•	–		
Address Setup Time Prior to Write	t_{WSA}	4.0	–	•	–		
Address Hold Time After Write	t_{WHA}	3.0	–	•	–		
Chip Select Setup Time Prior to Write	t_{WSCS}	1.0	–	•	–		
Chip Select Hold Time After Write	t_{WHCS}	1.0	–	•	–		
Write Disable Time	t_{WS}	2.0	8.0	•	•		
Write Recovery Time	t_{WR}	2.0	8.0	•	•		
Rise and Fall Time	t_r, t_f	1.5	5.0	•	•	ns	Measured between 20% and 80% points.
Capacitance						pF	Measured with a pulse technique.
Input Capacitance	C_{in}	–	5.0	–	•		
Output Capacitance	C_{out}	–	8.0	–	•		

NOTES: 1. Test circuit characteristics: R_T = 50 Ω, MCM10147; 100 Ω, MCM10547.
C_L ≤ 5.0 pF (including jig and stray capacitance).
Delay should be derated 30 ps/pF for capacitive load up to 50 pF.
2. The maximum Address Access Time is guaranteed to be the Worst-Case Bit in the Memory
3. For proper use of MECL Memories in a system environment, consult MECL System Design Handbook.

*To be determined; contact your Motorola representative for up-to-date information.

MCM10148/MCM10548

64 X 1-BIT RANDOM ACCESS MEMORY



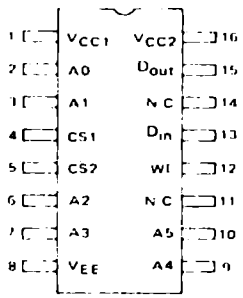
The MCM10148/10548 is a fast 64 word X 1 bit RAM. Bit selection is achieved by means of a 6 bit address, A0 through A5.

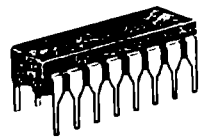
The active low chip selects and fast chip select access time allow easy memory expansion up to 256 words without affecting system performance.

The operating mode ($\overline{CS}$ inputs low) is controlled by the $\overline{WE}$ input. With $\overline{WE}$ low the chip is in the write mode the output is low and the data present at D_{in} is stored at the selected address. With $\overline{WE}$ high the chip is in the read mode – the data state at the selected memory location is presented non inverted at D_{out}.

- Typical Address Access Time of 10 ns
- Typical Chip Select Access Time of 4.0 ns
- 50 kΩ Input Pulldown Resistors on All Inputs
- Power Dissipation (420 mW typ @ 25°C) Decreases with Increasing Temperature

PIN ASSIGNMENT



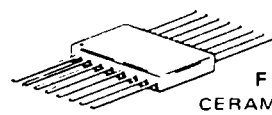


L SUFFIX
CERAMIC PACKAGE
CASE 620

TRUTH TABLE

MODE	INPUT			OUTPUT
	$\overline{CS}$*	$\overline{WE}$	D_{in}	D_{out}
Write 0	L	L	L	L
Write 1	L	L	H	L
Read	L	H	Ø	Q
Disabled	H	Ø	Ø	L

*$\overline{CS}$ = $\overline{CS1}$ • $\overline{CS2}$ • $\overline{CS3}$ Ø = Don't Care



F SUFFIX
CERAMIC PACKAGE
CASE 650

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	-55°C		0°C		+25°C		+75°C		+125°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_{EE}	–	115	–	105	–	100	–	95	–	95	mAdc
Input Current High	I_{inH}	–	375	–	220	–	220	–	220	–	220	μAdc

-55°C and +125°C test values apply to MC105xx devices only

SWITCHING CHARACTERISTICS (Note 1)

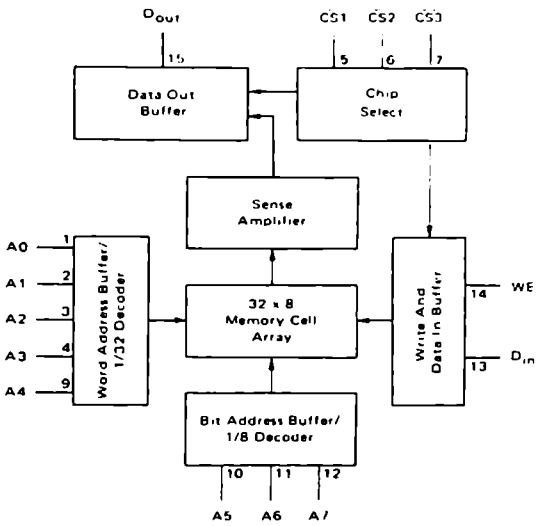
Characteristics	Symbol	MCM10148 T_A = 0 to +75°C, V_{EE} = -5.2 Vdc ± 5%		MCM10548 T_A = -55 to +125°C, V_{EE} = -5.2 Vdc ± 5%		Unit	Conditions
		Min	Max	Min	Max		
Read Mode						ns	Measured from 50% of input to 50% of output. See Note 2.
Chip Select Access Time	t_{ACS}	–	7.5	–	*		
Chip Select Recovery Time	t_{RCS}	–	7.5	–	*		
Address Access Time	t_{AA}	–	15	–	*		
Write Mode						ns	t_{WSA} = 5.0 ns Measured at 50% of input to 50% of output t_W = 8.0 ns.
Write Pulse Width	t_W	8.0		*	–		
Data Setup Time Prior to Write	t_{WSD}	3.0	–	*	–		
Data Hold Time After Write	t_{WHD}	2.0	–	*	–		
Address Setup Time Prior to Write	t_{WSA}	5.0		*	–		
Address Hold Time After Write	t_{WHA}	3.0	–	*	–		
Chip Select Setup Time Prior to Write	t_{WSCS}	3.0	–	*	–		
Chip Select Hold Time After Write	t_{WHCS}	0	–	*	–		
Write Disable Time	t_{WS}	2.0	7.5	*	*		
Write Recovery Time	t_{WR}	2.0	7.5	*	*		
Rise and Fall Time	t_r, t_f	1.5	5.0	*	*	ns	Measured between 20% and 80% points.
Capacitance						pF	Measured with a pulse technique.
Input Capacitance	C_{in}	–	5.0	–	*		
Output Capacitance	C_{out}	–	8.0	–	*		

NOTES: 1. Test circuit characteristics: R_T = 50 Ω, MCM10148, 100 Ω, MCM10548.
$C_L \leq 5.0$ pF (including jig and stray capacitance)
Delay should be derated 30 ps/pF for capacitive load up to 50 pF.
2. The maximum Address Access Time is guaranteed to be the Worst-Case Bit in the Memory.
3. For proper use of MECL Memories in a system environment, consult MECL System Design Handbook.

*To be determined, contact your Motorola representative for up-to-date information.

MCM10152/MCM10552

256 X 1-BIT RANDOM ACCESS MEMORY



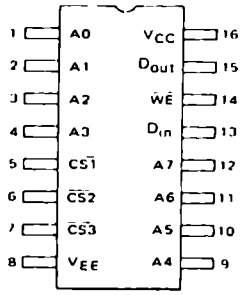
The MCM10152/10552 is a 256-word X 1 bit RAM. Bit selection is achieved by means of an 8 bit address A0 through A7.

The active low chip select allows memory expansion up to 2048 words. The fast chip select access time allows memory expansion without affecting system performance.

The operating mode of the RAM ($\overline{CS}$ inputs low) is controlled by the $\overline{WE}$ input. With $\overline{WE}$ low the chip is in the write mode—the output is low and the data present at D_{in} is stored at the selected address. With $\overline{WE}$ high the chip is in the read mode—the data state at the selected memory location is presented non-inverted at D_{out}.

- Typical Address Access Time = 11 ns
- Typical Chip Select Access Time = 4.0 ns
- 50 kΩ Input Pulldown Resistors on All Inputs
- Power Dissipation (570 mW typ @ 25°C) Decreases with Increasing Temperature
- Pin-for Pin Compatible with F10410/10414

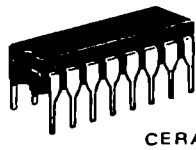
PIN ASSIGNMENT



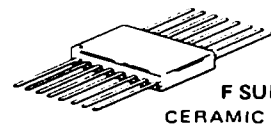
TRUTH TABLE

MODE	INPUT			OUTPUT
	$\overline{CS}$*	$\overline{WE}$	D_{in}	D_{out}
Write "0"	L	L	L	L
Write "1"	L	L	H	L
Read	L	H	Ø	Q
Disabled	H	Ø	Ø	L

*$\overline{CS} = \overline{CS1} + \overline{CS2} + \overline{CS3}$ Ø = Don't Care



L SUFFIX
CERAMIC PACKAGE
CASE 620



F SUFFIX
CERAMIC PACKAGE
CASE 650

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	-55°C		0°C		+25°C		+75°C		+125°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_{EE}		140		135		130		125		125	mAdc
Input Current High	I_{inH}		375		220	-	220		220	-	220	μAdc

55°C and +125°C test values apply to MC105xx devices only

SWITCHING CHARACTERISTICS (Note 1)

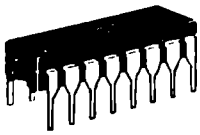
Characteristics	Symbol	MCM10152 T_A = 0 to +75°C, V_{EE} = -5.2 Vdc 5%		MCM10552 T_A = -55 to +125°C, V_{EE} = -5.2 Vdc 5%		Unit	Conditions
		Min	Max	Min	Max		
Read Mode							Measured from 50% of input to 50% of output. See Note 2.
Chip Select Access Time	t_{ACS}	20	75	*	*		
Chip Select Recovery Time	t_{RCS}	20	75	*	*		
Address Access Time	t_{AA}	70	15	*	*		
Write Mode						ns	t_{WSA} 50 ns
Write Pulse Width	t_W	10		*	-		Measured at 50% of input to 50% of output
Data Setup Time Prior to Write	t_{WSD}	20		*	-		t_W 10 ns
Data Hold Time After Write	t_{WHD}	20		*			
Address Setup Time Prior to Write	t_{WSA}	50		*			
Address Hold Time After Write	t_{WHA}	30		*			
Chip Select Setup Time Prior to Write	t_{WSCS}	20		*			
Chip Select Hold Time After Write	t_{WHCS}	20		*			
Write Disable Time	t_{WS}	25	75	*	*		
Write Recovery Time	t_{WR}	25	75	*	*		
Rise and Fall Time	t_r, t_f	15	50	*	*	ns	Measured between 20% and 80% points
Capacitance						pF	Measured with a pulse technique
Input Capacitance	C_{in}		50		*		
Output Capacitance	C_{out}	-	80	-	*		

NOTES 1. Test circuit characteristics: R_T = 50 Ω, MCM10152, 100 Ω, MCM10552
C_L = 5.0 pF (including jig and stray capacitance).
Delay should be derated 30 ps/pF for capacitive load up to 50 pF.
2. The maximum Address Access Time is guaranteed to be the Worst-Case Bit in the Memory.
3. For proper use of MECL Memories in a system environment, consult MECL System Design Handbook.

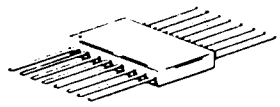
*To be determined, contact your Motorola representative for up-to-date information.

MCM10139/MCM10539

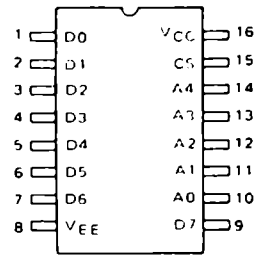
32 x 8-BIT PROGRAMMABLE READ-ONLY MEMORY



L SUFFIX
CERAMIC PACKAGE
CASE 620



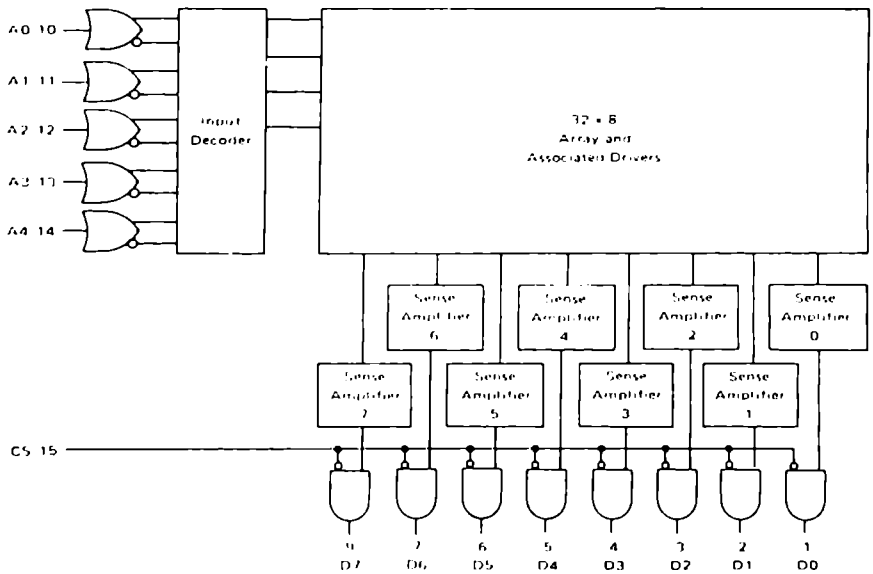
F SUFFIX
CERAMIC PACKAGE
CASE 650



The MCM10139/10539 is a 256-bit field programmable read only memory (PROM). Prior to programming, all stored bits are at logic 0 (low) levels. The logic state of each bit can then be changed by on-chip programming circuitry. The memory has a single negative logic chip enable. When the chip is disabled ($\overline{CS}$ = high), all outputs are forced to a logic 0 (low).

- Typical Address Access Time = 15 ns
- Typical Chip Select Access Time = 10 ns
- 50 kΩ Input Pulldown Resistors on all Inputs
- Power Dissipation (520 mW typ @ 25°C) Decreases with Increasing Temperature

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	-55°C		-0°C		+25°C		+75°C		+125°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_{EE}	–	160	–	150	–	145	–	140	–	160	mAdc
Input Current High	I_{inH}	–	450	–	265	–	265	–	265	–	265	μAdc
Logic "0" Output Voltage	V_{OL}											Vdc
MCM10139		–	–	-2.010	-1.665	-1.990	-1.650	-1.970	-1.625	–	–	
MCM10539		-2.060	-1.655	–	–	-1.990	-1.620	–	–	-1.960	-1.545	

SWITCHING CHARACTERISTICS (Note 1)

Characteristic	Symbol	MCM10139 (V_{EE} = -5.2 Vdc ±5%; T_A = 0°C to +75°C)	MCM10539 (V_{EE} = -5.2 Vdc ± 5 %; T_A = -55°C to +125°C)	Conditions
Chip Select Access Time	t_{ACS}	15 ns Max	*	Measured from 50% of Input to 50% of output. See Note 2
Chip Select Recovery Time	t_{RCS}	15 ns Max	*	
Address Access Time	t_{AA}	20 ns Max	*	
Rise and Fall Time	t_r, t_f	3.0 ns Typ	*	Measured between 20% and 80% points.
Input Capacitance	C_{in}	5.0 pF Max	*	Measured with a pulse technique.
Output Capacitance	C_{out}	8.0 pF Max	*	

NOTES: 1. Test circuit characteristics R_T = 50 Ω, MCM10139, 100 Ω, MCM10539. $C_L \leq 6.0$ pF including jig and stray capacitance. For Capacitance Loading ≤50 pF, delay should be derated by 30 ps/pF.
2. The maximum Address Access Time is guaranteed to be the Worst-Case Bit in the Memory.
3. For proper use of MECL Memories in a system environment, consult MECL System Design Handbook.

*To be determined; contact your Motorola representative for up to-date information.

FIGURE 1 – MANUAL PROGRAMMING CIRCUIT

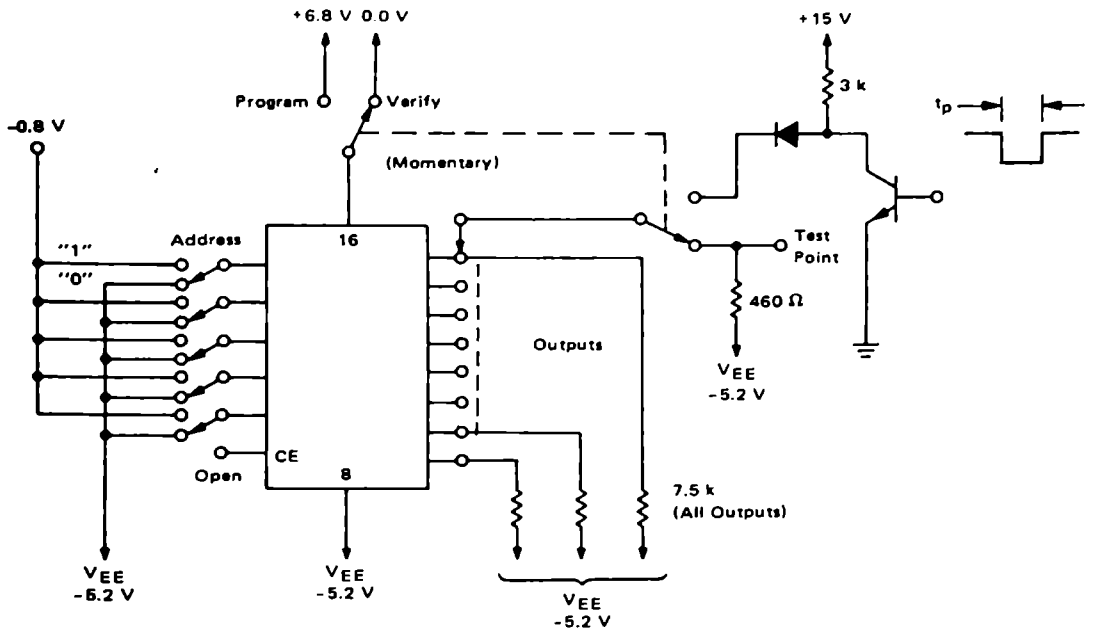
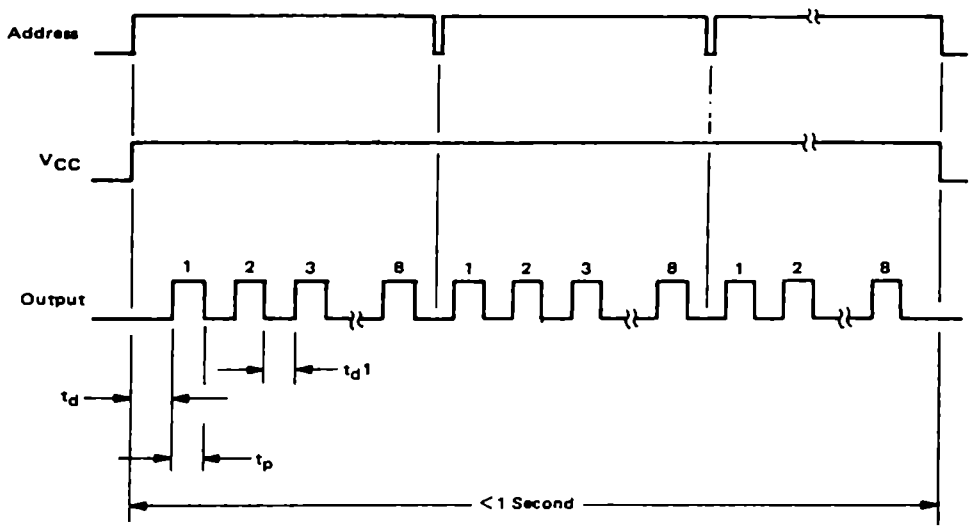


FIGURE 2 – AUTOMATIC PROGRAMMING CIRCUIT



RECOMMENDED PROGRAMMING PROCEDURE*

The MCM10139 is shipped with all bits at logical "0" (low). To write logical "1s", proceed as follows.

MANUAL (See Figure 1)

Step 1 Connect V_{EE} (Pin 8) to -5.2 V and V_{CC} (Pin 16) to 0.0 V. Address the word to be programmed by applying -1.2 to -0.6 volts for a logic "1" and -5.2 to -4.2 volts for a logic "0" to the appropriate address inputs.

Step 2 Raise V_{CC} (Pin 16) to +6.8 volts.

Step 3 After V_{CC} has stabilized at +6.8 volts (including any ringing which may be present on the V_{CC} line), apply a current pulse of 2.5 mA to the output pin corresponding to the bit to be programmed to a logic "1".

Step 4 Return V_{CC} to 0.0 Volts.

CAUTION

To prevent excessive chip temperature rise, V_{CC} should not be allowed to remain at +6.8 volts for more than 1 second

Step 5 Verify that the selected bit has programmed by connecting a 460 Ω resistor to -5.2 volts and measuring the voltage at the output pin. If a logic "1" is not detected at the output, the procedure should be repeated once. During verification V_{IH} should be -1.0 to -0.6 volts.

Step 6 If verification is positive, proceed to the next bit to be programmed.

AUTOMATIC (See Figure 2)

Step 1 Connect V_{EE} (Pin 8) to -5.2 volts and V_{CC} (Pin 16) to 0.0 volts. Apply the proper address data and raise V_{CC} (Pin 16) to +6.8 volts.

Step 2 After a minimum delay of 100 μs and a maximum delay of 1.0 ms, apply a 2.5 mA current pulse to the first bit to be programmed ($0.1 \leq PW \leq 1$ ms).

Step 3 Repeat Step 2 for each bit of the selected word specified as a logic "1". (Program only one bit at a time. The delay between output programming pulses should be equal to or less than 1.0 ms.)

Step 4 After all the desired bits of the selected word have been programmed, change address data and repeat Steps 2 and 3.

NOTE: If all the maximum times listed above are maintained, the entire memory will program in less than 1 second. Therefore, it would be permissible for V_{CC} to remain at +6.8 volts during the entire programming time.

Step 5 After stepping through all address words, return V_{CC} to 0.0 volts and verify that each bit has programmed. If one or more bits have not programmed, repeat the entire procedure once. During verification V_{IH} should be -1.0 to -0.6 volts.

*NOTE: For devices that program incorrectly—return serialized units with individual truth tables. Noncompliance voids warranty.

PROGRAMMING SPECIFICATIONS

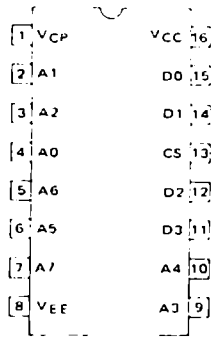
Characteristic	Symbol	Limits			Units	Conditions
		Min	Typ	Max		
Power Supply Voltage	V_{EE}	-5.46	-5.2	-4.94	Vdc	
To Program	V_{CCP}	+6.04	+6.8	+7.56	Vdc	
To Verify	V_{CCV}	0	0	0	Vdc	
Programming Supply Current	I_{CCP}	–	200	600	mA	V_{CC} = +6.8 Vdc
Address Voltage	V_{IH} Program	-1.2	–	-0.6	Vdc	
Logical "1"	V_{IH} Verify	-1.0	–	-0.6	Vdc	
Logical "0"	V_{IL}	-5.2	–	-4.2	Vdc	
Maximum Time at $V_{CC} = V_{CCP}$	–	–	–	1.0	sec	
Output Programming Current	I_{OP}	2.0	2.5	3.0	mAdc	
Output Program Pulse Width	t_p	0.5	–	1.0	ms	
Output Pulse Rise Time	–	–	–	10	μs	
Programming Pulse Delay (1)						
Following V_{CC} change	t_d	0.1	–	1.0	ms	
Between Output Pulses	t_d	0.01	–	1.0	ms	

NOTE 1. Maximum is specified to minimize the amount of time V_{CC} is at +6.8 volts.

MCM10149/MCM10549

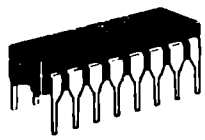
256 X 4-BIT PROGRAMMABLE READ-ONLY MEMORY

PIN ASSIGNMENT

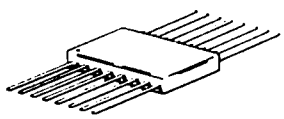


The MCM10149/10549 is a 256 word X 4 bit field programmable read only memory (PROM). Prior to programming, all stored bits are at logic 1 (high) levels. The logic state of each bit can then be changed by on-chip programming circuitry. The memory has a single negative logic chip enable. When the chip is disabled ($\overline{CS}$ high), all outputs are forced to a logic 0 (low).

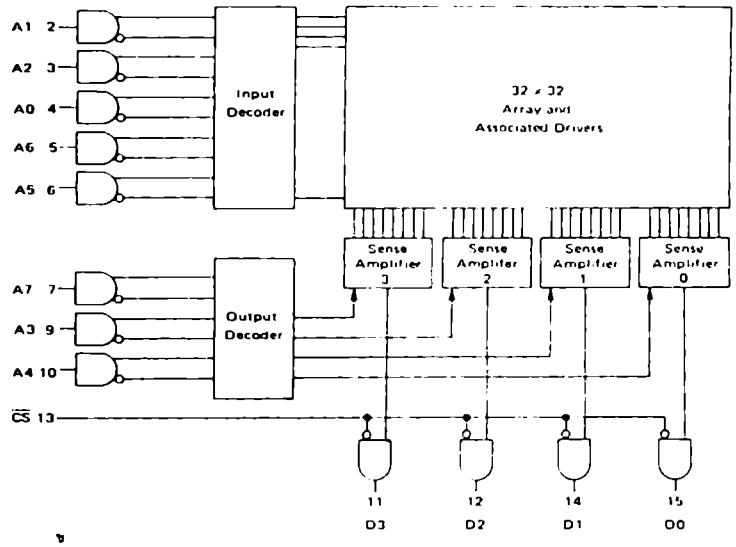
- Typical Address Access Time of 20 ns
- Typical Chip Select Access Time of 8.0 ns
- 50 kΩ Input Pulldown Resistors on All Inputs
- Power Dissipation (540 mW typ @ 25°C) Decreases with Increasing Temperature



L SUFFIX
CERAMIC PACKAGE
CASE 620



F SUFFIX
CERAMIC PACKAGE
CASE 650



ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	−55°C Min	−55°C Max	0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	+125°C Min	+125°C Max	Unit
Power Supply Drain Current	I_{EE}	–	140	–	135	–	130	–	125	–	125	mAdc
Input Current High	I_{inH}	–	450	–	265	–	265	–	265	–	265	μAdc

55°C and +125°C test values apply to MC105xx devices only

SWITCHING CHARACTERISTICS (Note 1)

Characteristics	Symbol	MCM10149 T_A = 0 to +75°C, V_{EE} = −5.2 Vdc ± 5% Min	MCM10149 Max	MCM10549 T_A = −55 to +125°C, V_{EE} = −5.2 Vdc ± 5% Min	MCM10549 Max	Unit	Conditions
Read Mode						ns	Measured from 50% of input to 50% of output. See Note 1.
Chip Select Access Time	t_{ACS}	2.0	10	*	*		
Chip Select Recovery Time	t_{RCS}	2.0	10	*	*		
Address Access Time	t_{AA}	7.0	25	*	*		
Rise and Fall Time	t_r, t_f	1.5	7.0	*	*	ns	Measured between 20% and 80% points.
Capacitance						pF	Measured with a pulse technique.
Input Capacitance	C_{in}	–	5.0	–	5.0		
Output Capacitance	C_{out}	–	8.0	–	8.0		

NOTES: 1. Test circuit characteristics. R_T = 50 Ω, MCM10149, 100 Ω, MCM10549.
$C_L \leq 5.0$ pF (including jig and stray capacitance)
Delay should be derated 30 ps/pF for capacitive load up to 50 pF
2. The maximum Address Access Time is guaranteed to be the Worst-Case Bit in the Memory.
3. For proper use of MECL Memories in a system environment, consult MECL System Design Handbook.
4. $V_{CP} = V_{CC} = Gnd$ for normal operation.

*To be determined, contact your Motorola representative for up-to-date information.

PROGRAMMING THE MCM10149 †

During programming of the MCM10149, input pins 7, 9, and 10 are addressed with standard MECL 10K logic levels. However, during programming input pins 2, 3, 4, 5, and 6 are addressed with $0 \text{ V} \leq V_{IH} \leq +0.25$ V and $V_{EE} \leq V_{IL} \leq -3.0$ V. It should be stressed that this deviation from standard input levels is required only during the programming mode. During normal operation, standard MECL 10,000 input levels must be used.

With these requirements met, and with $V_{CP} = V_{CC} = 0$ V and $V_{EE} = -5.2$ V ± 5%, the address is set up. After a minimum of 100 ns delay, V_{CP} (pin 1) is ramped up to +12 V ± 0.5 V (total voltage V_{CP} to V_{EE} is now 17.2 V, +12 V − [−5.2 V]). The rise time of this V_{CP} voltage pulse should be in the 1-10 μs range, while its pulse width (t_{W1}) should be greater than 100 μs but less than 1 ms. The V_{CP} supply current at +12 V will be approximately 525 mA while current drain from V_{CC} will be approximately 175 mA. A current limit should therefore be set on both of these supplies. The current limit on the V_{CP} supply should be set at 700 mA while the V_{CC} supply should be limited to 250 mA. It should be noted that the V_{EE} supply must be capable of sinking the combined current of the V_{CC} and V_{CP} supplies while maintaining a voltage of −5.2 V ± 5%.

Coincident with, or at some delay after the V_{CP} pulse has reached its 100% level, the desired bit to be fused can be selected. This is done by taking the corresonding output pin to a voltage of +2.85 V ± 5%. It is to be noted that only one bit is to be fused at a time. The other three unselected outputs should remain terminated through their 50 ohm load resistor (100 ohm for MCM10549) to −2.0 V. Current into the selected output is 5 mA maximum.

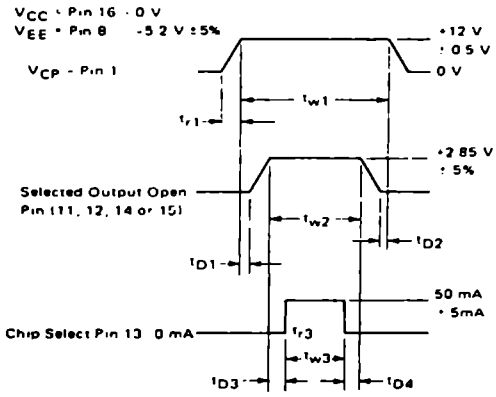
After the bit select pulse has been applied to the appropriate output, the fusing current is sourced out of the chip select pin 13. The 0% to 100% rise time of this current pulse should be 250 ns max. Its pulse width should be greater than 100 μs. Pulse magnitude is 50 mA ± 5.0 mA. The voltage clamp on this current source is to be −6.0 V.

After the fusing current source has returned 0 mA, the bit select pulse is returned to it initial level, i.e., the output is returned through its load to −2.0 V. Thereafter, V_{CP} is returned to 0 V. Strobing of the outputs to determine success in programming should occur no sooner than 100 ns after V_{CP} has returned to 0 V. The remaining bits are programmed in a similar fashion.

† NOTE: For devices that program incorrectly, return serialized units with individual truth tables. Non compliance voids warranty.

PROGRAMMING SPECIFICATIONS

The following timing diagrams and fusing information represent programming specifications for the MCM10149.



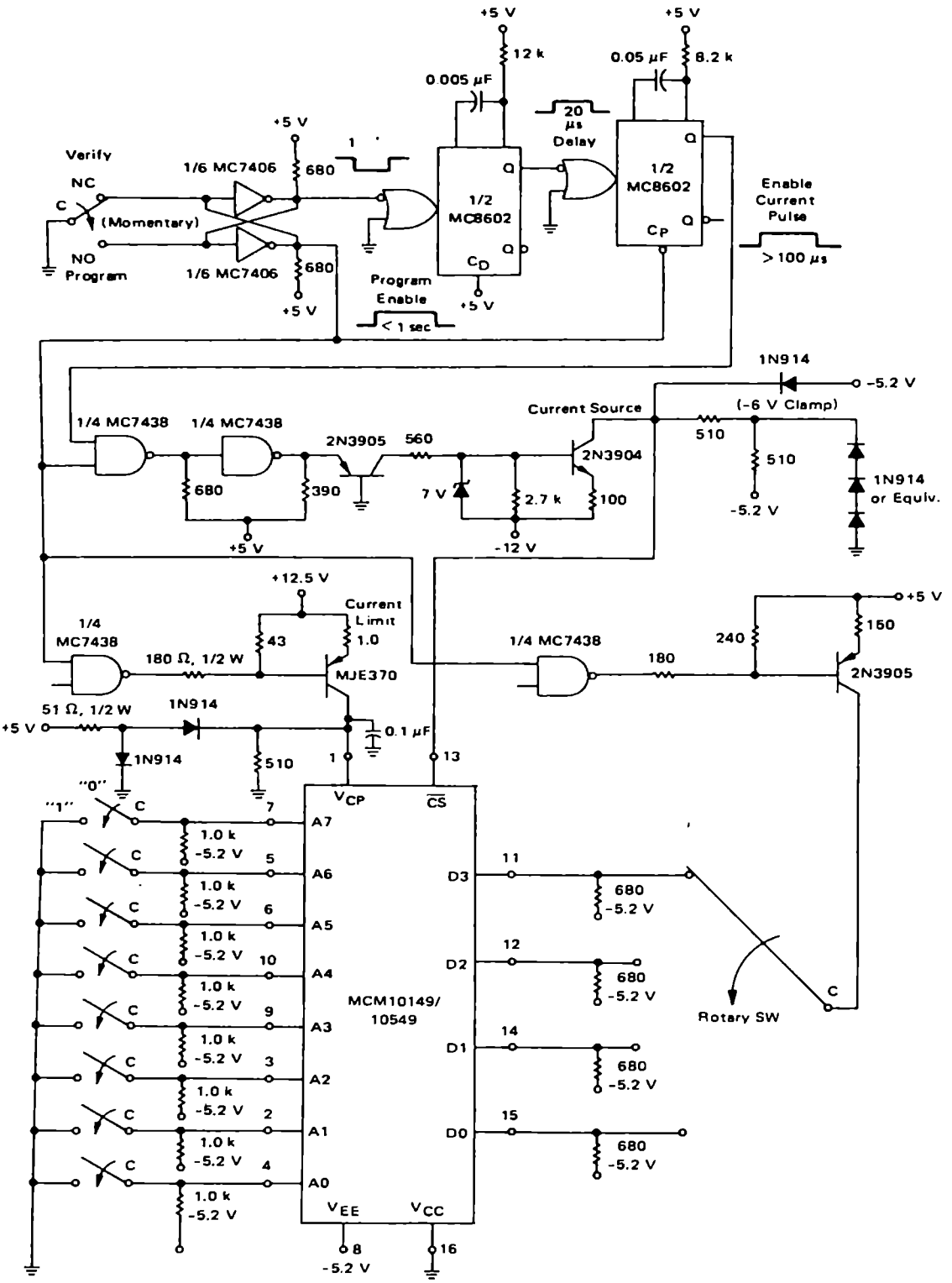
The timing diagram is shown for programming one bit. Note that only one bit is blown at a time. All addressing must be done 100 ns prior to the beginning of the V_{CP} pulse, i.e., V_{CP} = 0 V. Likewise, strobing of the outputs to determine success in programming should occur no sooner than 100 ns after V_{CP} returns to 0 V.

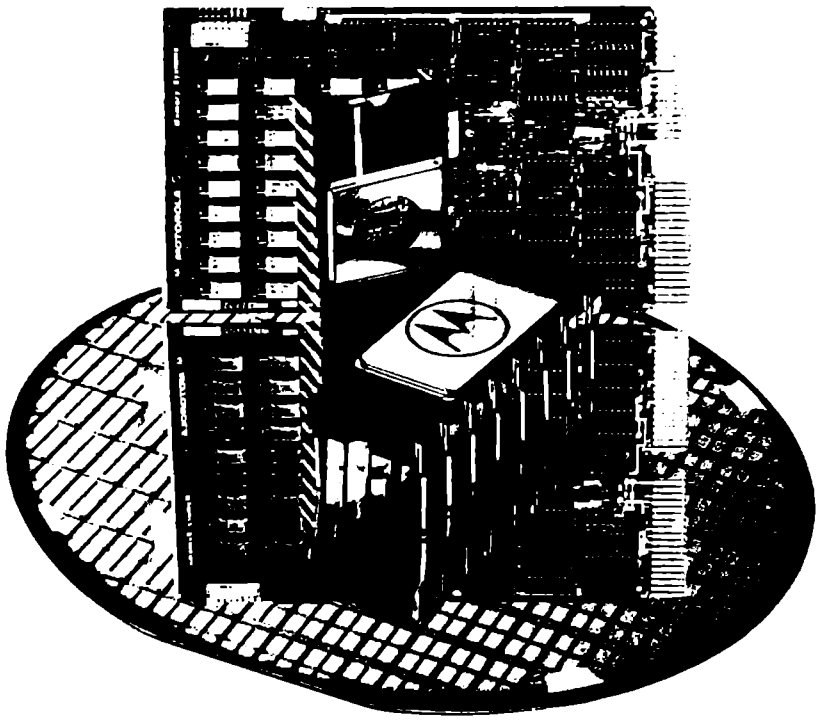
Note that the fusing current is defined as a positive current out of the chip select, pin 13. A programming duty cycle of ≤ 15% is to be observed.

Definitions and values of timing symbols are as follows.

Symbol	Definition	Value
t_{r1}	Rise Time, Programming Voltage	≥ 1 μs
t_{w1}	Pulse Width, Programming Voltage	≥ 100 μs < 1 ms
t_{D1}	Delay Time, Programming Voltage Pulse to Bit Select Pulse	≥ 0
t_{w2}	Pulse Width, Bit Select	≥ 100 μs
t_{D2}	Delay Time, Bit Select Pulse to Programming Voltage Pulse	≥ 0
t_{D3}	Delay Time, Bit Select Pulse to Programming Current Pulse	≥ 1 μs
t_{r3}	Rise Time, Programming Current Pulse	250 ns max
t_{w3}	Pulse Width, Programming Current Pulse	≥ 100 μs
t_{D4}	Delay Time, Programming Current Pulse to Bit Select Pulse	≥ 1 μs

MANUAL PROGRAMMING CIRCUIT





Memory Boards

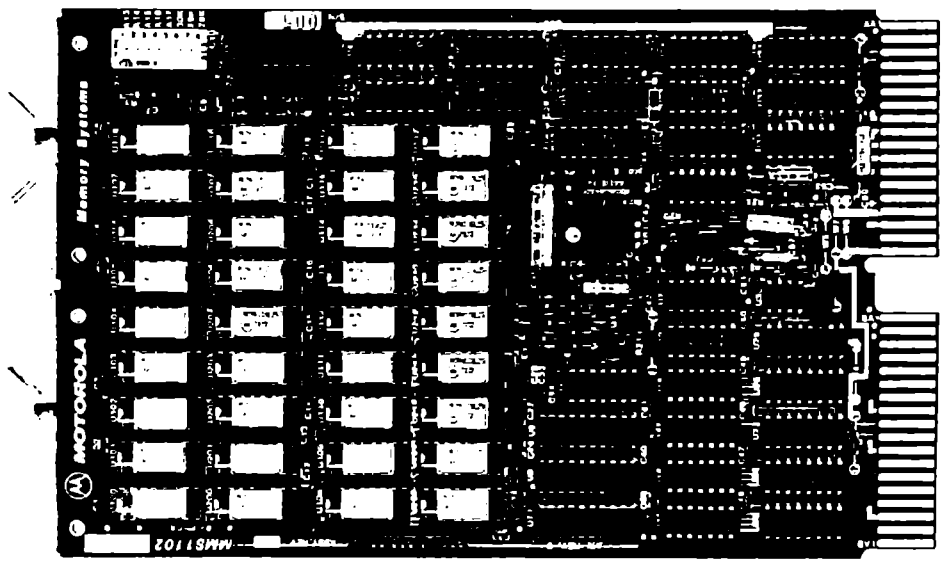
MOTOROLA

MMS1102

Advance Information

ADD-ON MEMORY CARD FOR THE LSI-11 FAMILY

The MMS1102 is a dual height (5.187" × 8.94") add-on memory card for the LSI-11 family of computers. It is compatible with the LSI-11/2 and LSI-11 processors as well as the PDP 11V03 computer systems. It incorporates byte parity storage as well as generation and detection logic.



Specification Highlights

INTERFACE	LSI-11, "Q" Bus-Plus.
CAPACITY	8K words × 16 bits, 16K words × 16 bits, 32K words × 16 bits.
PARITY	Optional on-board storage, generation and detection logic for both upper and lower byte. Parity option does not degrade access times.
SPEED	The MMS1102-3X has a read access time under 300 ns. Read access time is defined here as the time from receipt of SYNC H to the transmission of RPLY H, assuming that the SYNC H to DIN H time is no greater than 160 ns.
ADDRESSING	Switch-selectable, to start on any 4K word boundary between 0 and 128K.
I/O PAGE USE	Three switches allow any one of the lowest three kilowords of the I/O page to be used as Read/Write memory.
BATTERY BACKUP	Jumper selectable; allows the MMS1102 to be operated from a separate uninterrupted power source (+5 BBU and +12 BBU).
REFRESH	Implemented internal to the MMS1102 and totally transparent to the system.

MMS1102-XX ORDERING INFORMATION

Storage Capacity	Part Number (With Parity and Controller)	Part Number (No Parity)
16 Kilobytes	MMS1102-31PC	MMS1102-31
32 Kilobytes	MMS1102-32PC	MMS1102-32
64 Kilobytes	MMS1102-34PC	MMS1102-34

MMS1102-3X — AC OPERATING CHARACTERISTICS

	Read Access (ns)		Write Access (ns)	
	Typical	Worst Case	Typical	Worst Case
Access Time*	250	300	125	175
Cycle Time**	470	500	350	400
Refresh Latency***	175	400	175	400

*As measured from receipt of RSYNC H to transmission of TRPLY H.
**This is the reciprocal of the maximum continuous transfer rate, assuming no refresh interference.
***Occurs approximately once every 16 microseconds.

MMS1102 POWER REQUIREMENTS

Nominal Voltage	Min	Max	Current Requirements (mA)				Input Pins
			Standby		Active		
			Typical	Worst Case	Typical	Worst Case	
+5 VDC (Total)	4.75	5.25	725 925*	800 1000*	775 1000*	850 1100*	AA2, BA2
+12 VDC	11.40	12.60	100	150	250	400	AD2, BD2
+5 VDC (BBU)	4.75	5.25	400	500	450	550	AV1**
+12 VDC (BBU)	11.40	12.60	100	150	250	400	AS1***

*Parity version only.
**In systems without battery backup this voltage is obtained from the regular +5 V rail via an on-board jumper.
***The +12 V supply requirement can be met via an on-board jumper from the regular +12 V rail.

MMS1102 BACKPLANE CONNECTOR PIN ASSIGNMENT

Row	A		B	
Side	1	2	1	2
Pin				
A	—	+5 V	BDCOK H	+5 V
B	—	—	—	—
C	BAD16 L**	GND	—	GND
D	BAD17 L	+12 V	—	+12 V
E	—	BDOUT L	—	BDAL 2 L
F	—	BRPLY L	—	BDAL 3 L
H	—	BDIN L	—	BDAL 4 L
J	GND	BSYNC L	GND	BDAL 5 L
K	} *	BWTBT L	} *	BDAL 6 L
L	}	—	}	BDAL 7 L
M	GND	BIAKI L } ***	GND	BDAL 8 L
N	—	BIAKO L }	—	BDAL 9 L
P	—	BBS7 L	—	BDAL 10 L
R	BREF L	BDMGI L } ***	—	BDAL 11 L
S	+12 V BBU	BDMGO L }	—	BDAL 12 L
T	GND	—	GND	BDAL 13 L
U	—	BDAL 0 L	—	BDAL 14 L
V	+5 V BBU	BDAL 1 L	+5 V	BDAL 15 L

*Must be hardwired on backplane or damage to MOS devices may result.
**Or PRTYER or PRTYCK.
***Hardwired on MMS1102.

MOTOROLA

MMS1122

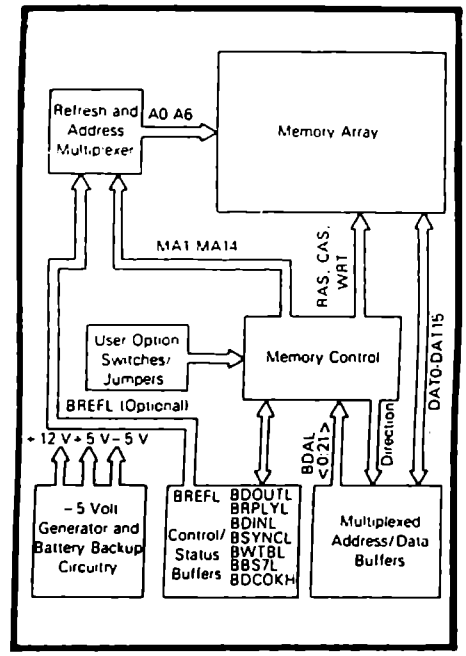
Product Preview

ADD-IN MEMORY CARD FOR THE LSI-11 FAMILY

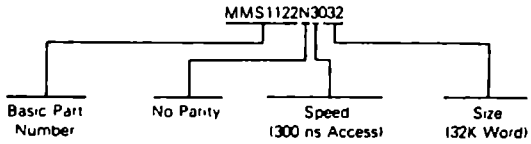
The MMS1122 is a dual height (5.19" × 8.94") add-on memory card for the LSI-11 family of computers. It is compatible with LSI-11, LSI-11/2, and LSI-11/23 processors as well as PDP-11V03* computer systems. It utilizes MCM4132L 32K RAM modules.

FEATURES

- Capacity of 32K Words, Each 16-Bits Long
- Effective Capacity is Switch Selectable at any 1K Word Increment
- Addressing is Switch Selectable to Start on Any 1K Word Boundary From 0 to 127K
- Read Access Time of 300 ns (max.)
- Cycle Time 500 ns (max.)
- Refresh Implemented Internal to the Card (Transparent to the System). On-Board Jumpers Permit Synchronization of Refresh if Desired.
- Jumper Selectable Battery Backup Provisions Allow Use of Separate Power Source
- LSI-11 (Q-Bus and Q-Bus Plus) Interface Compatible



ORDERING INFORMATION



SIMILAR PRODUCTS

Other Add-In memory cards for the LSI-11 family include the MMS1102 and MMS1132.

ENVIRONMENTAL RATINGS

Rating	Symbol	Limit	Units
Operating Temperature	T_A	0 to +50	°C
Storage Temperature	T_{stg}	−40 to +80	°C
Relative Humidity (Without Condensation)	RH	5 to 90	%

*PDP is a trademark of Digital Equipment Corporation

PHYSICAL DIMENSIONS

Dimension	Millimeters	Inches
Width	227 08	8 94
Height	131 75	5 19
PC Board Thickness	1 575	0 062
Clearance Required (Component Side)*	0 826	0 325
Clearance Required (Solder Side)*	1 524	0 060

*Measured from surface of PC Board

POWER REQUIREMENTS (+5 Volts)

Mode	Pin	Current Required		Units
		Typical	Worst-Case	
Active	**	0 775	0 850	Adc
Standby	**	0 725	0 800	Adc
Battery Backup	AV1	0 400	0 500	Adc

POWER REQUIREMENTS (−12 Volts)

Mode	Pin	Current Required		Units
		Typical	Worst-Case	
Active	***	0 250	0 400	Adc
Standby	***	0 100	0 150	Adc
Battery Backup	AS1	0 100	0 150	Adc

**AA2, BA2, BV1, AV1 (Jumper option allows all +5 V current to be supplied by AA2, BA2, and BV1 if battery backup operation is not required)

***AD2, BD2, AS1 (Jumper option allows all +12 V current to be supplied by AD2 and BD2 if battery backup operation is not required)

AC OPERATING CHARACTERISTICS

Characteristic	Typical	Worst-Case	Unit
Cycle Time – Read or Write	500	525	ns
Access Time – Read Write	250 125	300 175	ns

BACKPLANE CONNECTOR PIN ASSIGNMENT

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
AA2	+5 V	AL1	(Note 1)	AU2	BDAL (0)	BF1	BDAL (21)	BN2	BDAL (9)
AC1	BDAL (16)	AK2	BWTBT L	AV1	+5 V BBU[2]	BF2	BDAL (3)	BP2	BDAL (10)
AC2	GND	AM1	GND	AV2	BDAL (1)	BH2	BDAL (4)	BR2	BDAL (11)
AD1	BDAL (17)	AM2	BIAKI L	BA1	BDCOK H	BJ1	GND	BS2	BDAL (12)
AD2	+12 V	AN2	BIAKO L	BA2	+5 V	BJ2	BDAL (5)	BT1	GND
AE2	BDOUT L	AP2	BBS7 L	BC1	BDAL (18)	BK1	(Note 3)	BT2	BDAL (3)
AF2	BRPLY L	AR1	BREF L	BC2	GND	BL1	(Note 3)	BU2	BDAL (14)
AH2	BDIN L	AR2	BDMGI L	BD1	BDAL (19)	BK2	BDAL (6)	BV1	+5 V
AJ1	GND	AS2	BDMGO L	BD2	+12 V	BL2	BDAL (7)	BV2	BDAL (15)
AJ2	BSYNC L	AS1	+12 V BBU[2]	BE1	BDAL (20)	BM1	GND		
AK1	(Note 1)	AT1	GND	BE2	BDAL (2)	BM2	BDAL (8)	BV2	BDAL (15)

Notes: (1) AK1 and AL1 normally connected together at backplane. User jumper option allows negative 5 V supply to be connected through AL1 if desired

(2) +12 V BBU and +5 V BBU may be driven by normal +5 V and +12 V if desired

(3) User jumper options allow BK1 and BL1 to be used for synchronous refresh

MOTOROLA

MMS1132

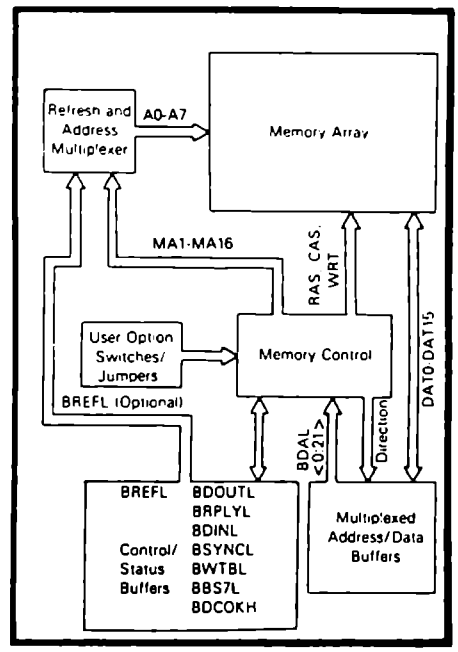
Product Preview

ADD-IN MEMORY CARD FOR THE LSI-11 FAMILY

The MMS1132 is a dual height (5.19" x 8.94") add-on memory card for the LSI-11 family of computers. It is compatible with LSI-11, LSI-11/2, and LSI-11/23 processors as well as PDP-11V03* computer systems. It utilizes MCM6633L 32K RAM or MCM6665L 64K RAM chips.

FEATURES

- Capacity of up to128K Words, Each 16-Bits Long Without Parity, 18-Bits with Parity
- Effective Capacity is Switch Selectable at any 1K Word Increment
- Addressing is Switch Selectable to Start on Any 1K Word Boundary From 0 to 127K
- Optional Parity and On-Board Parity Controller
- Read Access Time of 300 ns (max.)
- Cycle Time 500 ns (max.)
- Refresh Implemented Internal to the Card (Transparent to the System). On-Board Jumpers Permit Synchronization of Refresh if Desired
- Single +5 V Power Supply
- Jumper Selectable Battery Backup Provisions Allow Use of Separate Power Source
- LSI-11 (Q-Bus and Q-Bus Plus) Interface Compatible



ORDERING INFORMATION

MMS1132 X 3 $Z_2Z_1Z_0$

Basic Part Number

X	Option
P	Parity
N	No Parity

Speed (300 ns Access)

Z_2	Z_1	Z_0	Capacity
0	3	2	32K Words
0	6	4	64K Words
1	2	8	128K Words

Note: K = 1024, Word = 16 Bits W/O, 18 Bits With Parity

SIMILAR PRODUCTS

Other Add-In memory cards for the LSI-11 family include the MMS1102 and MMS1122.

ENVIRONMENTAL RATINGS

Rating	Symbol	Limit	Units
Operating Temperature	T_A	0 to +50	°C
Storage Temperature	T_{stg}	−40 to +80	°C
Relative Humidity (Without Condensation)	RH	5 to 90	%

*PDP is a trademark of Digital Equipment Corporation.

PHYSICAL DIMENSIONS

Dimension	Millimeters	Inches
Width	227 08	8 94
Height	131 75	5 19
PC Board Thickness	1 575	0 062
Clearance Required (Component Side)*	0 826	0 325
Clearance Required (Solder Side)*	1 524	0 060

*Measured from surface of PC Board

POWER REQUIREMENTS (+5 V Only Required)

Mode	Pins	Total Required Current				Units
		32K Word Capacity		64 or 128K Word Capacity		
		Typical	Worst-Case	Typical	Worst-Case	
Active	AA2, BA2, BV1, AV1**	1 375	1 80	1 50	1.95	Adc
Standby	AA2, BA2, BV1, AV1**	0 965	1 15	1 05	1 25	Adc
Battery Backup	AV1	0 640	0 86	0 70	0 93	Adc

**Jumper option allows all current to be supplied by AA2, BA2, and BV1 if battery backup operation is not required

AC OPERATING CHARACTERISTICS

Characteristic	Typical	Worst-Case	Units
Cycle Time – Read	470	500	ns
Write	350	400	
Access Time – Read	250	300	ns
Write	125	175	

BACKPLANE CONNECTOR PIN ASSIGNMENT

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
AA2	+5 V	AL1	(Note 1)	AU2	BDAL (0)	BF1	BDAL (21)	BN2	BDAL (9)
AC1	BDAL (16)	AK2	BWTBT L	AV1	+5 V BBU[2]	BF2	BDAL (3)	BP2	BDAL (10)
AC2	GND	AM1	GND	AV2	BDAL (1)	BH2	BDAL (4)	BR2	BDAL (11)
AD1	BDAL (17)	AM2	BIAKI L	BA1	BDCOK H	BJ1	GND	BS2	BDAL (12)
AD2	+12 V	AN2	BIAKO L	BA2	+5 V	BJ2	BDAL (5)	BT1	GND
AE2	BDOUT L	AP2	BBS7 L	BC1	BDAL (18)	BK1	(Note 3)	BT2	BDAL (3)
AF2	BRPLY L	AR1	BREF L	BC2	GND	BL1	(Note 3)	BU2	BDAL (14)
AH2	BDIN L	AR2	BDMGI L	BD1	BDAL (19)	BK2	BDAL (6)	BV1	+5 V
AJ1	GND	AS2	BDMGO L	BD2	+12 V	BL2	BDAL (7)	BV2	BDAL (15)
AJ2	BSYNC L	AS1	+12 V BBU[2]	BE1	BDAL (20)	BM1	GND		
AK1	(Note 1)	AT1	GND	BE2	BDAL (2)	BM2	BDAL (8)	BV2	BDAL (15)

Notes: (1) +5 V BBU may be driven by normal +5 V if desired
(2) User jumper options allow BK1 and BL1 to be used for synchronous refresh.

MOTOROLA

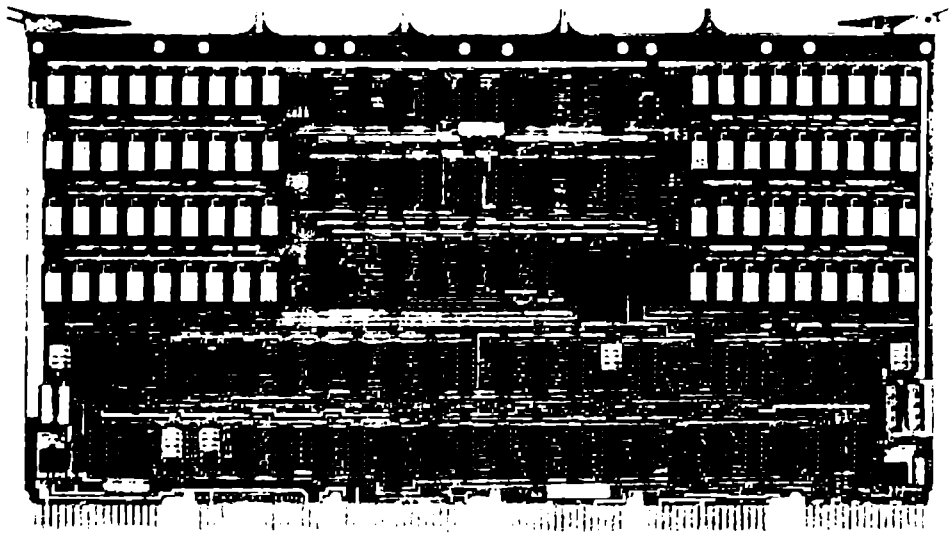
MMS1117

Advance Information

PDP-11* UNIBUS* COMPATIBLE RANDOM ACCESS MEMORIES, UP TO 128 KILOBYTES OF STORAGE CAPACITY PLUS OPTIONAL PARITY CONTROLLER ON A SINGLE CARD

The MMS1117 family of memory systems offers owners of PCP-11* computers an opportunity to easily add storage capacity and parity features to their system. Each member of the family is contained on a single plug-in circuit card that interfaces mechanically and electrically with the following models of UNIBUS* PDP-11* processors: 11/04, 11/05, 11/10, 11/34, 11/35, 11/40, 11/45, 11/50, 11/55, and 11/60. It plugs into a single hex SPC slot in any of the following backplanes: DD11-B, DD11-C, DD11-D and DD11-P.

The MMS1117 can provide up to 128K 8-bit bytes of main memory on a single module. Quick address select changes are possible via onboard switches. In addition, 1 or 2 kilowords of I/O page can selectively be made available for random access storage. Optional parity as well as full parity generation, detection, and exception control circuits can be provided on the same card with the memory. No additional bus loading is imposed on the system by the addition of the fully compatible parity controller option.



MMS1117 FEATURES

- High Density
- Low Cost
- Fast Access and Cycle Times
- Low Power
- Fully UNIBUS Compatible
- High Reliability
- One UNIBUS Load

*Trademark of Digital Equipment Corporation

MMS1117 OPTION DESIGNATOR SUFFIX

Typical Read Access Time	Parity Options	Total Storage Capacity (in Kilobytes)			
		32K	64K	96K	128K
290 ns	Parity + Controller	-32-PC	-34-PC	-36-PC	-38-PC
	Parity Data Only	-32-P	-34-P	-36-P	-38-P
	No Parity	-32	-34	-36	-38
360 ns	Parity + Controller	-42-PC	-44-PC	-46-PC	-48-PC
	Parity Data Only	-42-P	-44-P	-46-P	-48-P
	No Parity	-42	-44	-46	-48
390 ns	Parity + Controller	-52-PC	-54-PC	-56-PC	-58-PC
	Parity Data Only	-52-P	-54-P	-56-P	-58-P
	No Parity	-52	-54	-56	-58

ACCESS AND CYCLE TIMES

Option Designator Suffix	Write		Read		Cycle	
	Typical	Worst Case	Typical	Worst Case	Typical	Worst Case
-3X	105	125	290	315	375	390
-4X	115	135	360	390	480	500
-5X	115	135	390	420	560	585

MMS1117 POWER REQUIREMENTS

Nominal Voltage	Voltage Tolerance		Current Requirements		Input Pins
	Min	Max	Standby—Typ/WC (Amps)	Active—Typ/WC (Amps)	
+5 Vdc	4.75	5.25	2.0/2.5	2.0/2.5	DA2, EA2, FA2
+15 Vdc	15	20	0.15/0.20	0.35/0.70	AV1, AR1, CE1, CU1
-15 Vdc	-7.0	-20	0.015/0.030	0.015/0.030	FB2

MMS1117 BACK PLANE CONNECTOR PIN ASSIGNMENT

Row	A		B		C		D		E		F	
Side	1	2	1	2	1	2	1	2	1	2	1	2
Pin A					[**			+5 V		+5 V		+5 V
Pin B					[**							-15 V
Pin C		Gnd		Gnd	PA	Gnd		Gnd	A12	Gnd		Gnd
Pin D			+588			D15			A17	A15		
Pin E			*SSyn	*PA DE	***V_{DD}	D14			MSyn	A16		
Pin F						D13			A02	C1		
Pin H					D11	D12			A01	A00		
Pin J						D10			SSyn	C0		
Pin K						D09		[**	A14	A13		
Pin L						D08	Init	[**	A11			
Pin M						D07		[**				
Pin N	*P1				DCL0	D04		[**		A08		
Pin P	*P0					D05		[**	A10	A07		
Pin R	***V_{DD}					D01		[**	A09			
Pin S					PB	D00		[**				
Pin T	Gnd		Gnd		Gnd	D03	Gnd	[**	Gnd		Gnd	
Pin U					***V_{DD}	D02			A06	A04		
Pin V	***V_{DD}					D06			A05	A03		

*Options for use with External Parity Controller

**Grant Continuity Jumpers

***V_{DD} is any voltage between +15 Vdc and +20 Vdc on any one of the four listed pins

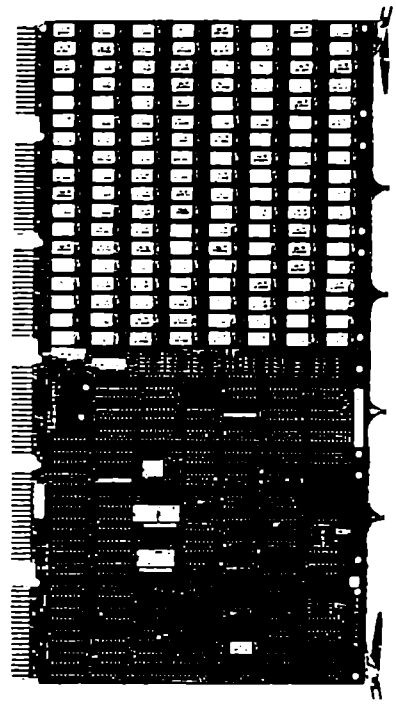
MOTOROLA

MMS1119

Advance Information

PDP-11* MODIFIED UNIBUS*/EXTENDED UNIBUS COMPATIBLE MEMORY SYSTEM

- Uses 16K or 64K Dynamic RAM Chips
- Available in 64K, 96K, 128K, 256K, and 512K Word Capacities
- Read Access Time Typically 300 ns (Measured Inside Buffers)
- Cycle Times as Low as 390 ns Typical
- Two Speed Options Available
- Worst-Case AC Limits Specified at Card Edge
- On-Board Parity and Parity Controller Standard
- Also Available Without Parity
- Starting Address Configurable at Any 4K Boundary
- Optional Selection of I/O Page Size; 2K, 4K, or 8K Words
- Automatic Internal Refresh
- Provisions for External Refresh Control
- Battery Backup Capability Standard
- Single 5-Volt Power Supply Required for 256K and 512K Word Versions



ORDERING INFORMATION

M M S 1 1 1 9 X Y Z_2 Z_1 Z_0

Basic Product Designation

X	Option
P	Parity + Controller
N	No Parity**

Y	Read Access
3	300 ns (Typ)
4	350 ns (Typ)

Z_2	Z_1	Z_0	Capacity
0	6	4	64K Words
0	9	6	96K Words
1	2	8	128K Words
2	5	6	256K Words
5	1	2	512K Words

**Available on special order

NOTE: K = 1024, Word = 16 Bits W/O, 18 Bits With Parity

*PDP-11 and UNIBUS are trademarks of Digital Equipment Corporation

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Limit		Units
		Min	Max	
Supply Voltage (Relative to Ground)	V_{DD}	−0.3	20.0	Vdc
	V_{CC}	−0.3	7.0	
	V_{BB}	−20.0	+0.3	
Input Voltage (Any input relative to Ground)	V_{in}	−0.7	+6.5	Vdc

NOTES: 1. Permanent damage may occur if Absolute Maximum Ratings are exceeded. Functional operation shall be restricted to Recommended Operating Conditions.

2. Permanent damage may also occur if V_{DD} is applied for more than one second while V_{BB} is outside its Recommended Operating Range.

ENVIRONMENTAL RATINGS

Rating	Symbol	Limit	Units
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	−40 to +85	°C
Relative Humidity (Without Condensation)	RH	0 to 90	%

RECOMMENDED DC OPERATION CONDITIONS

Parameter	Symbol	Limit		Units	Note
		Min	Max		
Supply Voltage — Nominal +15 V or nominal +12 V, pin AR1	V_{DD}	14.50	18.50	Vdc	1, 3
		11.40	12.60		
— Nominal +5 V, pins AA2, BA2, CA2	V_{CC}	4.75	5.25		2
— Nominal +5 V BBU, pin BD1	V_{CC}/BBU	4.75	5.25		3
— Nominal −15 V or nominal −12 V, pin AS1	V_{BB}	−7.00	−20.00		3, 4

NOTES: 1. +15 V or +12 V is jumper selectable on all modules populated with 16K RAMs.

2. Pins AA2, BA2, and CA2 are connected together on the MMS1119.

3. These voltages must be present on cards populated with 16K RAMs if Battery Backup is required. Only V_{CC}/BBU need be present for cards populated with 32K or 64K RAMs.

4. V_{DD} and V_{BB} not required for cards populated with 32K or 64K RAMs.

DC OPERATING CHARACTERISTICS ($0°C < T_A < 70°C$)

Characteristic	Capacity (K Words)	Mode	Symbol	Limit			Units	Notes
				Min	Typ	Max		
Supply Current — Nominal +15 V or +12 V Supply	64, 96, 128	Active	IDD	—	0.25	0.50	Adc	1, 2
	64, 96, 128	Standby	IDD	—	0.16	0.30	Adc	1, 2
Supply Current — Nominal +5 V Supply and +5 V BBU	64, 96, 128	Active/Standby	IDD	—	3.30	3.90	Adc	1, 2
Supply Current — Nominal +5 V BBU	64, 96, 128	BBU	ICC	—	1.10	1.30	Adc	1
Supply Current — Nominal +5 V Supply and +5 V BBU	256	Active/Standby	ICC	—	3.30	4.60	Adc	1
Supply Current — Nominal +5 V BBU	256	BBU	ICC	—	1.00	1.50	Adc	1
Supply Current — Nominal +5 V Supply and +5 V BBU	512	Active/Standby	ICC	—	3.80	5.1	Adc	1
Supply Current — Nominal +15 V BBU	512	BBU	ICC	—	1.50	2.00	Adc	1
Supply Current — Nominal −15 V or −12 V Supply	64, 96, 128	All	IBB	—	12	20	mAdc	1, 2
Logic "1" Input Current — Any Input, V_{IH} = 2.4 Vdc	Any	All	I_{IH}	—	15	50	μAdc	3
Logic "0" Input Current — Any Input, V_{IL} = 0.4 Vdc	Any	All	I_{IL}	—	−1.0	−50	μAdc	3
Logic "1" Leakage Current — Any Output, V Bus = 4.0 Vdc	Any	All	V_{OH}	—	20	100	μAdc	3
Logic "0" Output Voltage — Any Output, I_{OL} = 50 mAdc	Any	All	V_{OL}	—	0.40	0.70	Vdc	3
Input Threshold Voltage — Any Input — High Logic State			V_{ILH}	1.80	2.25	2.50	Vdc	
Input Threshold Voltage — Any Input — Low Logic State			V_{IHL}	1.05	1.30	1.55	Vdc	

NOTES 1. Active Mode = Memory accesses at maximum continuous rates; Standby Mode = Internal Refresh Cycles only; Battery Backup (BBU) = Standby Mode with +5 V applied only through Pin BD1.

2. +15/+12 V and −15/−12 V supplies not required for products populated with 64K RAMs.

3. Negative sign = Current out of pin. Min/Max Limits refer to absolute values of current.

AC OPERATING CONDITIONS

Parameter	Symbol	Limit		Unit	Note
		Min	Max		
Address Hold Time – MSYN↓ to A <0:21> Invalid	tAH	25	–	ns	1
Address Setup Time – A <0:21> Valid to MSYN↓	tAS	75	–	ns	1
Processor Handshake Time – SSYN↓ to MSYN↑	tPH	–	0	ns	1, 2
Data Hold Time (Write Cycle/DATO) – MSYN↓ to D <0:15> Invalid	tDHW	40	–	ns	1
Data Setup Time (Write Cycle/DATO) – D <0:15> Valid to MSYN↓	tDSW	15	–	ns	1

NOTES: 1. All timing is referenced at card edge. Operation is assumed to be in a properly terminated backplane, with memory not busy and no refresh arbitration.

2. Assumes handshaking occurs immediately.

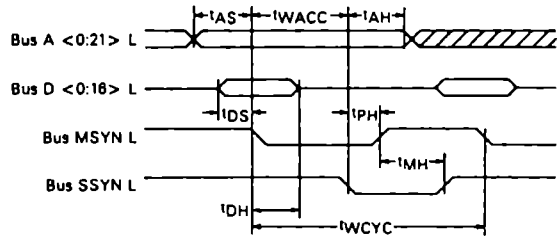
AC OPERATING CHARACTERISTICS ($0°C \leq T_A \leq 70°C$)

Characteristics	Symbol	MMS1119X3XXX			MMS1119X4XXX			Unit	Note
		Min	Typ	Max	Min	Typ	Max		
Cycle Time – Read (DATI) Cycle	tRCYC	390	360	–	440	425	–	ns	1
Read Access Time – MSYN↓ to SSYN↓	tRACC	–	330	360	–	380	430	ns	1
Data Hold Time – Read (DATI) Cycle MSYN↓ to Data Invalid	tDH	70	–	–	70	–	–	ns	1
Data Setup Time – Read (DATI) Cycle D<0:15> Valid to SSYN↓	tDS	0	–	–	0	–	–	ns	1
Memory Handshake Time – Read (DATI) or Write (DATO) Cycle – MSYN↑ to SSYN↓	tMH	–	–	75	–	–	75	ns	1
Write Access Time – MSYN↓ to SSYN↓	tWACC	–	125	166	–	125	165	ns	1
Cycle Time – Write (DATO) Cycle	tWCYC	340	–	–	440	–	–	ns	1

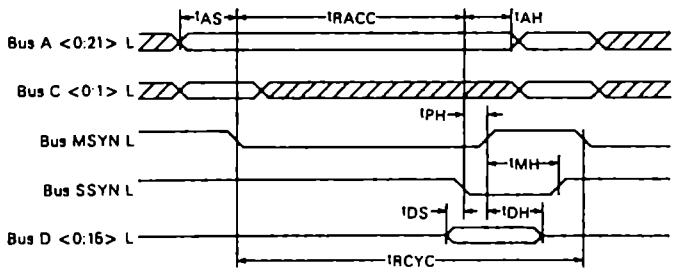
NOTES: 1. All timing is referenced at card edge. Operation is assumed to be in a properly terminated backplane, with memory not busy and no refresh arbitration.

2. Assumes handshaking occurs immediately.

WRITE CYCLE TIMING



READ CYCLE TIMING



TIMING

The MMS1119 is fully compatible with the PDP-11 Modified and Extended UNIBUS protocol and timing. Limits are specified in the AC Conditions/Characteristics Tables in conjunction with the DATI/DATO waveforms.

REFRESH

The storage cells in the MMS1119 are implemented with dynamic MOS RAM's. The charge stored in the cells must be refreshed every 2 milliseconds, requiring a single refresh cycle to be initiated approximately once every 16 M Seconds. The latency induced to bus cycles concurrent with refresh cycles is no greater than the specified minimum cycle time for the MMS1119 version chosen.

The MMS1119 contains circuitry to automatically refresh the memory cells. An option is also provided to allow the User to control the refresh externally. In this case, the Refresh Latency will be no greater than the refresh cycle time defined by the external circuitry. Note that any external refresh circuitry must conform to the requirements previously mentioned, i.e., each cell refreshed at a 2 millisecond rate and a refresh cycle time not less than the minimum Read Cycle time.

AVAILABLE OPTIONS

The MMS1119 features a variety of options, allowing its configuration into a wide range of applications. Several of these options are installed at the factory, with most of these specified by the part number as shown in the "Ordering Information" on Page 1. Others are chosen by the User prior to installation of the product.

MEMORY CAPACITY

The MMS1119 utilizes either 16K or 64K RAM components to allow optional storage capacities of 64K, 96K, 128K, 256K, or 512K Words. As noted on Page 1 (Ordering Information), the last three digits of the full part number identifies the total memory capacity in K Words.

BUS INTERFACE

The MMS1119 is provided with a switch to select the type of Bus to be used. With this switch closed, the interface is to an Extended UNIBUS backplane (22 bit address). The memory operates with a Modified UNIBUS system (18 bit address) with this switch open.

STARTING ADDRESS

The MMS1119 utilizes a set of switches to allow the starting address to be selected at any 4K boundary. This feature is available regardless of the Bus Interface or Memory Capacity option chosen. In cases where the sum of the starting address and the memory capacity exceeds the host machine addressing capability, the capability is automatically reduced. (No wraparound to starting address locations occurs.)

I/O PAGE SIZE

When the MMS1119 is located in high memory, the User may select part of the I/O page as Read/Write memory. This is implemented via three switches, resulting in optional I/O page sizes of 2K, 4K, or 8K words.

PARITY OPTIONS

The MMS1119PXXXX contains parity control circuitry which is fully compatible with the DEC parity module. This circuitry does not degrade access or cycle times, and the Panty Control Status Register (CSR) address can be switch selected to any standard pre-assigned bus address. (772100_8 thru 772136_8 for Modified UNIBUS, 17721008 thru 17721368 for Extended UNIBUS. In any case, the CSR occupies a single two-byte address space). The on-board parity circuitry does not impose any additional bus loading on the system.

The MMS1119PXXXX can also be used in systems which utilize the DEC Parity Module. The User selects this mode of operation by opening a switch (provided on the MMS1119P) prior to installation of the memory. The parity generation and detection circuitry of the MMS1119P is fully compatible with the DEC Parity Module.

The MMS1119NXXXX version is available for those systems not requiring parity. This product is supplied as a 16-bit word memory with the Internal/External Parity Control switch open (External).

I/O SIGNAL DESCRIPTION

Signal	Type	Description
A<0:21>	Input	Address lines to select memory locations. A0 selects byte in DATOB
D<0:15>	Bidir.	Data lines used to communicate with Master
C<0:1>	Input	Control lines to specify type of cycle
MSYN	Input	Timing control from Master. Used to start cycle
SSYN	Output	Timing control used to notify Master that cycle is complete
INIT	Input	System Reset
DCLO	Input	Power monitoring
PB	Output	Signal to Master that parity error has occurred
P<0:1>	Bidir.	Data Parity Bits
PAR DET	Input	Indicates external parity module is in use
INT SSYN	Output	Slave Sync used with external parity module only

NOTE: All signals are low assertion level.

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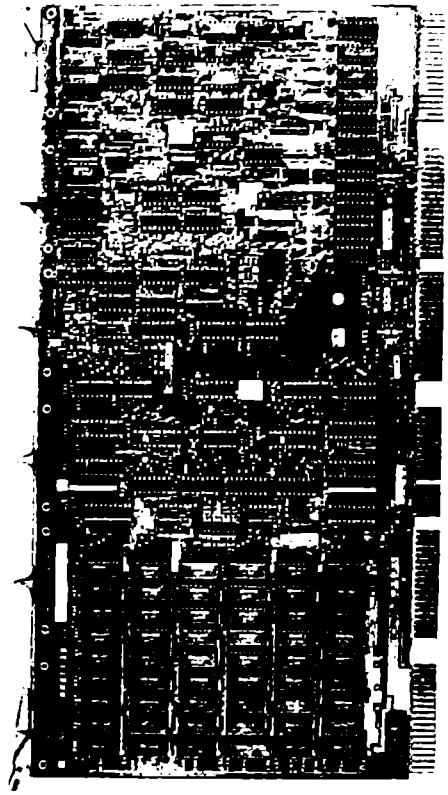
MMS1128

Advance Information

PDP-11 MODIFIED UNIBUS COMPATIBLE MEMORY SYSTEM

- Uses 16K, 32K, or 64K Dynamic RAM Chips
- Available in 32K, 48K, 64K, 96K, and 128K Word Capacities
- Read Access Time Typically 300 ns (Measured Inside Buffers)
- Cycle Times as Low as 460 ns Typical
- Two Speed Options Available
- Worst-Case AC Limits Specified at Card Edge
- On-Board Parity and Parity Controller Standard
- Also Available Without Parity
- Starting Address Configurable at any 4K Boundary
- Automatic Internal Refresh
- Provisions for External Refresh Control
- Battery Backup Capability Standard
- Single 5-Volt Power Supply Required for 64K, 96K, 128K, Word Versions



ORDERING INFORMATION

M M S 1 1 2 8 X Y Z_2 Z_1 Z_0

Basic Product Designation

X	Option
P	Parity + Controller
N	No Parity**

Y	Read Access
3	300 ns (typ)
4	350 ns (typ)

Z_2	Z_1	Z_0	Capacity
0	3	2	32 K Words
0	4	8	48 K Words
0	6	4	64 K Words
0	9	6	96 K Words
1	2	8	128 K Words

**Available on special order

NOTE: K = 1024, Word = 16 Bits W/O, 18 Bits With Parity

I/O SIGNAL DESCRIPTION

Signal	Type	Description
A <0:17>	Input	Address lines to select memory locations. A0 selects byte in DATOB
D <0:15>	Bidirectional	Data lines used to communicate with Master
C <0:1>	Input	Control lines to specify type of cycle
MSYN	Input	Timing control from Master. Used to start cycle
SSYN	Output	Timing control used to notify Master that cycle is complete
INIT	Input	System Reset
DCLO	Input	Power monitoring
PB	Output	Signal to Master that parity error has occurred
P <0:1>	Bidirectional	Data Parity Bits
PAR DET	Input	Indicates extend parity module in use
INT SSYN	Output	Slave Sync used with external parity module only

NOTE: All signals are low assertion level.

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Limit		Units
		Min	Max	
Supply Voltage (Relative to Ground)	V_{DD}	−0.3	20.0	Vdc
	V_{CC}	−0.3	7.0	
	V_{BB}	−20.0	0.3	
Input Voltage (Any input relative to GND)	V_{in}	−0.7	5.5	Vdc

NOTES: 1. Permanent damage may occur if Absolute Maximum Ratings are exceeded. Functional operation shall be restricted to Recommended Operating Conditions.

2. Permanent damage may also occur if V_{DD} is applied for more than one second while V_{BB} is outside its Recommended Operating Range.

ENVIRONMENTAL RATINGS

Rating	Symbol	Limit	Units
Operating Temperature	T_A	0 to 55	°C
Storage Temperature	T_{stg}	−40 to +85	°C
Relative Humidity (Without Condensation)	RH	0 to 90	%

RECOMMENDED DC OPERATION CONDITIONS

Parameter	Symbol	Limit		Units	Note
		Min	Max		
Supply Voltage − Nominal + 15 V or nominal + 12 V, pin AR1	V_{DD}	14.50 11.40	16.50 12.60	Vdc	1, 3
− Nominal +5 V, pins AA2, BA2, CA2	V_{CC}	4.75	5.25		2
− Nominal +5 V BBU, pin BD1	V_{CC}/BBU	4.75	5.25		3
− Nominal − 15 V or nominal − 12 V, pin AS1	V_{BB}	−7.00	−20.00		3, 4

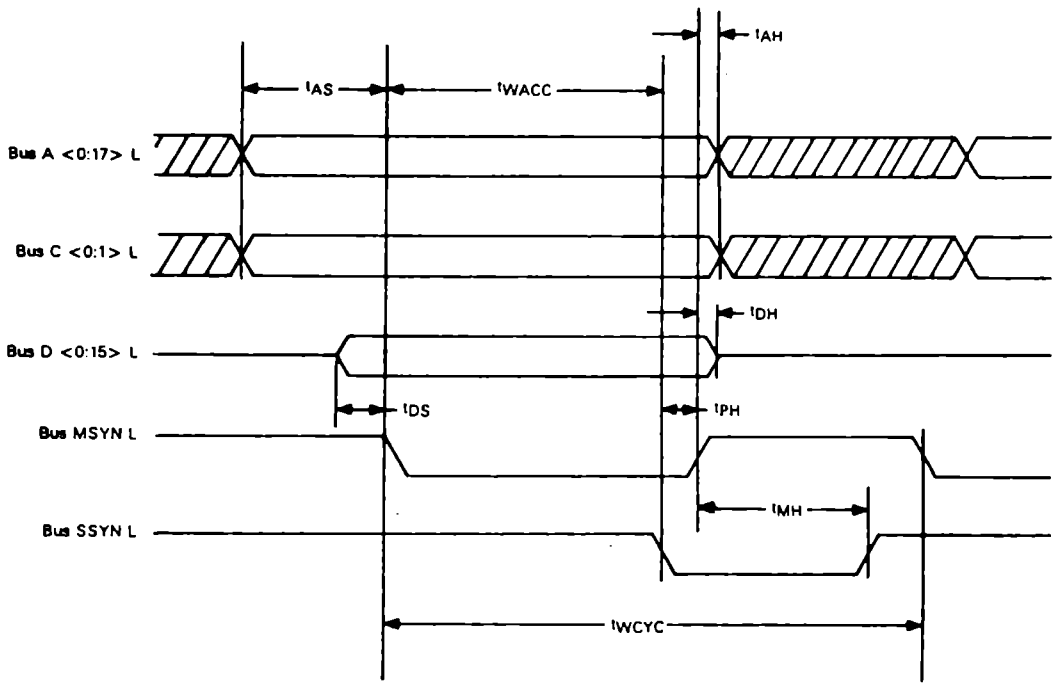
NOTES: 1. + 15 V or + 12 V is jumper selectable on all modules populated with 16K RAMs.

2. Pins AA2, BA2, and CA2 are connected together on the MMS1128.

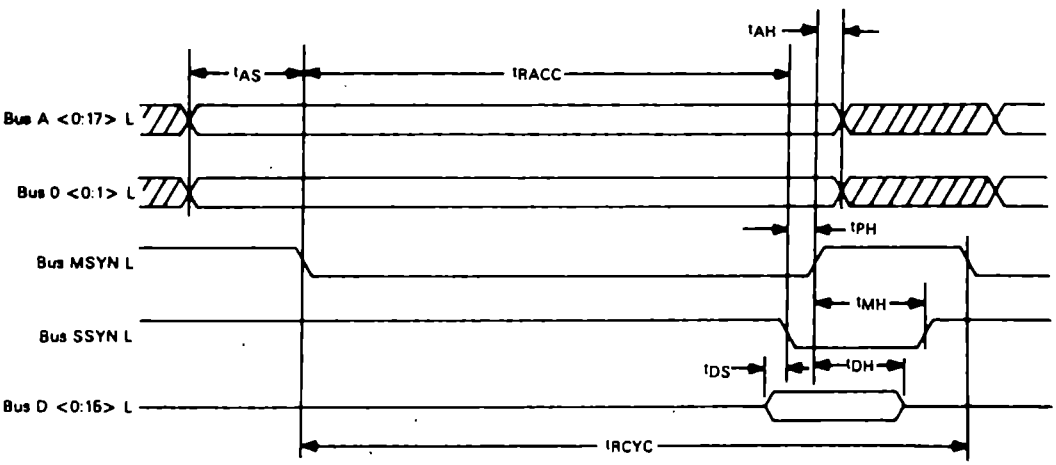
3. These voltages must be present on cards populated with 16K RAMs if Battery Back Up is required. Only V_{CC}/BBU need be present for cards populated with 32K or 64K RAMs.

4. V_{DD} and V_{BB} not required for cards populated with 32K or 64K RAMs.

WRITE CYCLE TIMING (DATO)



READ CYCLE TIMING (DATI)



DC OPERATING CHARACTERISTICS ($0° < T_A < 55°C$)

Characteristic	Capacity (K Words)	Mode	Symbol	Limit Min	Limit Typ	Limit Max	Units	Notes
Supply Current								
– Nominal +15 V or +12 V Supply BBU	32, 48	Active	I_{DD}		0.25	0.50	Adc	1, 2
	32, 48	Standby	I_{DD}		0.16	0.30		
– Nominal +5 V Supply	32, 48	Act/Stby	I_{CC}		1.20	1.50	Adc	1
– Nominal +5 V BBU	32, 48	BBU	I_{CC}		0.56	0.80	Adc	1
– Nominal +5 V Supply	64, 96, 128	Act/Stby	I_{CC}		1.60	2.25	Adc	1
– Nominal +5 V BBU	64, 96, 128	BBU	I_{CC}		0.80	1.15	Adc	1
– Nominal –15 V or –12 V Supply BBU	32, 48	All	I_{BB}		12	20	mAdc	1, 2
Logic "1" Input Current – Any Input, $V_{IH} = 4.0$ Vdc			I_{IH}		15	50	μAdc	3
Logic "0" Input Current – Any Input, $V_{IL} = 0.4$ Vdc			I_{IL}			–1.6	mAdc	3
Logic "1" Output Current – Any Output, V Bus = 4.0 Vdc			V_{OH}		20	100	μAdc	3
Logic "0" Output Voltage – Any Output, $I_{OL} = 50$ mAdc			V_{OL}		0.4	0.70	Vdc	3
Input Threshold Voltage – Any Input – High Logic State			V_{ILH}	1.80	2.25	2.50	Vdc	
Input Threshold Voltage – Any Input – Low Logic State			V_{IHL}	1.05	1.30	1.55	Vdc	

NOTES: 1. Active Mode = Memory accesses at maximum continuous rates. Standby Mode = Internal Refresh Cycles only. Battery Back Up (BBU) = Standby Mode with +5 V applied only through Pin BD1

2. +15 V/+12 V and –15 V/–12 V supplies not required for products populated with 64K RAMs

3. Negative Sign = Current out of pin. Min/Max Limits refer to absolute values of current

AC OPERATING CONDITIONS

Parameter	Symbol	Limit Min	Limit Max	Unit	Note
Address Hold Time – MSYN to A<0:17> Invalid	t_{AH}	50		ns	1
Address Setup Time – A <0:17> Valid to MSYN	t_{AS}	75		ns	1
Processor Handshake Time – SSYN to MSYN	t_{PH}		0	ns	1, 2
Data Hold Time (Write Cycle/DATO) – MSYN to D <0:15> Invalid	t_{DHW}	40		ns	1
Data Setup Time (Write Cycle/DATO) – <0:15> Valid to MSYN	t_{DSW}	15		ns	1

NOTES: 1. All timing is referenced at card edge. Operation is assumed to be in a properly terminated backplane, with memory not busy and no refresh arbitration.

2. Assumes handshaking occurs immediately.

AC OPERATING CHARACTERISTICS ($0°C < T_A < 70°C$)

Characteristics	Symbol	MMS1128X3XXX Min	MMS1128X3XXX Typ	MMS1128X3XXX Max	MMS1128X4XXX Min	MMS1128X4XXX Typ	MMS1128X4XXX Max	Unit	Note
Cycle Time – Read (DATI) Cycle	t_{RCYC}		460	515		510	565	ns	1
Read Access Time – MSYN to SSYN	t_{RACC}		330	380		380	430	ns	1
Data Hold Time – Read (DATI) Cycle MSYN to Data Invalid	t_{DH}			70			70	ns	1
Data Setup Time – Read (DATI) Cycle D <0:15> Valid to SSYN	t_{DS}	0			0			ns	2
Memory Handshake Time – Read (DATI) or Write (DATO) Cycle – MSYN to SSYN	t_{MH}	25		75	25		75	ns	1
Write Access Time – MSYN to SSYN	t_{WACC}		125	165		125	165	ns	1
Cycle Time – Write (DATO) Cycle	t_{WCYC}		325	340		425	440	ns	1

NOTES: 1. All timing is referenced at card edge. Operation is assumed to be in a properly terminated backplane, with memory not busy and no refresh arbitration.

2. Timing is referenced inside Bus Drivers

TIMING

The MMS1128 is fully compatible with the PDP-11 Modified UNIBUS protocol and timing. Limits are specified in the A.C. Conditions/Characteristics Tables in conjunction with the DATI/DATO waveforms.

REFRESH

The storage cells in the MMS1128 are implemented with dynamic MOS RAM's. The charge stored in the cells must be refreshed every 2 milliseconds, requiring a single refresh cycle to be initiated approximately once every 16 milliseconds. The latency induced to bus cycles concurred with refresh cycles is no greater than the specified minimum cycle time for the MMS1128 version chosen.

The MMS1128 contains circuitry to automatically refresh the memory cells. An option is also provided to allow the User to control the refresh externally. In this case, the Refresh Latency will be no greater than the refresh cycle time defined by the external circuitry. Note that any external refresh circuitry must conform to the requirements previously mentioned, i.e., each cell refreshed at a 2 millisecond rate and a refresh cycle time not less than the minimum Read Cycle time.

AVAILABLE OPTIONS

The MMS1128 features a variety of options, allowing its configuration into a wide range of applications. Several of these options are installed at the factory, with most of these specified by the part number as shown in the "Ordering Information" on Page 1. Others are chosen by the User prior to installation of the product.

MEMORY CAPACITY

The MMS1128 utilizes 16K, 32K, or 64K RAM components to allow optional storage capacities of 32K, 48K, 64K, 96K, or 128K Words. As noted on Page 1 (Ordering Information), the last three digits of the full part number identifies the total memory capacity in K Words.

STARTING ADDRESS

The MMS1128 utilizes a set of switches to allow the starting address to be selected at any 4K boundary. This feature is available regardless of the Memory Capacity option chosen. In cases where the sum of the starting address and the memory capacity exceeds the host machine addressing capability, the capability is automatically reduced. (No wraparound to starting address location occurs.)

I/O PAGE SIZE

When the MMS2118 is located in high memory, the User may select part of the I/O page as Read/Write memory. This is implemented via three switches, resulting in optional I/O page sizes of 2K, 4K, or 8K words.

PARITY OPTIONS

The MMS2118PXXXX contains parity control circuitry which is fully compatible with the DEC parity module. This circuitry does not degrade access or cycle times, and the Parity Control Status Register (CSR) address can be switch selected to any standard pre-assigned bus address. (772100_8 through 772136_8.) In any case, the CSR occupies a single two-byte address space. The on-board parity circuitry does not impose any additional bus loading on the system.

The MMS1128PXXXX can also be used in systems which utilize the DEC Parity Module. The User selects this mode of operation by inserting a jumper prior to installation of the memory. The parity generation and detection circuitry of the MMS1128P is fully compatible with the DEC Parity Module.

The MMS1128PXXXX version is available for those systems not requiring parity. This product is supplied as a 16-bit word memory with the Internal/External Parity Control switch open (External).

MOTOROLA

MMS1170

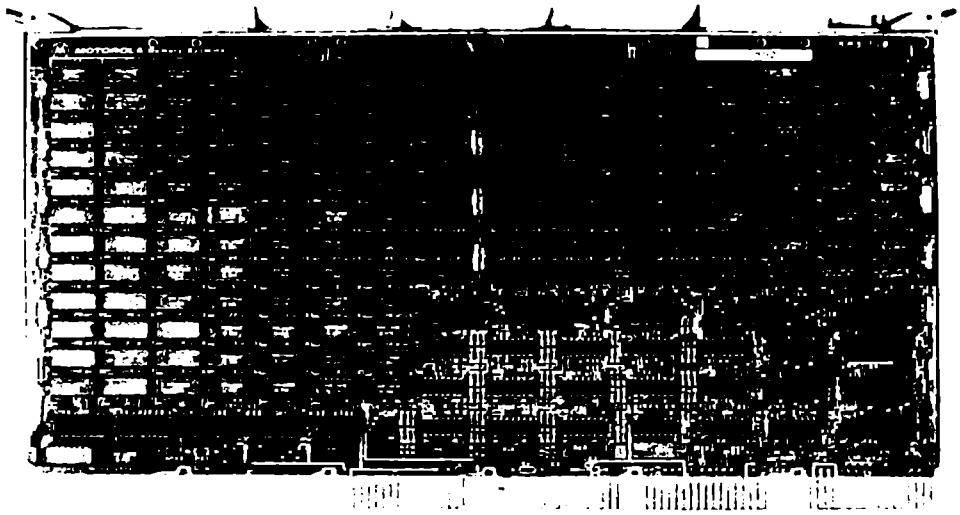
Product Preview

MEMORY ARRAY CARD FOR PDP*-11/70

The MMS1170 is a dynamic memory array system specifically designed for use in PDP-11/70 minicomputers from Digital Equipment Corporation. The array has a capacity of 64K double words (256K bytes) using 16K RAM chips. It is hardware and software compatible with the PDP-11/70 memory controller module and DEC diagnostics.

The MMS1170 is designed to occupy a single hex slot of the DEC MK-11 Memory System chassis. It features an On Line/Off Line switch (with an LED indicator) to facilitate trouble-shooting. A separate LED indicates when battery backup voltage is available via the backplane connector.

All RAMs used on the MMS1170 are socketed. Two spare 16K x 1 RAMs are provided on the board. The product is fully burned-in and covered by the Motorola Memory System One-Year Limited Warranty.



ORDERING INFORMATION

MMS1170 E 1 064

Basic Part No	ECC	Speed Option	Size (64 x 1024 Double Words)

NOTE: Double Word = 32 Data and 7 ECC Bits

*PDP is a trademark of Digital Equipment Corporation

ENVIRONMENTAL RATINGS

Rating	Symbol	Limit	Units
Operating Temperature	T_A	0 to + 50	°C
Storage Temperature	T_{stg}	- 40 to + 80	°C
Relative Humidity (Without Condensation)	RH	0 to 90	%

PHYSICAL DIMENSIONS

Dimension	Millimeters	Inches
Width	39 85	15 688
Height	22 225	8 75
PC Board Thickness	0 142	0 056
Clearance Required (Component Side)*	0 952	0.375
Clearance Required (Solder Side)*	0.254	0 10

*Measured from surface of PC Board.

POWER REQUIREMENTS

Input Voltage	Maximum Current Requirements			Units
	Operating	Standby	Battery Backup	
+ 12 B	1.5	0.25	0.25	Adc
+ 5 V	0.4	0.35	0	Adc
- 12 B	0.04	0.02	0.02	Adc
+ 5 V B	0.9	0.8	0.8	Adc

AC OPERATING CHARACTERISTICS

Characteristic	Nominal**	Units
Cycle Time – Read Write	650 680	ns
Access Time – Read Write	320 70	ns

**The actual response times are determined by DEC MK-11 Memory System Controller design Nominal values shown are for reference only.

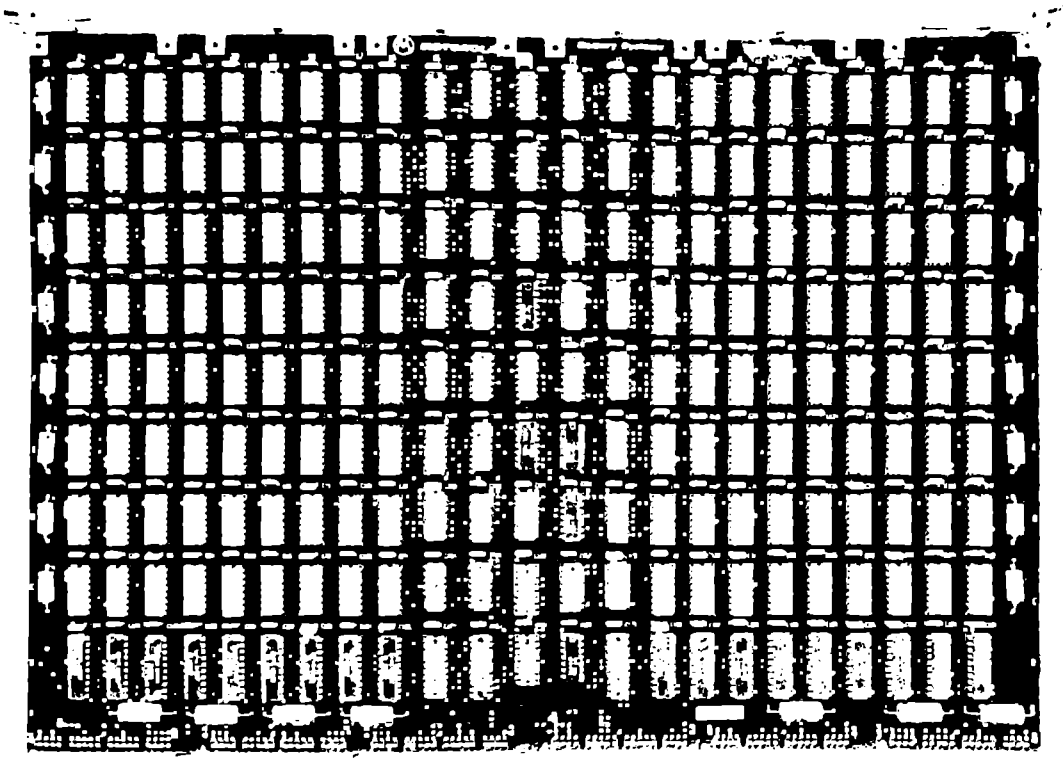
MOTOROLA

MMS780

Advance Information

MEMORY ARRAY CARD FOR VAX-11/780*

The MMS780 is a dynamic memory array system specifically designed for use in VAX-11/780 minicomputers from Digital Equipment Corporation. The array has a capacity of 32K words (256K Bytes) using 16K RAM chips. It is fully compatible with the VAX-11/780 memory controller module.



ORDERING INFORMATION

MMS780AE1032

- Basic Part No.
- ECC
- Speed Option
- Size (K Words)

Note. K = 1024
Word = 64 Data + 8 ECC Bits

*VAX is a trademark of Digital Equipment Corporation.

ENVIRONMENTAL RATINGS

Rating	Symbol	Limit	Units
Operating Temperature	T_A	0 to +55	°C
Storage Temperature	T_{stg}	−40 to +80	°C
Relative Humidity (Without Condensation)	RH	0 to 90	%

PHYSICAL DIMENSIONS

Dimension	Millimeters	Inches
Width	39.85	15.688
Height	30.48	12.0
PC Board Thickness	0.142	0.056
Clearance Required (Component Side)*	0.952	0.375
Clearance Required (Solder Side)*	0.254	0.10

*Measured from surface of PC Board

POWER REQUIREMENTS

Input Voltage	Maximum Current Requirements			Units
	Operating	Standby	Battery Backup	
+12 V	1.5	0.25	0.25	Adc
+5 V	0.7	0.6	0	Adc
−5 V	0.04	0.02	0.02	Adc
+5 V Battery	0.9	0.8	0.8	Adc

AC OPERATING CHARACTERISTICS

Characteristic	Nominal**	Units
Cycle Time – Read, Refresh, or Init. – Read/Modify/Write	530 1100	ns
Access Time – Read – Write	250 750	ns

**The actual response times are determined by VAX-11/780 Memory Subsystem Controller design. Nominal values shown are for reference only

OPERATING PRINCIPLES

The MSM780 is based on 16K x 1 dynamic RAMs arranged in two banks, each containing 72 chips. The 72-bit word thus formed is subdivided into two 32-bit long words (Upper and Lower) and eight ECC bits. All memory array accesses correspond to a Read from, or write to, the selected 72-bit word. (All 8, 16, and 32 bit memory operations are transformed into 72 bit accesses by the memory controller.)

The memory array selection is accomplished via address lines (ADR19:ADR16) and four select signals at the Memory Subsystem Backplane. This Backplane has 16 slots dedicated for memory array cards, with the select signals uniquely specified for each slot. This arrangement eliminates the need for special jumpers and address switches. The MMS780 is merely inserted in the next available backplane slot. A total of 4 Megabytes of memory can be accomodated by one Memory Subsystem.

USAGE RECOMMENDATIONS

The MMS780 is recommended for use with any VAX-11/780 memory subsystem set up for operation with the DEC M8210 array card. It is hardware and software compatible with the VAX-11/780, including DEC diagnostics which allow failure isolation at the chip level. The MMS780 is also compatible with DEC battery backup provisions.

INTERFACE

The VAX-11/780 computer system is normally configured with either one or two memory subsystems, as shown in Figure 1. The normal interface signals utilized within each subsystem are depicted in Figure 2. The MMS780 Array Module functions in any slot of either subsystem, with no modifications required.

FIGURE 1 – NORMAL VAX-11/780 MEMORY CONFIGURATION

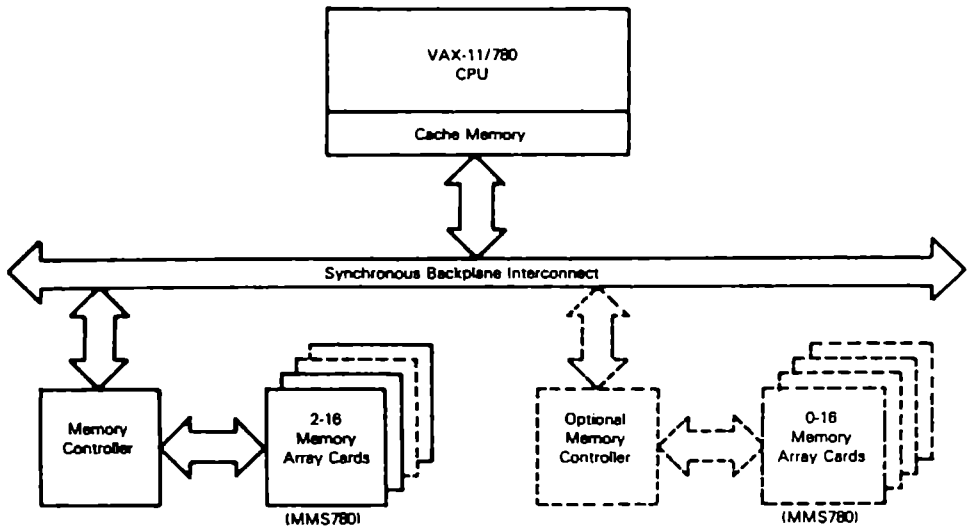
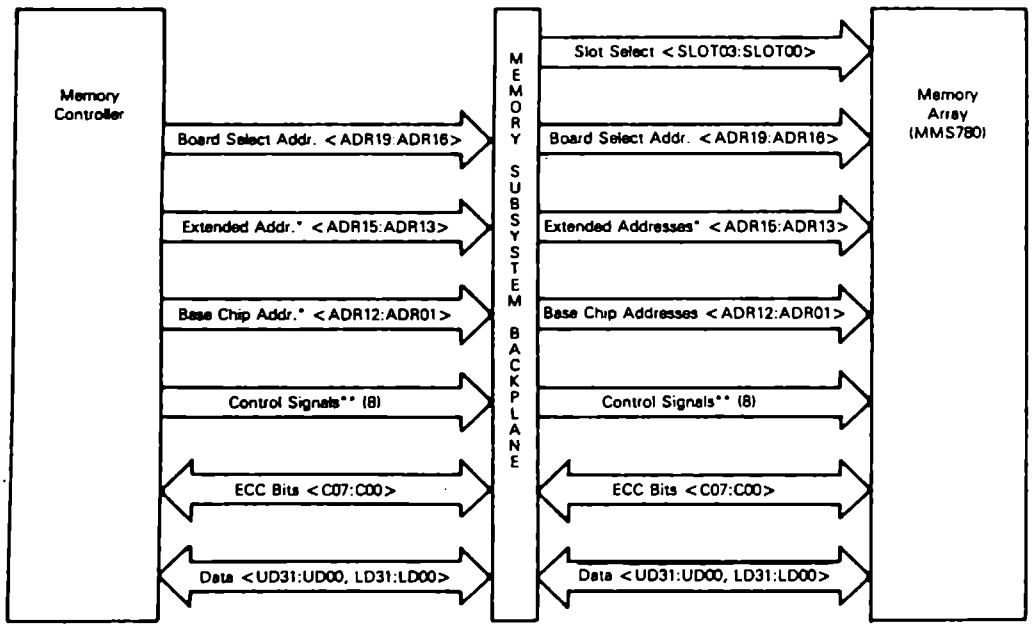


FIGURE 2 – MEMORY SUBSYSTEM INTERFACE



*Extended Addresses are labeled ADR13, ADRCS, and ADREXT. During normal operation, they correspond to >ADR15:ADR13<.
**Control signals are: Read, Column Address Strobe (CAS), Row Address Strobe (RAS), Multiplexer Control, Refresh Cycle, Bus Select, Bus Output Enable, and Initiate.

MOTOROLA

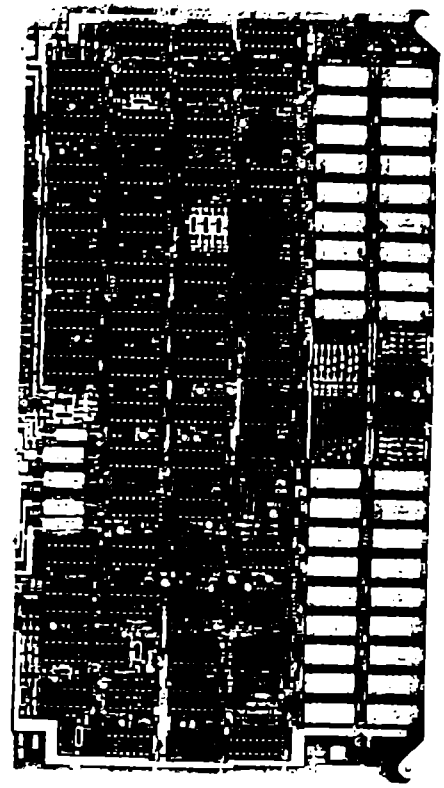
MMS8064(P)
MMS8048(P)
MMS8032(P)
MMS8016(P)

Advance Information

SBC-COMPATIBLE MEMORY SYSTEMS

The MMS80XX family of memory systems is designed for use with the Intel SBC 80 Series computers, System 80 microcomputers, MDS systems, and the 16-bit SBC 86/12. The modules employ 16K dynamic RAM's mounted on a single 6 3/4" X 12" PC board along with timing, control, and bus interface logic. Eight models are available, all having the same access and cycle times. All electrical connections are made via two edge connectors.

- Pin, Function, and Form-Factor Compatible with MULTIBUS* Systems
- Even/Odd Bank Address Allows 16-Bit or 8-Bit Operation
- Addresses Selectable in Independent 8K Blocks
- 20 Address Lines — Operates in 1M Byte System
- Handles Early or Late Inhibits
- Operates in Delayed Write, Advance Write, and Read Modes
- Battery Backup Capability through use of Memory Protect Signal on P2 Connector
- On-Board Refresh Control Circuitry
- Programmable Advanced Acknowledge (AACK/) Signal
- On-board V_{BB} Generation (-5 V) Allows Operation from 12 V, +5 V, and -12 V, -10 V, or -5 V Supplies
- Cycle Times of 700 ns (Read, Delayed, Write) and 1240 ns (Advanced Write)
- Available in 16K, 32K, 48K, and 64K Byte Configurations



ORDERING INFORMATION

No Parity	Parity	Capacity
MMS8064	MMS8064P	64K Bytes
MMS8048	MMS8048P	48K Bytes
MMS8032	MMS8032P	32K Bytes
MMS8016	MMS8016P	16K Bytes

PHYSICAL CHARACTERISTICS

Characteristic	Limit
Width	30 48 cm (12 00 inches)
Depth	17 15 cm (6 75 inches)
Thickness	1 27 cm (0 50 inches)
Weight	397 grams (14 0 ounces)

*Trademark of Intel, Inc

AC OPERATING CONDITIONS

Parameter		Symbol	Limit Min	Limit Max	Units	Notes
Cycle Time	Read or Delayed Write Cycle Advanced Write Cycle	tCYC tCYC(A)	700 1240		ns	1, 2 1, 2, 3
Address Setup Time	Address Valid to MRDC/↓ or MWRC/↓	tAS	50		ns	
Address Hold Time	MRDC/↑ or MWRC/↑ to Address Invalid	tAH	0		ns	
Write Data Setup Time (Delayed Write)	Data Valid to MWRC/↓	tDSW	-100		ns	
Write Data Delay Time (Advanced Write)	MWRC/↑ to Data Invalid	tDDAW		500	ns	3
Write Data Hold Time		tDHW	0		ns	
Inhibit Setup Time INH1/ Valid to MRDC/↓ or MWRC/↓	Early Inhibit Late Inhibit Option Installed	tIS1 tIS2	10 -50		ns	
Inhibit Hold Time	MRDC/↑ or MWRC/↑ to INH1 Invalid	tIH	100		ns	
Byte High Enable Setup Time	BHEN/ Valid to MRDC/↓ or MWRC/↓	tBS	50		ns	
Byte High Enable Hold Time	MRDC/↑ or MWRC/↑ to BHEN/ Invalid	tBH	0		ns	
Memory Protect Setup Time	MPRO/↓ to VCC < 4 75 Vdc	tMPS	15		μs	
Memory Protect Hold Time	VCC ≥ 4 75 Vdc to MPRO/↑	tMPH	0		ns	
Refresh Interval		tRI	12 7	15 6	ms	

NOTES 1) Add Refresh Delay Time (TRD) to these parameters when Asynchronous Refresh occurs
2) Add 40 ns (Typ), 50 ns (Max) to these parameters if Late Inhibit Option is installed
3) Applicable only if Advanced Write Cycle option is installed

AC OPERATING CHARACTERISTICS ($0°C \leq T_A \leq 55°C$)

Parameter		Symbol	Limit Min	Limit Typ	Limit Max	Units	Notes
Read Access Time	MRDC/↓ to Data Valid	tACC		400	450	ns	1, 3
Read Data Setup Time	Read Data Valid to XACK/↓	tDSR	0			ns	
Read Data Hold Time	XACK/↑ to Data Invalid	tDHR	0		65	ns	
Advance Acknowledge Delay Time	MRDC/↓ or MWTC/↓ to AACK/↓	tAAK	—	—	—	ns	1, 4, 5
Transfer Acknowledge Delay Time	MRDC/↓ or MWTC/↓ to XACK/↓	tACK			50	ns	1, 2
Acknowledge Turn-Off Time	MRDC/↑ or MWTC/↑ to AACK/↑ or XACK/↑	tTO	15		65	ns	
Parity Error Setup Time	PAR ERR/ Valid to XACK/↓	tPS	0			ns	
Parity Error Hold Time	XACK/↑ to PAR ERR/ Invalid	tPH	50			ns	
Refresh Delay Time		tDR			550	ns	

NOTES: 1) Add 40 ns (Typ), 50 ns (Max) to these parameters if Late Inhibit option is installed.
2) Add 450 ns (Typ), 500 ns (Max) to these parameters for Advanced Write Cycle operations.
3) Add Refresh Delay Time (tRD) to these parameters when Asynchronous Refresh occurs.
4) See Advance Acknowledge options table for Delay Time
5) Advance Acknowledge is delayed until Transfer Acknowledge Time if Asynchronous Refresh occurs

ADVANCE ACKNOWLEDGE OPTIONS

The MMS8060 Series can be programmed to provide an ADV ACK Delay (tAAK) of 100 to 450 ns. Available options are as noted in table at right. Selection is made via installation of a single jumper between two terminals of a 16-pin DIP socket. (Jumper between pins 8 & 9 – 100 ns Typ, between 1 & 16 – 150 ns, etc.)

Limit	Option Selected 8-9	1-16	7-10	2-15	3-14	5-12	4-13	6-11	Units
Min	70	120	165	215	260	310	360	400	ns
Typ	100	150	200	250	300	350	400	450	ns
Max	125	175	230	285	335	400	450	500	ns

ABSOLUTE MAXIMUM RATINGS

Rating		Limit			
		Symbol	Min	Max	Units
Power Supply Voltage (Measured at Connector P1 or P2 With Respect to GND).	Nominal +5 Vdc	V_{CC}	-0.3	+7.0	Vdc
	Nominal +12 Vdc	V_{DD}	-0.3	+15.0	Vdc
	Nominal -5 Vdc (Negative voltage regulator disabled)	V_{BB}	+0.3	-7.0	Vdc
	Nominal -10 Vdc or -12 Vdc (Negative voltage regulator enabled)		+0.3	-15.0	Vdc
Input Voltage, Any Input (Measured at P1 or P2 Conn. With Respect to GND)		V_{IN}	-0.3	+5.5	Vdc

NOTES 1) Permanent damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to Recommended Operating Conditions.

2) Permanent damage may also occur if V_{DD} is applied for more than one second while V_{BB} is outside its Recommended Operating Range.

ENVIRONMENTAL RATINGS

Rating	Limit			
	Symbol	Min	Max	Unit
Operating Temperature	T_A	0	+55	°C
Storage Temperature	T_{stg}	-40	+85	°C
Relative Humidity (Without Condensation)	R.H.	0	90	%

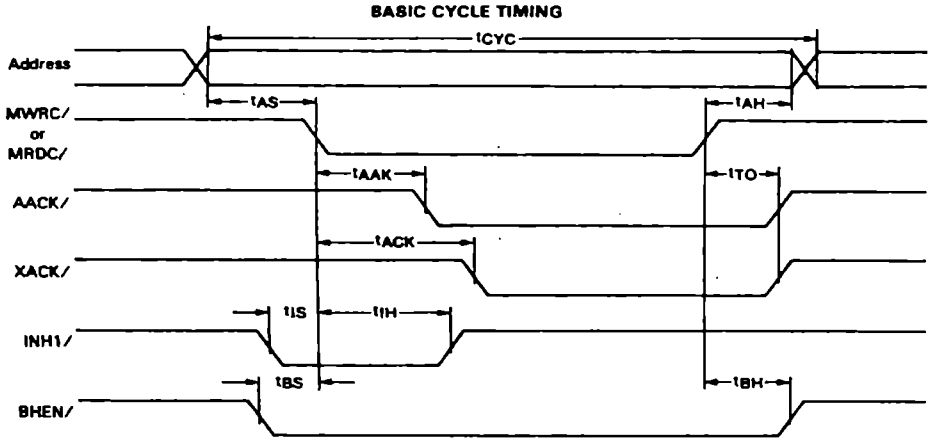
RECOMMENDED DC OPERATING CONDITIONS

Condition		Limit			
		Symbol	Min	Max	Units
Supply Voltage	Nominal +5 Vdc	V_{CC}	4.75	5.25	Vdc
	Nominal +12 Vdc	V_{DD}	11.4	12.6	Vdc
	Nominal -5 Vdc (Negative voltage regulator disabled)	V_{BB}	-4.75	-5.25	Vdc
	Nominal -10 Vdc or -12 Vdc (Negative voltage regulator enabled)		-9.5	-12.6	
Logic Zero Input Voltage, Any Input		V_{IL}	-0.3	+0.8	Vdc
Logic One, Input Voltage, Any Input		V_{IH}	+2.0	+5.25	Vdc

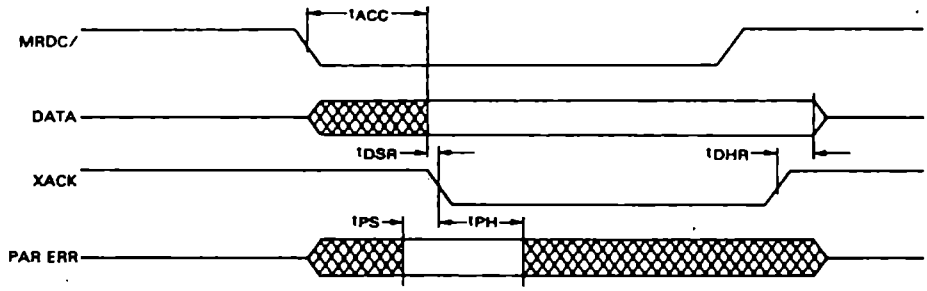
DC OPERATING CHARACTERISTICS ($0°C \leq T_A \leq 55°C$)

Parameter		Symbol	Limit			Units
			Min	Typ	Max	
Supply Current (Normal Mode)	Nominal +5 Vdc	I_{CC}			3.0	Adc
	Nominal +12 Vdc	I_{DD}			260	mAdc
	Nominal -5 Vdc (Negative voltage regulator disabled)	I_{BB}			14	mAdc
	Nominal -10 Vdc or -12 Vdc (Negative voltage regulator enabled)				30	mAdc
Supply Current (Battery Backup Mode)	Nominal +5 Vdc	I_{CC}			1.1	Adc
	Nominal +12 Vdc	I_{DD}			90	mAdc
	Nominal -5 Vdc (Negative voltage regulator disabled)	I_{BB}			7.2	mAdc
	Nominal -10 Vdc or -12 Vdc (Negative voltage regulator enabled)				14	mAdc
Logic One Input Current (V_{CC} = 4.75 Vdc, V_{IH} = 2.4 Vdc	DATO/-DATF/	I_{IH}			250	µAdc
	All Other Inputs				40	µAdc
Logic Zero Input Current (V_{CC} = 5.25 Vdc, V_{IL} = 0.4 Vdc)	DATO/-DATF/	I_{IL}			-600	µAdc
	All Other Inputs				-400	µAdc
Logic One Output Voltage (V_{CC} = 4.75 Vdc, I_{OH} = -5 mAdc)	All Outputs	V_{OH}	2.4			Vdc
Logic Zero Output Voltage (V_{CC} = 4.75 Vdc, I_{OL} = 48 mAdc)	All Outputs	V_{OL}			0.5	Vdc

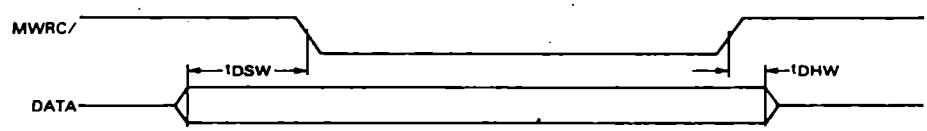
BASIC CYCLE TIMING



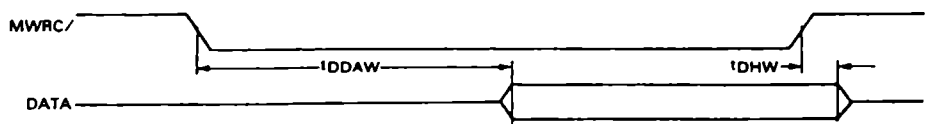
READ CYCLE TIMING



DELAYED WRITE CYCLE TIMING



ADVANCED WRITE CYCLE TIMING



P1 CONNECTOR PIN ASSIGNMENTS

Signal Name	Symbol	Pin No.	Signal Name	Symbol	Pin No.	Signal Name	Symbol	Pin No.
Ground	V_{SS}	1, 2	Address Line 0	ADR0/	57	Memory Read		
Ground	V_{SS}	11, 12	Address Line 1	ADR1/	58	Command	MRDC/	19
Ground	V_{SS}	75, 76	Address Line 2	ADR2/	55	Memory Write	MWTC/	20
Ground	V_{SS}	85, 86	Address Line 3	ADR3/	56	Command		
+12 V Supply	V_{DD}	7, 8	Address Line 4	ADR4/	53	Data Line 0	DAT0/	73
+5 V Supply	V_{CC}	3, 4	Address Line 5	ADR5/	54	Data Line 1	DAT1/	74
+5 V Supply	V_{CC}	5, 6,	Address Line 6	ADR6/	51	Data Line 2	DAT2/	71
+5 V Supply	V_{CC}	81, 82	Address Line 7	ADR7/	52	Data Line 3	DAT3/	72
+5 V Supply	V_{CC}	83, 84	Address Line 8	ADR8/	49	Data Line 4	DAT4/	69
-5 V Supply	V_{BB}	9, 10	Address Line 9	ADR9/	50	Data Line 5	DAT5/	70
-10 V Supply	V_{BB1}	77, 78	Address Line A	ADRA/	47	Data Line 6	DAT6/	67
-12 V Supply	V_{BB2}	79, 80	Address Line B	ADRB/	48	Data Line 7	DAT7/	68
Transfer	XACK/	23	Address Line C	ADRC/	45	Data Line 8	DAT8/	65
Acknowledge			Address Line D	ADRD/	46	Data Line 9	DAT9/	66
Advance	AACK/	25	Address Line E	ADRE/	43	Data Line A	DATA/	63
Acknowledge			Address Line F	ADRF/	44	Data Line B	DATB/	64
Command	INH1/	24	Address Line 10	ADR10/	28	Data Line C	DATC/	61
Inhibit			Address Line 11	ADR11/	30	Data Line D	DATD/	62
Byte High	BHEN/	27	Address Line 12	ADR12/	32	Data Line E	DATE/	59
Enable			Address Line 13	ADR13/	34	Data Line F	DATF/	60

NOTE: Pins not listed are not connected to Memory System circuitry

P2 CONNECTOR PIN ASSIGNMENTS

Signal Name	Symbol	Pin No.
Memory Protect	MPRO/	20
Parity Error	PAR ERR/	29
Test Point — Advanced Write	TP-ADVW	38
Test Point — Refresh Clock	TP-REFCLK	40
Test Point — Parity 0 & 1	TP-PART 0 & 1	42

Signal Name	Symbol	Pin No.
Test Point — Parity 2 & 3	TP-PART 2 & 3	44
Ground	V_{SS}	1, 2
+5 V (Battery)	V_{CC} (BATT)	3, 4
+12 V (Battery)	V_{DD} (BATT)	
-5 V (Battery)	V_{BB} (BATT)	9, 10

NOTE Pins not listed are not connected to Memory System circuitry

MMS80XX SYSTEM

Signal (P1)	Description
ADR0/-ADRF/	Lower Order Address used to select 1 location out of 64K* block
ADR10-ADR-13/	High Order Addresss used to select one 64K block out of 1024K
DAT0/-DAT7/	Data signals for 8-bit mode or lower byte of data signals for 16-bit mode
DAT8/-DATF/	High order byte data signals for 16-bit mode
AACK/	(Programmable — 8 timing selections) Advanced Acknowledgement Signal from Memory Card in response to MWTC/ or MRDC
XACK/	Acknowledgement Signal from Memory Card indicating that Data Transfer has occurred
MRDC/	Signal to Memory Card requesting to read RAM memory
MWTC/	Signal to Memory Card requesting to write data into RAM memory
INH1/	Signal disabling response of the Memory card to MWTC/ and MRDC/
BHEN/	Signal used to enable the 16-bit mode of operation
Signal (P2)	**Description**
MPRO/	Signal used to enable the transfer from normal voltages to battery back-up voltages by disabling all circuits except refresh. Can also be used separately from battery back-up to do same thing
PAR ERR/	Signal used to indicate a Parity Error
TP-ADVW	Test Point Signal used to select Advanced Write Mode
TP-REF C/K	Test Point Signal used to clock refresh flip-flop externally (used only for evaluation purposes)
TP-PART 0 AND 1	Test Point Signal used to force a Parity Error on Reading Banks 0 or 1
TP-PART 2 AND 3	Test Point Signal used to force a Parity Error on Reading Banks 2 or 3

*K = 1024 Bytes

GENERAL DESCRIPTION

The MSM80XX series is designed for operation with SBC/BLC 80 Series Single-Board Computers (including the SBC 86/12 16-bit computer), System 80 Series Microcomputers, and Intel MDS Systems. The four configurations are plug-in replacements for Intel/National SBC/BLC 016, 032, 048, 064 memory cards.

OPTIONS

The MMS80XX series is available in four population options. Each of these configurations can be obtained with or without parity. (See Ordering Information on Page 1.) In addition to the population and parity options, provisions are made to allow the user to configure the memory card to meet system requirements. The primary user options are Address Selection, Advance-Acknowledge Response time, Early/Late Inhibit options, Advanced/Delayed Write selection, and -5 Vdc derivation.

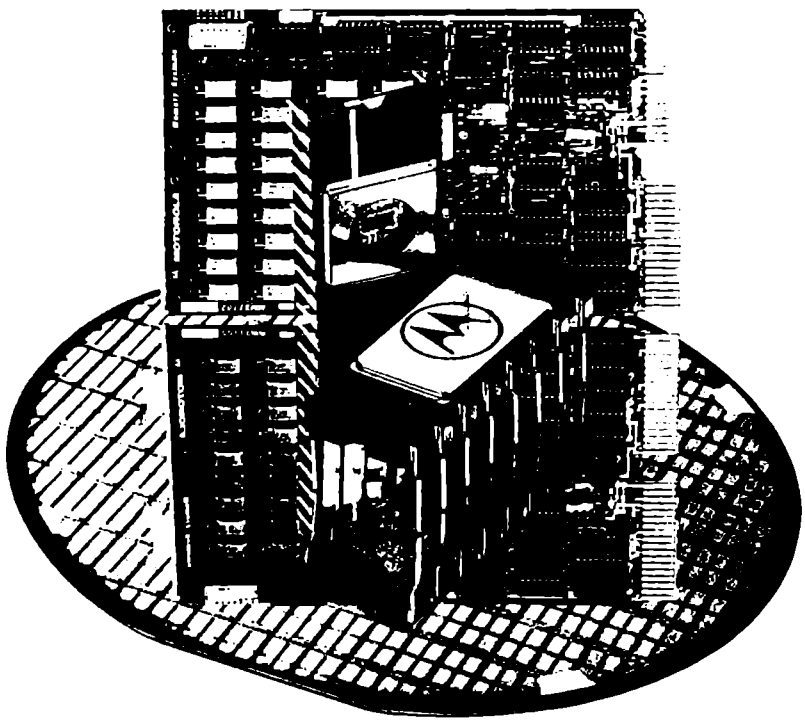
Address Selection options allow the user to locate the memory card in any one of sixteen memory segments — with each of these segments defined as a 64K memory space. If the MMS8064 is chosen, the memory system responds to all addresses within the selected memory segment. When depopulated modules (8016/8032/8048) are used, address selection for independent 8K Byte blocks is provided. The MMS8048, for example, can be configured to respond to 6 of the eight 8K blocks in the chosen segment.

Advance Acknowledge is utilized to prevent initiation of unnecessary processor "Wait" states. (In effect, the signal indicates that the memory transfer will be completed during the current cycle). The MMS80XX series allows the user to select an Advance-Acknowledge Delay Time of 100 to 450 ns (in 50 ns increments) This facilitates tailoring of the memory response time to the system speed.

An Inhibit input is provided with the MMS80XX series to allow the Bus Master to turn off the memory for certain operations. In general, the system activates this signal prior to a Memory Read (MRDC/) or Write (MWRC/) command. In certain types of systems, however, the Inhibit signal arrives after the Read/Write command. A jumper option is provided with the MMS80XX Series, allowing the Inhibit input to respond to a "Late Inhibit" signal. This option should be installed only if the system requires it, since it slows the Memory System response by approximately 50 ns.

Most SBC systems utilize a "Delayed Write" command wherein the Data is available coincident with activation of MWRC/. Some systems, however, utilize an "Advanced Write" technique, with the data becoming valid some 500 ns after the Write Command. A jumper option is provided with the MMS80XX series to allow operation in the Write Cycle. Transfer Acknowledge (XACK/) is inhibited during the dummy cycle, but Advance Acknowledge (AACK/) occurs if programmed to do so. XACK/ then occurs during the actual Write Cycle unless the system has responded to the AACK/ signal. (In this case, system response to the AACK/ signal is defined as a deactivation of the MWRC/ input). Selection of the "Advanced Write" option does not affect Read Cycle operations.

In general, SBC backplanes provide -5 volts at pins 9 and 10 of connector P1. Some systems, however, provide only -10 volts at pins 77 and 78 and/or -12 volts of pins 79 and 80. The MMS80XX Series contain an on-board negative 5 volt regulator to allow operation with such systems.



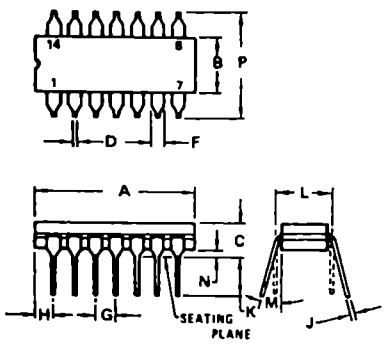
Mechanical Data

MECHANICAL DATA

The packaging availability for each device is indicated on the individual data sheets. Dimensions for the packages are given in this section.

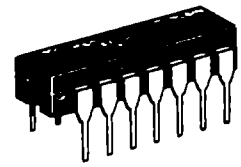
14-PIN PACKAGES

FRIT-SEAL CERAMIC PACKAGE
CASE 632



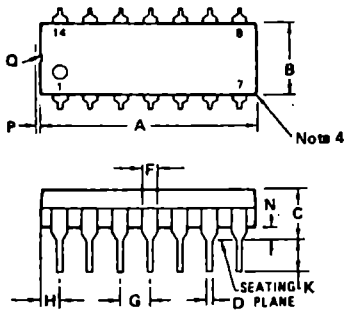
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	19.05	19.94	0.750	0.785
B	6.10	7.49	0.240	0.295
C	–	5.08	–	0.200
D	0.38	0.58	0.015	0.023
F	1.40	1.77	0.055	0.070
G	2.54 BSC		0.100 BSC	
H	1.91	2.29	0.075	0.090
J	0.20	0.38	0.008	0.015
K	3.18	5.08	0.125	0.200
L	7.62 BSC		0.300 BSC	
M	–	15°	–	15°
N	0.51	1.02	0.020	0.040

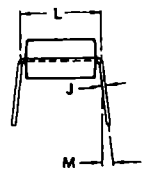
CASE 632-06



NOTES:
1. ALL RULES AND NOTES ASSOCIATED WITH MO-001 AA OUTLINE SHALL APPLY.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION "A" AND "B" (632-06) DO NOT INCLUDE GLASS RUN OUT.
4. LEADS WITHIN 0.25 mm (0.010) DIA OF TRUE POSITION AT SEATING PLANE AND MAXIMUM MATERIAL CONDITION.

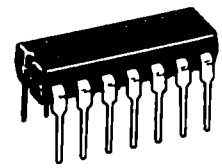
PLASTIC PACKAGE
CASE 646





DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	18.16	19.56	0.715	0.770
B	6.10	6.60	0.240	0.260
C	4.06	5.08	0.160	0.200
D	0.38	0.53	0.015	0.021
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	1.32	2.41	0.052	0.095
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	10°	0°	10°
N	0.51	1.02	0.020	0.040

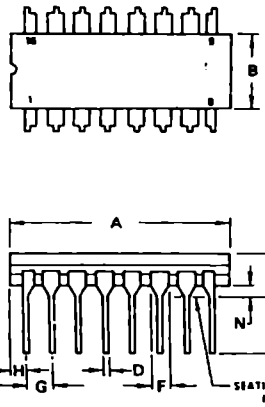
CASE 646-06

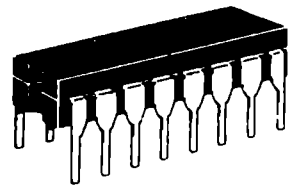


NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
4. ROUNDED CORNERS OPTIONAL.

16-PIN PACKAGES

FRIT-SEAL CERAMIC PACKAGE
CASE 620



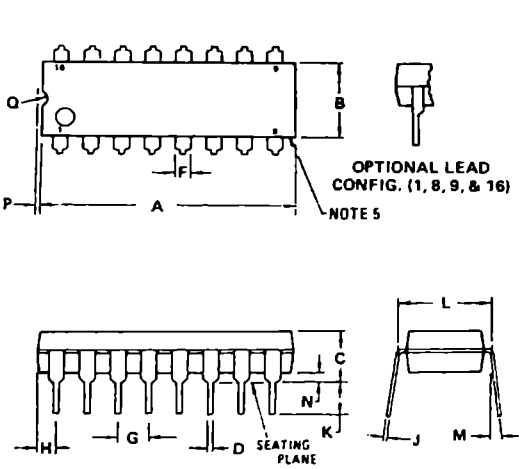


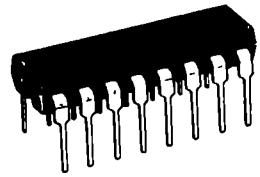
DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	19.05	19.94	0.750	0.785
B	6.10	7.49	0.240	0.295
C	–	5.08	–	0.200
D	0.38	0.53	0.015	0.021
F	1.40	1.78	0.055	0.070
G	2.54 BSC		0.100 BSC	
H	0.51	1.14	0.020	0.045
J	0.20	0.30	0.008	0.012
K	3.18	5.08	0.125	0.200
L	7.62 BSC		0.300 BSC	
M	–	15°	–	15°
N	0.51	1.02	0.020	0.040

CASE 620-06

1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. PACKAGE INDEX: NOTCH IN LEAD NOTCH IN CERAMIC OR INK DOT.
3. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIM "A" AND "B" DO NOT INCLUDE GLASS RUN-OUT.
5. DIM "F" MAY NARROW TO 0.76 mm (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

PLASTIC PACKAGE
CASE 648





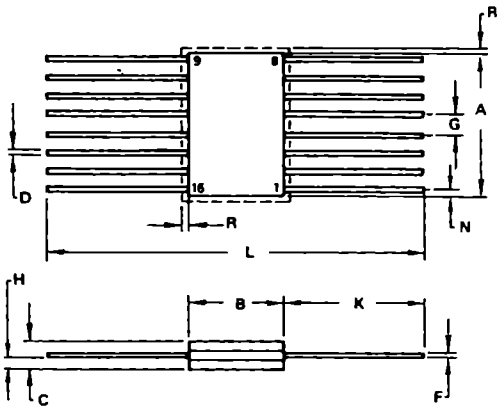
DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	18.80	21.34	0.740	0.840
B	6.10	6.60	0.240	0.260
C	4.06	5.08	0.160	0.200
D	0.38	0.53	0.015	0.021
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	0.38	2.41	0.015	0.095
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	10°	0°	10°
N	0.51	1.02	0.020	0.040

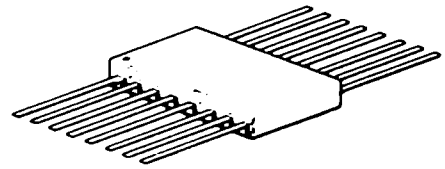
CASE 648-05

NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
4. "F" DIMENSION IS FOR FULL LEADS. "HALF" LEADS ARE OPTIONAL AT LEAD POSITIONS 1, 8, 9, and 16).
5. ROUNDED CORNERS OPTIONAL.

16-PIN PACKAGES (Continued)

CERAMIC PACKAGE
CASE 650



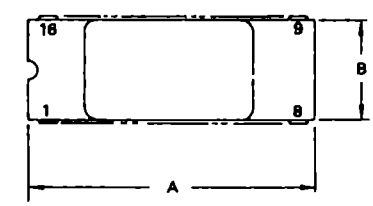


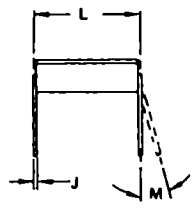
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.40	10.16	0.370	0.400
B	6.22	7.24	0.245	0.285
C	1.52	2.03	0.060	0.080
D	0.41	0.48	0.016	0.019
F	0.08	0.15	0.003	0.006
G	1.27 BSC		0.050 BSC	
H	0.64	0.89	0.025	0.035
K	6.35	9.40	0.250	0.370
L	18.92	–	0.745	–
M	–	0.51	–	0.020
R	–	0.38	–	0.015

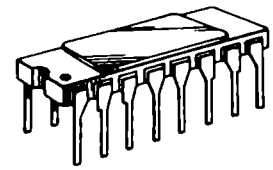
CASE 650-03

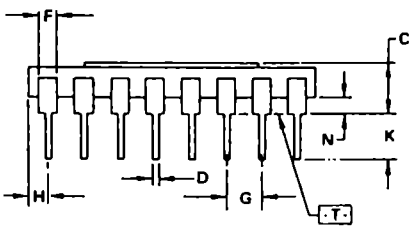
NOTES:
1. LEAD NO. 1 IDENTIFIED BY TAB ON LEAD OR DOT ON COVER.
2. LEADS WITHIN 0.13 mm (0.005) TOTAL OF TRUE POSITION AT MAXIMUM MATERIAL CONDITION.

CERAMIC PACKAGE
CASE 690









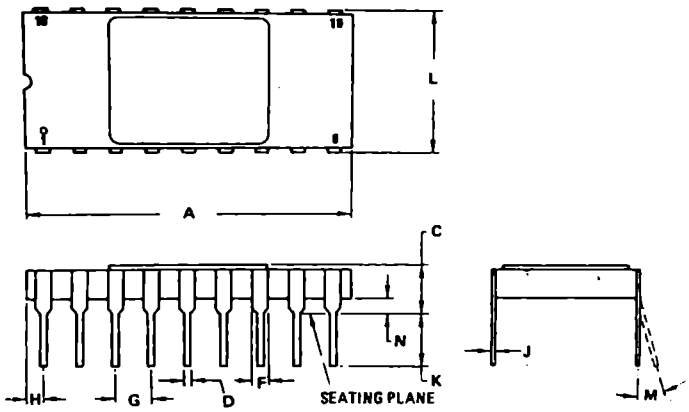
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	20.07	20.57	0.790	0.810
B	7.11	7.62	0.280	0.300
C	2.67	4.19	0.105	0.165
D	0.38	0.53	0.015	0.021
F	0.76	1.52	0.030	0.060
G	2.54 BSC		0.100 BSC	
H	0.76	1.78	0.030	0.070
J	0.20	0.30	0.008	0.012
K	3.18	5.08	0.125	0.200
L	7.62 BSC		0.300 BSC	
M	-	10°	-	10°
N	0.38	1.52	0.015	0.060

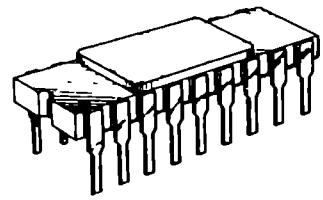
CASE 690-13

NOTES:
1. -A- AND -B- ARE DATUMS.
2. -T- IS SEATING PLANE
3. POSITIONAL TOLERANCE FOR LEADS (D). ⌖ Ø 0.25 (0.010) Ⓜ T A Ⓜ B Ⓜ
4. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.
6. 690-11 AND 690-12 OBSOLETE. NEW STANDARD 690-13.

18-PIN PACKAGES

CERAMIC PACKAGE
CASE 680



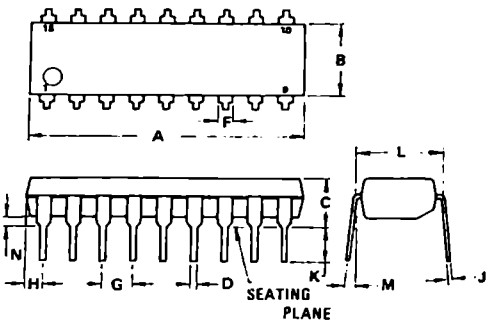


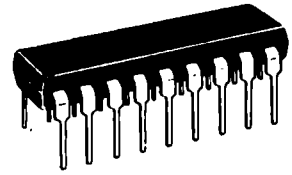
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	22.48	23.24	0.885	0.915
B	7.16	7.57	0.282	0.298
C	3.18	4.27	0.125	0.168
D	0.38	0.58	0.015	0.023
F	0.76	1.40	0.030	0.055
G	2.54 BSC		0.100 BSC	
H	1.02	1.52	0.040	0.060
J	0.20	0.30	0.008	0.012
K	2.68	4.44	0.105	0.175
L	7.37	7.87	0.290	0.310
M	–	10°	–	10°
N	0.38	1.40	0.015	0.055

CASE 680-06

NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RAD OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

PLASTIC PACKAGE
CASE 701-01





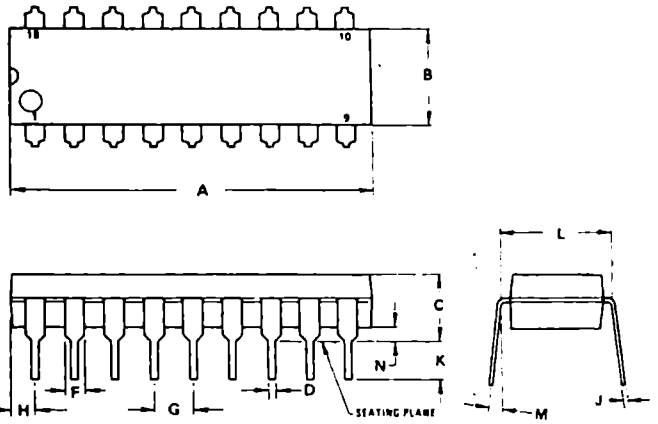
NOTES
1. LEADS WITHIN 0.13 mm (0.005) RADIUM OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION (DIM "G")
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

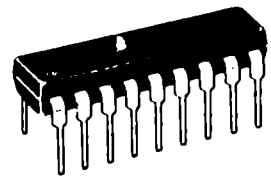
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	23.11	23.88	0.910	0.940
B	6.10	6.60	0.240	0.260
C	4.06	4.57	0.160	0.180
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.32	1.83	0.052	0.072
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.37	7.87	0.290	0.310
M	0°	10°	0°	10°
N	0.51	1.02	0.020	0.040

CASE 701-01

18-PIN PACKAGES (Continued)

PLASTIC PACKAGE
CASE 707



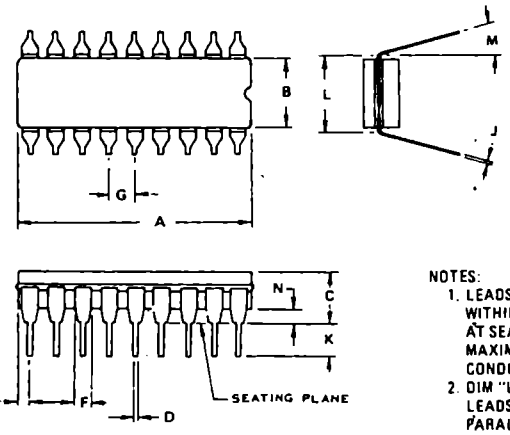


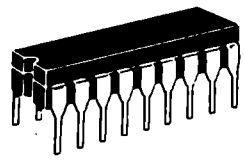
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	22.22	23.24	0.875	0.915
B	6.10	6.60	0.240	0.260
C	3.94	4.57	0.155	0.180
D	0.36	0.56	0.014	0.022
F	1.27	1.78	0.050	0.070
G	2.54 BSC		0.100 BSC	
H	1.02	1.52	0.040	0.060
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

CASE 707-02

NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25mm(0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

FRIT SEAL CERAMIC PACKAGE
CASE 726





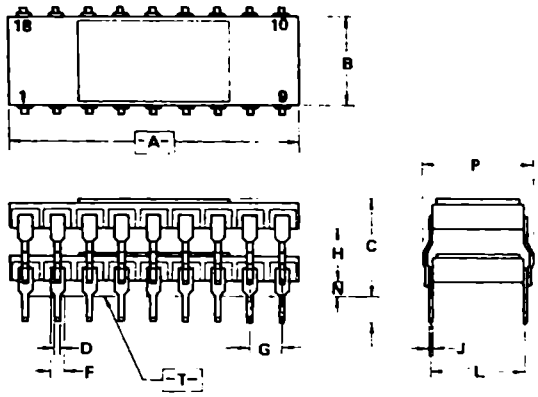
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	22.35	23.11	0.880	0.910
B	7.11	7.75	0.280	0.305
C	–	4.06	–	0.160
D	0.41	0.51	0.016	0.020
F	1.27	1.52	0.050	0.060
G	2.54 BSC		0.100 BSC	
H	–	1.40	–	0.055
J	0.20	0.30	0.008	0.012
K	–	4.44	–	0.175
L	7.37	8.00	0.290	0.315
M	0°	15°	0°	15°
N	0.51	1.27	0.020	0.050

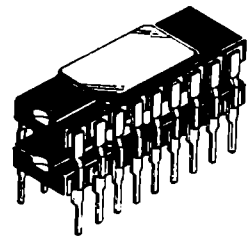
CASE 726-02

NOTES:
1. LEADS, TRUE POSITIONED WITHIN 0.25 mm,(0.010) DIA. AT SEATING PLANE, AT MAXIMUM MATERIAL CONDITION.
2. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIM "A" & "B" INCLUDES MENISCUS.

18-PIN PACKAGES (Continued)

CERAMIC PACKAGE
CASE 749





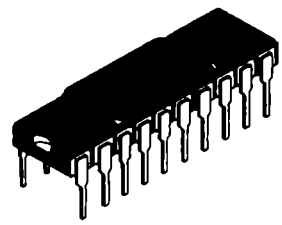
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	22.61	23.11	0.890	0.910
B	7.24	7.75	0.285	0.305
C	–	8.64	–	0.340
D	0.36	0.61	0.014	0.024
F	0.89	1.40	0.035	0.055
G	2.54 BSC		0.100 BSC	
H	3.30	–	0.130	–
J	0.23	0.30	0.009	0.012
K	–	2.92	–	0.115
L	7.37	7.87	0.290	0.310
N	0.64	1.14	0.025	0.045
P	–	9.14	–	0.360

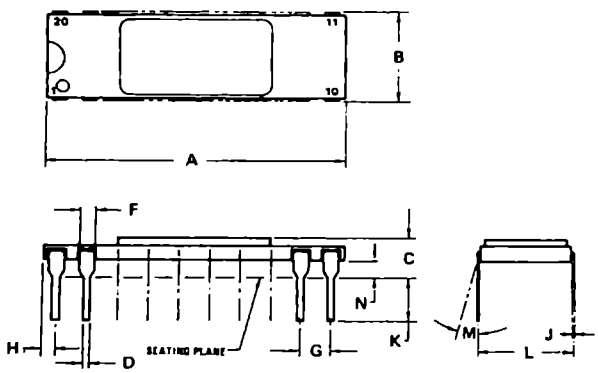
CASE 749-01

NOTES:
1. DIMENSION [A] IS DATUM.
2. POSITIONAL TOLERANCE FOR LEADS:
   ⌖ 0.25 (0.010) Ⓜ T A Ⓜ
3. [T] IS SEATING PLANE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

20-PIN PACKAGE

CERAMIC PACKAGE
CASE 729





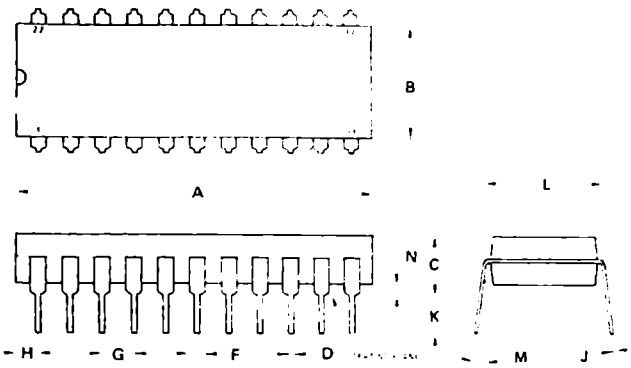
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	24.64	25.91	0.970	1.020
B	7.06	8.13	0.278	0.320
C	2.79	4.70	0.110	0.185
D	0.38	0.51	0.015	0.020
F	1.14	1.40	0.045	0.055
G	2.54	BSC	0.100	BSC
H	0.89	1.52	0.035	0.060
J	0.20	0.30	0.008	0.012
K	3.18	4.57	0.125	0.180
L	7.62	BSC	0.300	BSC
M	0°	10°	0°	10°
N	0.51	1.52	0.020	0.060

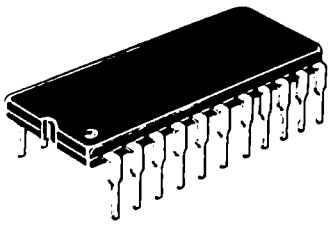
CASE 729-02

NOTE:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE, AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.

22-PIN PACKAGES

PLASTIC PACKAGE
CASE 708





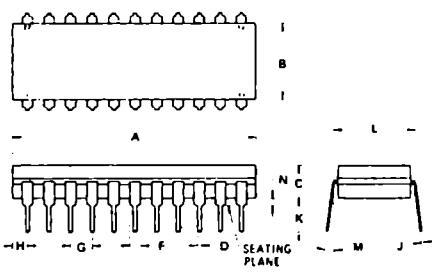
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	27.56	28.32	1.085	1.115
B	8.64	9.14	0.340	0.360
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.27	1.78	0.050	0.070
G	2.54 BSC		0.100 BSC	
H	1.02	1.52	0.040	0.060
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	10.16 BSC		0.400 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

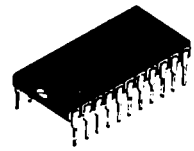
CASE 708-04

NOTES

1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25mm(0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH

FRIT-SEAL CERAMIC PACKAGE
CASE 736





DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	26.80	27.81	1.055	1.095
B	9.14	9.91	0.360	0.390
C	3.81	5.48	0.150	0.215
D	0.38	0.53	0.015	0.021
F	1.27	1.65	0.050	0.065
G	2.54 BSC		0.100 BSC	
H	0.51	1.27	0.020	0.050
J	0.20	0.38	0.008	0.015
K	2.54	4.32	0.100	0.170
L	9.91	10.41	0.390	0.410
M	-	15°	-	15°
N	0.25	0.89	0.010	0.035

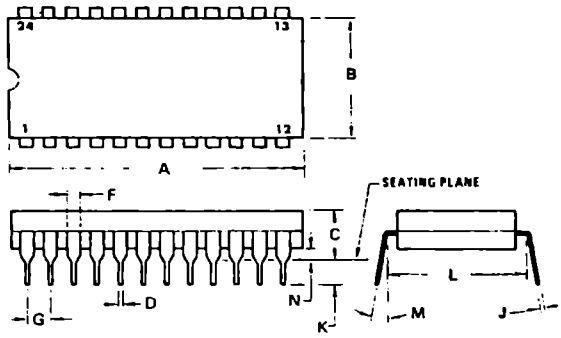
CASE 736-01

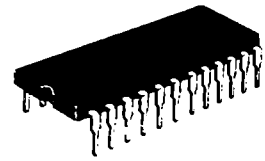
NOTES

1. LEADS TRUE POSITIONED WITHIN 0.25 mm (0.010) DIA AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION (DIM "D")
2. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

24-PIN PACKAGES

FRIT-SEAL CERAMIC PACKAGE
CASE 623



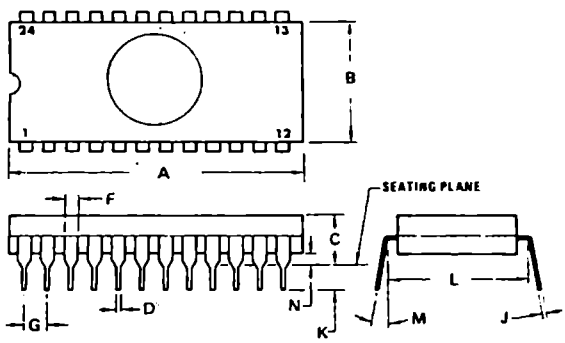


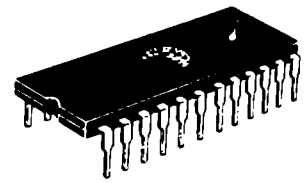
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	31.24	32.77	1.230	1.290
B	12.70	15.49	0.500	0.610
C	4.06	5.59	0.160	0.220
D	0.41	0.51	0.016	0.020
F	1.27	1.52	0.050	0.060
G	2.54 BSC		0.100 BSC	
J	0.20	0.30	0.008	0.012
K	2.29	4.06	0.090	0.160
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.27	0.020	0.050

CASE 623-04

NOTES:
1. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
2. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION. (WHEN FORMED PARALLEL)

FRIT-SEAL CERAMIC PACKAGE
CASE 623A





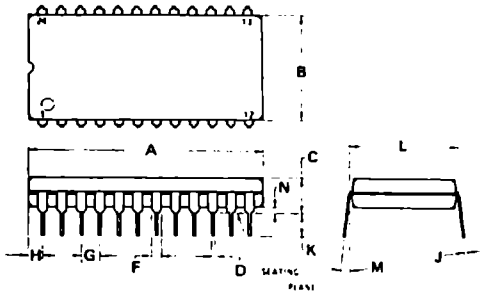
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	31.24	32.77	1.230	1.290
B	12.70	15.49	0.500	0.610
C	4.06	5.84	0.160	0.230
D	0.41	0.51	0.016	0.020
F	1.27	1.52	0.050	0.060
G	2.54 BSC		0.100 BSC	
J	0.20	0.30	0.008	0.012
K	2.29	4.06	0.090	0.160
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.27	0.020	0.050

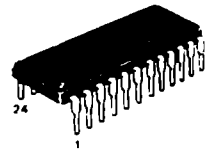
CASE 623A-02

NOTES:
1. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
2. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION. (WHEN FORMED PARALLEL).

24-PIN PACKAGES (Continued)

PLASTIC PACKAGE
CASE 709



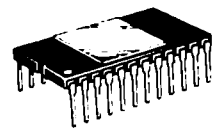


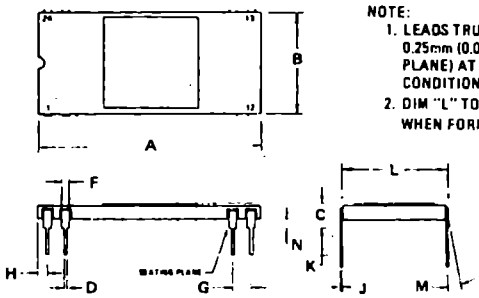
NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 mm (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	31.37	32.13	1.235	1.265
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.03	0.065	0.080
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

CASE 709-02

CERAMIC PACKAGE
CASE 716





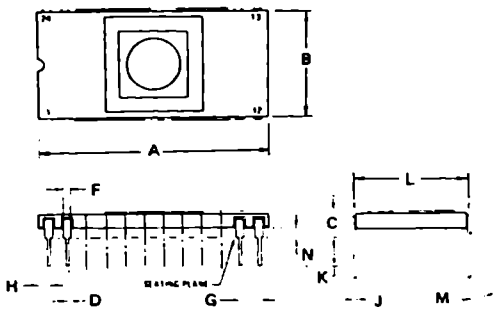
NOTE:
1. LEADS TRUE POSITIONED WITHIN 0.25mm (0.010) DIA (AT SEATING PLANE) AT MAXIMUM MATERIAL CONDITION.
2. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	27.64	30.99	1.088	1.220
B	14.94	15.34	0.588	0.604
C	2.67	4.32	0.105	0.170
D	0.38	0.53	0.015	0.021
F	0.76	1.40	0.030	0.055
G	2.54 BSC		0.100 BSC	
H	0.76	1.78	0.030	0.070
J	0.20	0.30	0.008	0.012
K	2.54	4.19	0.100	0.165
L	14.99	15.49	0.590	0.610
M	-	10°	-	10°
N	1.02	1.52	0.040	0.060

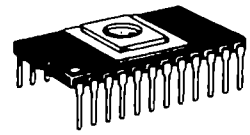
CASE 716-06

24-PIN PACKAGES (Continued)

CERAMIC PACKAGE
CASE 716



NOTE:
1. LEADS TRUE POSITIONED WITHIN 0.25mm (0.010) DIA (AT SEATING PLANE) AT MAXIMUM MATERIAL CONDITION.
2. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.



	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	27.64	30.99	1.088	1.220
B	14.73	15.34	0.580	0.604
C	3.18	5.08	0.125	0.200
D	0.38	0.53	0.015	0.021
F	0.76	1.40	0.030	0.055
G	2.54 BSC		0.100 BSC	
H	0.76	1.78	0.030	0.070
J	0.20	0.30	0.008	0.012
K	2.54	4.57	0.100	0.180
L	14.99	15.49	0.590	0.610
M	-	10°	-	10°
N	1.02	1.52	0.040	0.060

CASE 716-07

NOTES

1 SELECTOR GUIDES CROSS-REFERENCE

2 MOS Memories
RAM, EPROM, EEPROM, ROM

3 CMOS Memories
RAM, ROM

4 Bipolar Memories
TTL, MECL-RAM, PROM

5 Memory Boards

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